

# Simulation Of Two Stage Operational Amplifier Using 250nm And 350nm Technology

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## Abstract

As the CMOS process entering the nanometre scale analog circuit will need to operate in lower and lower supply voltage. This trend is primarily driven by the need to low power and low voltage requirement on the consumer electronics market. High gain enables the circuit to operate efficiently in a closed loop feedback system. The design is simulated in TSMC 250nm and 350nm CMOS process technology at 2.5V and 3V supply voltages respectively. Supply voltage under room temperature 27°C. The simulation result shows that a bandwidth is 2.19MHz and 22.86MHz in 250nm and 350nm technology. Gain is 59.69dB and 56.63dB achieved for the two stage op-amp circuit in 250nm and 350nm technology.

## 1. Introduction

Operational amplifier is among the most used electronics devices today, used in a wide range of consumer devices, industrial and scientific. Op-amp are available in many topologies, a two stage op-amp is an example of this kind, which is used when the high input impedance and low output impedance is needed.

The objective of the design methodologies in this paper is to propose a simple but accurate equation for the design of high gain two stage CMOS op-amp. To do this, a simple analysis with some significant parameters (phase margin, bandwidth etc.) is performed. The simulation results have been obtained by TSMC 250nm and 350nm CMOS technology. Design has been carried out in Mentor Graphics tool.

## 2. Block Diagram of Two Stage Operational Amplifier

Operational amplifier is the backbone for many analog circuit designs. Simulation of all parameters in a design has become mandatory now a day. We choose a simple pair differential amplifier immune input amplifier, a common source amplifier to the output amplifier, a current mirror circuit as bias circuit, and a buffer circuit compensation current as

well as a Miller capacitance in series with one another.

The topology of the circuit designed is that of a standard CMOS two stage op-amp. It comprised of three subsections of circuits, first is differential gain stage, second gain stage and bias strings.

### Differential Gain Stage:

The first section of interest is the differential gain stage which is comprised of transistor M1 to M4. In figure 1 transistor M1 and M2 are N-channel MOSFET transistor which from the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate M2 is non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The transconductance of this stage is simply the transconductance of M1 or M2.

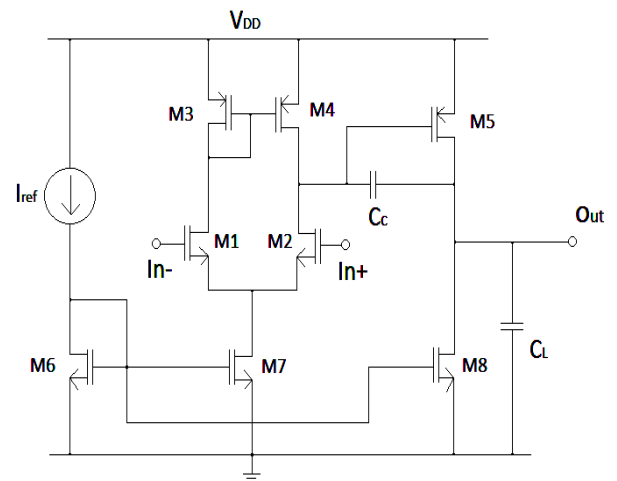


Figure 1 the topology chosen for this op-amp design

M3 and M4 is the active load transistor of the differential amplifier. The current mirror active load used in this circuit has three distinct advantages. First, the uses of active load devices create a large output resistance in a relatively small amount die area. The current mirror topology performs the differential to single-ended conversion of the input signal, and finally, the load also helps with common mode rejection ratio. In this stage, the conversion from differential to single ended is achieved by using a current mirror (M3

and M4). The current from M1 is mirrored by M3 and M4 and subtracted from the current from M2.

**Second Gain stage:**

The second stage is a current sink load inverter. The purpose of the second gain stage, as the name implies, is to provide additional gain, in the amplifier. Consisting of transistor M5 and M8, this stage takes the output from the drain of M2 and amplifies it through M5 which is in the standard common source configuration. This stage employs an active device M8, to serve as the load resistance for M5. The gain of this stage is the transconductance of M5 times the effective load resistance comprised of the output resistance of M5 and M8. M8 is the driver while M7 acts as load.

**Bias String:**

The biasing of the operational amplifier is achieved with only two transistors along with a current source. Transistor M6 and the current source supply a voltage between the gate and source of M7 and M8. M6 is diode connected to ensure it operate in the saturation region. Proper biasing of the other transistor in the circuit is controlled by the node voltages present in the circuit itself.

**3. Simulation Result**

**Simulation result in 250nm Technology**

Frequency Response: Obtained result in 250nm technology. Gain is 59.69dB, gain margin = 12.98dB. Phase margin for 250nm technology is 78.82° and bandwidth is 2.19MHz. Power dissipation is 2.09mW.

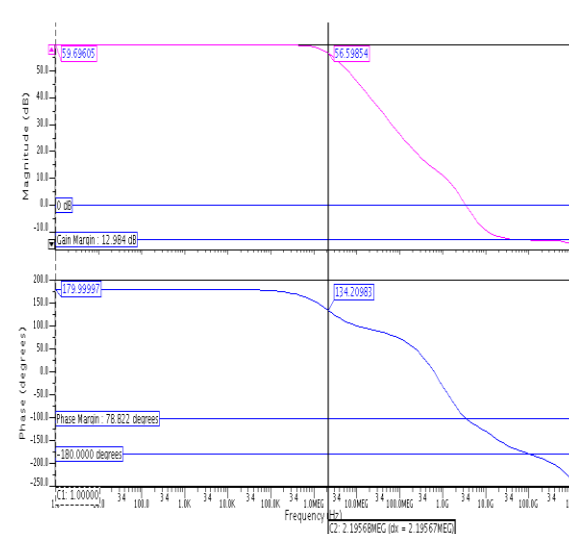


Figure 2 frequency responses in 250nm technology

ICMR: Input Common Mode Range is -0.99V to 1V.

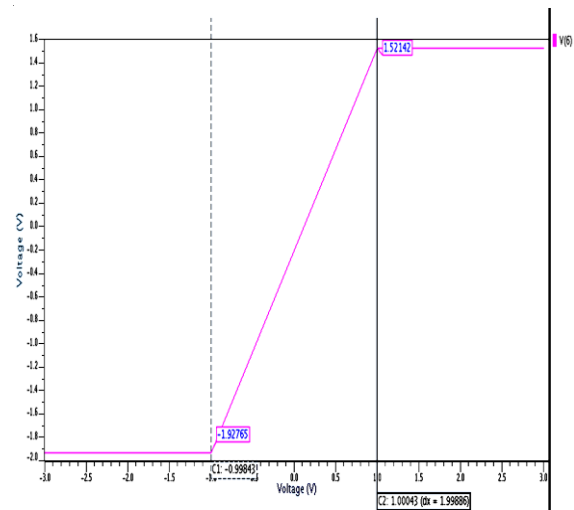


Figure 3 ICMR in 250nm technology

Offset: Output offset voltage is 7mV.

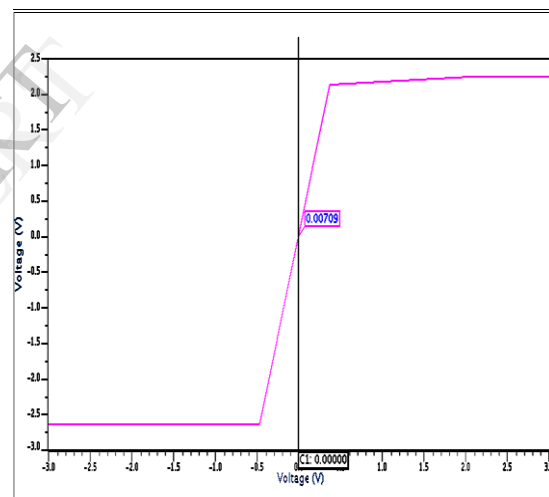


Figure 4 Offset in 250nm technology

**Simulation result in 350nm Technology**

Frequency Response: Obtained result in 350nm technology. Gain is 56.63 dB, gain margin = 17.49 dB. Phase margin for 350nm technology is 88.66° and bandwidth is 22.86MHz. Power dissipation is 3.93mW.

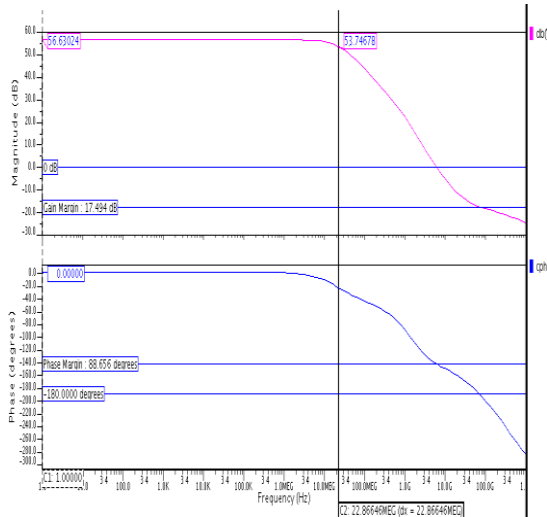


Figure 5 frequency responses in 350nm technology

ICMR: Input Common Mode Range is -0.49V to 1.5V.

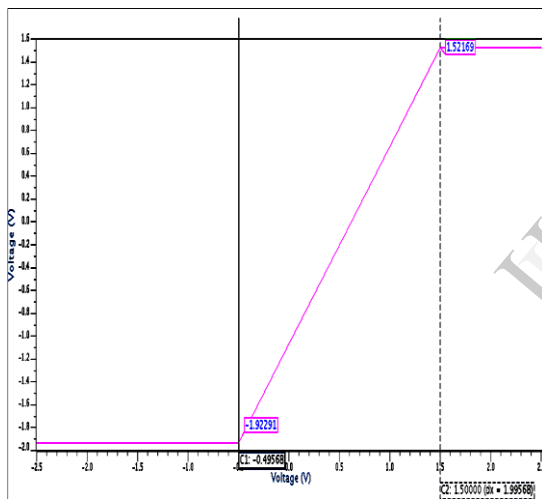


Figure 6 ICMR in 350nm technology

Offset:

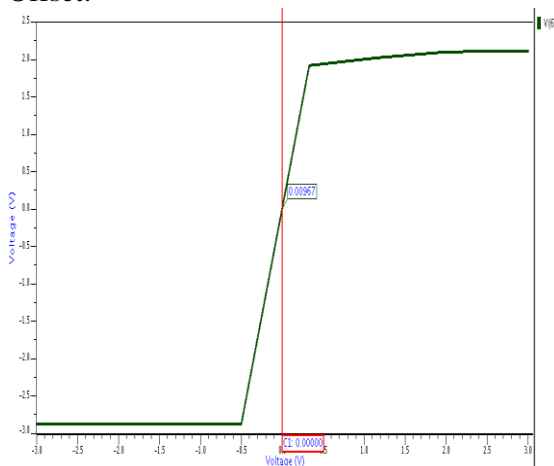


Figure 7 Offset in 350nm technology

This is simulation results of two stage operational amplifier in two different TSMC technologies.

Table 1: Comparison between 250nm and 350nm technology results

Parameters	Technologies	
	250nm	350nm
Supply Voltage (V)	2.5	3.0
Gain (dB)	59.69	56.63
Gain Margin (dB)	12.98	17.49
Phase Margin (°)	78.82	88.66
Bandwidth (MHz)	2.19	22.86
Power Dissipation (mW)	2.09	3.93
ICMR (V)	-0.99 to 1.0	-0.49 to 1.5
Offset (mV)	7	9

#### 4. Design Methodology for Op-Amp

Determine the necessary open-loop gain (Ao)

$$g_{m1} = g_{m2} = g_{m1}, g_{m6} = g_{m11}, g_{ds2} + g_{ds4} = G_I, \text{ and}$$

$$g_{ds6} + g_{ds7} = G_{II}$$

$$I_d = \frac{\mu_{n,p} C_{ox} \left(\frac{W}{L}\right) V_{eff}^2}{2}$$

$$g_m = \sqrt{2\mu_{n,p} C_{ox} \frac{W}{L} I_d}$$

$$\text{Slew Rate } SR = \frac{I_5}{C_c}$$

First Stage Gain

$$A_{v1} = \frac{-g_{m1}}{g_{ds2} + g_{ds4}} = \frac{-2g_{m1}}{I_5(\lambda_2 + \lambda_4)}$$

Second Stage Gain

$$A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \frac{-g_{m6}}{I_6(\lambda_6 + \lambda_7)}$$

$$\text{Gain Bandwidth } GB = \frac{g_{m1}}{C_c}$$

$$\text{Output Pole } p_2 = \frac{-g_{m6}}{C_L}$$

$$\text{RHP zero } Z_1 = \frac{g_{m6}}{C_c}$$

Positive CMR

$$V_{in}(\text{max}) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|(\text{max}) + V_{T1}(\text{min})$$

Negative CMR

$$V_{in}(\text{min}) = V_{SS} - \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(\text{max}) + V_{DS5}(\text{sat})$$

$$\text{Saturation Voltage } V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}}$$

It is assumed that all transistors are in saturation for the above relationships.

## 5. Conclusion

In these paper two stage op amps is simulated in two different TSMC 250nm and 350nm technology. Power dissipation in 250nm technology is 2.09mW and in 350nm technology 3.93mW. Gain is 59.69 and 56.63 in 250nm and 350nm respectively. Supply voltage is 2.5V in 250nm and 3.0V in 350nm technology. In my future work I will improve gain and bandwidth and also decrease power dissipation and offset.

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