International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 06, June-2015

Simulation of a Software Phase-Locked Loop for Typical Grid Disturbances

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***Abstract*— During the last year various techniques of electrical synchrony have been proposed for the interconnection of local power generation systems of small scale with the national electrical grid. This paper presents the simulation of second-grade software Phase-Locked Loop (PLL), to analyze the state of engagement (phase tracking) when the reference signal has disturbances.**

Keywords—SPLL, Phase Locked Loop, Loop Filter (LF), grid disturbances.

I. INTRODUCTION

Most applications of local systems for power generation (LSG) connected to the utility power grid require synchronization between the grid voltage and the voltage synthesized by the converter.

In many cases, the reference signal obtained from the grid voltage is contaminated by harmonics, which may have been produced by the power converter itself or generated elsewhere [1].

The most widely accepted solution to provide synchronization between time-varying signals is the use of a Phase-Locked Loop (PLL) system [8]. A PLL is a device which causes one signal to track another one. It keeps output signal synchronization with a reference input signal in frequency as well as in phase [2].

Every type of PLL (lineal PLL (LPLL), digital PLL, etc.), can be implemented by software (SPLL) [3].The design of a SPLL (Software-PLL) is similar to analog PLL, The advantage of such a software implemented is that the loop could be easily modified to incorporate signal processing components to improve the performances of the PLL [4].The block diagram of SPLL is given in Fig. 1, the first block is Analog Digital Converter (ADC), the phase detector is a multiplier (MUL), a proportional Integral controller (PI) is the loop filter, and in the last block a Digital Controller Oscillator (DCO) is located in the last block [5].

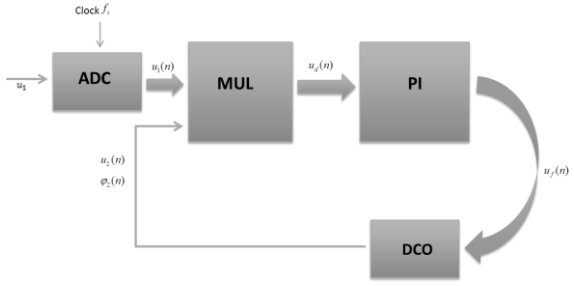

Fig. 1 Block diagram of SPLL

The goal of this work is to analyze the performance in phase tracking of a software-based lineal PLL (SLPLL) second-degree, when a reference electrical signal has normal and abnormal conditions. The SLPLL is tuned to work with the Mexican Electrical System (MES) 60 Hz of operation frequency.

The organization of the paper is as follow: in the next section the PLL components are studied, the second-order PLL structure is discussed in the subsequent stage, in the last three sections; filter design and simulation, second-order PLL simulation and results are presented.

II. PLL COMPONENTS

A phase-locked loop is a feedback system combining a voltage controlled oscillator (VCO) and a phase comparator so connected that the oscillator maintains a constant phase angle relative to a reference signal [6]. Fig. 2 shows the basic model for a PLL. The basic blocks of the PLL are the Error Detector (composed of a phase frequency detector), Loop Pass Filter (LPF), and VCO.

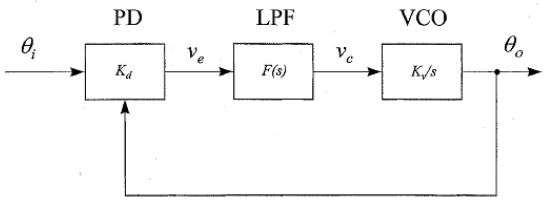

Fig. 2 Lineal basic model of the phase-locked loop [2]

A. *Phase Detector (PD)*

A phase detector is a device capable of generating a signal which is proportional to the phase difference between two signals, a multiplier is used usually [7].

B. *Loop Filter*

The next stage after the phase detector is the loop filter. The loop filter aim is to do stable the PLL, filtering the unwanted high frequencies. The PLL acts as a low pass, eliminating noise and spurious signals input and as a high pass to VCO noise [8].

C. *Voltage controlled oscillator (VCO)*

The VCO operates at a set frequency. If the frequency of the reference signal is near to the VCO frequency, the PLL feedback causes the VCO is engaged with the input signal. The VCO input is a voltage and the output is a frequency. [9].

III. SECOND-ORDER PLL DESCRIPTION

The second-order PLL system contains a first-order filter and a voltage controlled oscillator (VCO) [10]. The transfer function of an analog loop filter (1) and a VCO (2) are [10]:

$$F(s) = \frac{1}{s}\frac{\tau_2 s + 1}{\tau_1} \quad (1)$$

$$N(s) = \frac{K_O}{s} \quad (2)$$

Where F(s) and N(s) are the transfer functions of the filter and VCO. Ko is the VCO gain. The transfer of a linearized analog PLL is [11] (3).

$$H(s) = \frac{K_d F(s) N(s)}{1 + K_d F(s) N(s)} \quad (3)$$

K_d is the PD gain. Substituting Equations (1) and (2) in (3) yields (4)

$$H(s) = \frac{2\zeta\,\omega_n s + \omega_n^2}{s^2 + 2\zeta\,\omega_n s + \omega_n^2} \quad (4)$$

Where the natural frequency $\omega_n = \sqrt{(K_o K_d)/\tau_1}$, and the damping ratio $\zeta = (\tau_2 \omega_n)/2$ [10]. The damping ratio controls how fast the filter reaches its settle point, also controls how much overshoot the filter can have. The damping is chosen to ζ = 0.7 resulting in a filter that converges reasonably fast [[10].

The transfer function (4) is analog version and to convert the transform function to digital form; for future implementation in a DSP, the bilinear z transformation is used; this yields the following digital transfer functions for the PLL model (5).

$$H_1(z) = \frac{(4\zeta\omega_n T + (\omega_n T)^2) + 2(\omega_n T)^2 z^{-1} + ((\omega_n T)^2 - 4\zeta\omega_n T) z^{-2}}{(4 + 4\zeta\omega_n T + (\omega_n T)^2) + (2(\omega_n T)^2 - 8) z^{-1} + (4 - 4\zeta\omega_n T + (\omega_n T)^2) z^{-2}} \quad (5)$$

In-lock state, the output of the phase detector can be approximated as (6)

$$u_d \approx K_d \theta_e \quad (6)$$

IV. FILTER DESIGN AND SIMULATION

An active filter PI offers a good performance of a SPLL [12], it is assumed that (1) is the transfer function of an active filter PI in digital form, obtained through bilinear transformation (7).

$$F_z = \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}} \quad (7)$$

The filter coefficients are given by (8), (9), (10) and (11):

$$a_0 = 1 \quad (8)$$

$$a_1 \approx -1 \quad (9)$$

$$b_0 = \frac{T}{2\tau_1}\left[1 + \frac{1}{\tan(T/2\tau_2)}\right] \quad (10)$$

$$b_1 = \frac{T}{2\tau_1}\left[1 - \frac{1}{\tan(T/2\tau_2)}\right] \quad (11)$$

A. *Matlab® Filter simulation*

Matlab ™ is used as a tool for simulating the PI filter algorithm. The choice of Matlab ™ as programming and simulation environment was for the simplicity of use and the ability to integrate systems.

The technical specifications for the simulation of the algorithm are:

- Reference signal sinusoidal frequency 60 Hz. and amplitude 1 V.
- Sampling frequency 8000 Hz.
- DCO center frequency 60 Hz (376.9911 rad/s).
- PLL lock range 59.5 Hz to 60.5 Hz. operating frequencies required by the "Comisión Federal de Electricidad (CFE)" parastatal that manages the supply of electricity in México.

The simulated filter is analog type with amplification near to 60 Hz frequency to improve the performance of closed loop and the PLL lock range.

The filter coefficients are calculated according to (8), (9), (10) and (11), and substituted in (7), obtaining the following values:

a_0= 1,
a_1= -0.9612,
b_1= -0.2869,
b_2= 0.3256.

The filter response is shown in Fig. 3. The figure shows attenuation in the frequency close to 60 Hz (376.9911 rad/s).

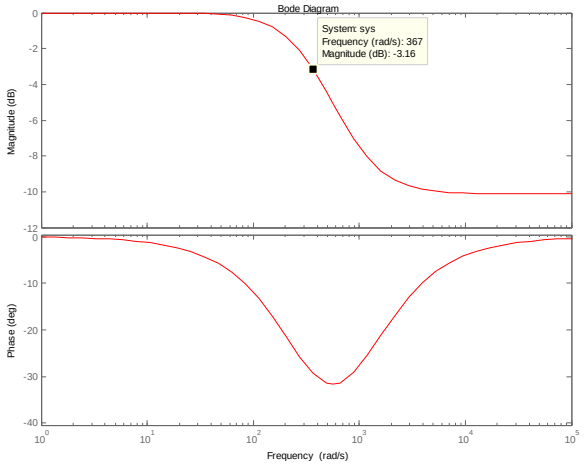

Fig. 3 Filter response

V. SECOND-ORDER PLL SIMULATION

The algorithm in Fig. 4, describes the SPLL process, begins with the initialization of the relevant variables, once the variables are initialized the algorithm enters an infinite loop and the instructions are executed repeatedly until the system is paused or turned off. Walsh function is implemented in subsequent lines and the values of all variables are updated, the next step is set back all the variables values (or displace in time) [7].

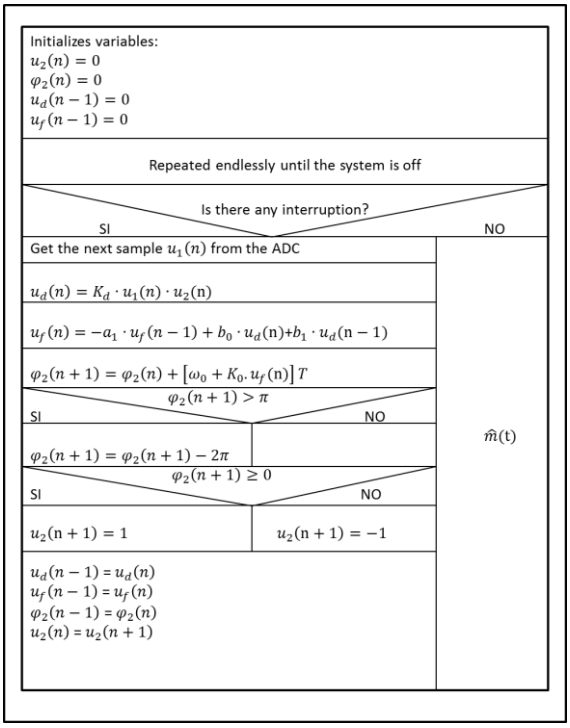

Fig. 4 Algorithm based on a PLL used for tuning radio frequency [12]

Fragment of program code [13] developed by Matlab® shown in Fig. 5.

```
ud(i)=ud_n_1;
u2(i)=u2_n;
uf(i)=uf_n_1;
phi2(i)=phi2_n;
ud_n=(input(i)*u2_n);
uf_n=(a1*uf_n_1)+(b0*ud_n)+(b1*ud_n_1)
phi2_nplus1=phi2_n+(w0+Ko*uf_n);
```

Fig. 5 Fragment of SPLL program code

In order to test the performance of the algorithm SPLL, a number of changes to the reference signal, similar to the characteristic disturbances of the mains are made.

A. *System response with an ideally stable input*

The electrical single phase signal should have a 60 Hz oscillation frequency, as shown in Fig. 6. This simulated signal is a reference for the SPLL to produce a square signal (sync pulse) with the same phase characteristics, sync pulse and the reference signal in Fig. 7 is shown, noting that they are in perfect synchrony.

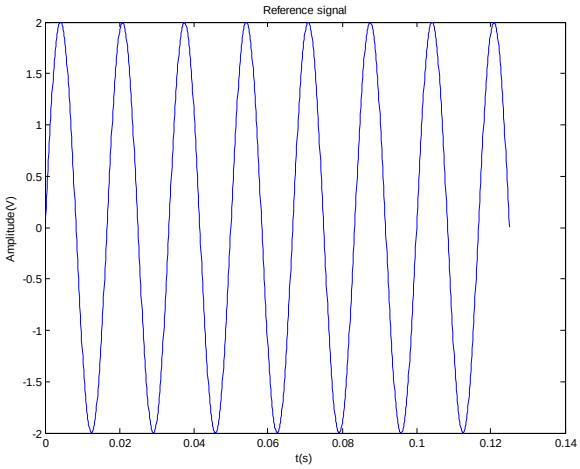

Fig. 6 Reference signal

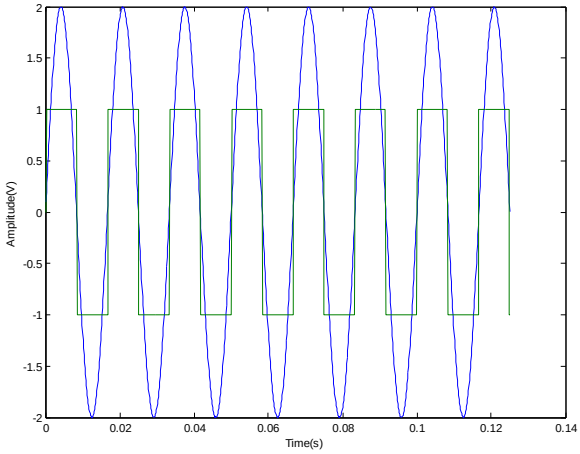

Fig. 7. Reference signal (sinusoidal wave) and sync pulse (square wave)

B. *Disturbances in the reference signal*

The transient stability of a power system can be defined as the system's ability to stay in sync when it experiences the occurrence of a severe disturbance [14] the aim of the researches on the transient stability is to determine the dynamic response of the system, during and after the occurrence of a great disturbance [15]. The disturbances such as short circuits, sudden loss of large amounts of electrical loads, own generation loss, loss of interconnection with the distribution network, network failures nearby power transmission interconnection point, are classified according to their magnitude in [15]:

- Small-scale disturbances: They are caused by normal variations in the system load and loss of small generators.
- Large-scale or severe disturbances: loss of large generators and short circuits in the transmission line.

VI. RESULTS

In this section SPLL performance is shown with different reference signals modified according the main MES disturbances.

A. 180° phase change

A phase change of 180 ° is applied in the reference signal in Fig. 8.

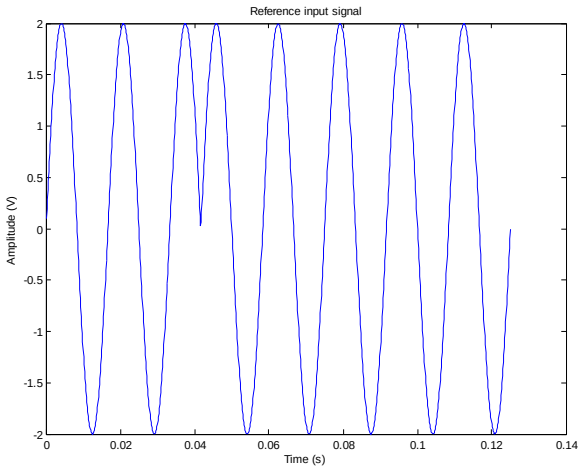

Fig. 8 Reference signal 60 Hz frequency, 180 ° phase.

Fig. 10 shows the reference signal and the synchronized pulse achieved even when the reference signal has a phase shift.

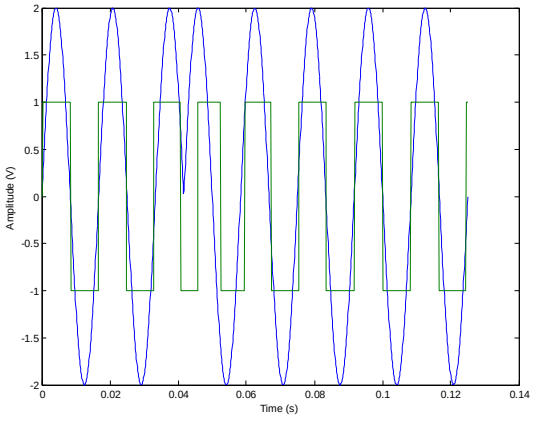

Fig. 9 Pulse in sync with a phase 180° shift reference signal

B. Harmonic analysis

Harmonics are currents and / or voltages present on an electrical system, are signals with a multiple frequency of the fundamental frequency [16]. MES has an operating frequency of 60 Hz and single phase loads that generate harmonic: the third harmonic operating at 180 Hz, 300 Hz fifth and seventh 420 Hz.

The reference signal; which is shown in Fig. 10, contains the type of harmonic described in the previous paragraph; this signal is used to check the second-order PLL level tracking the generated sync signal and the reference signal are reported in Fig. 11.

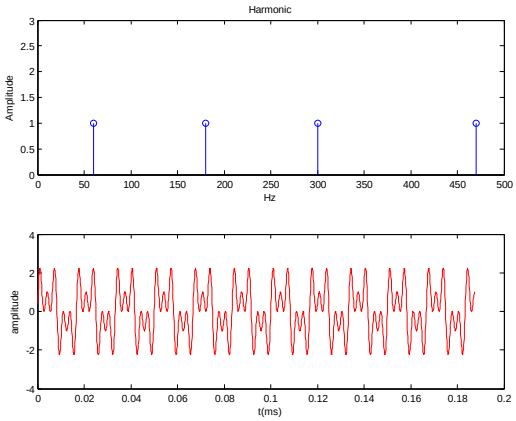

Fig. 10 Harmonics in the reference signal

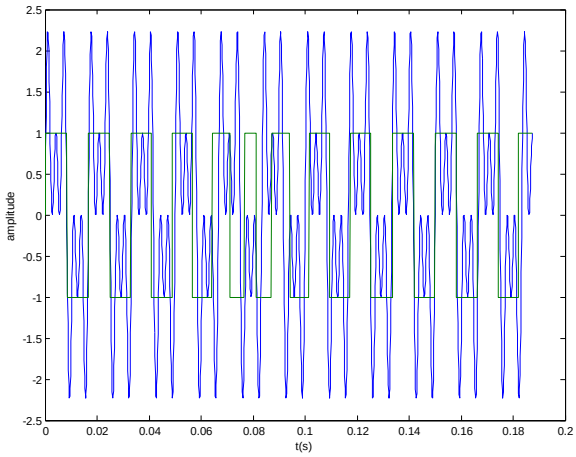

Fig. 11 System Response (green wave) to a reference signal with 3rd, 5th and 7th harmonic (blue wave)

C. Electromagnetic transients

It is called transient to the event which is undesirable and momentary. [17].

Impulse transient. It is a sudden change in the steady state condition of voltage and / or current is unidirectional with positive or negative polarity. In Fig. 12 the response of the PLL to a reference signal with abnormal conditions is observed.

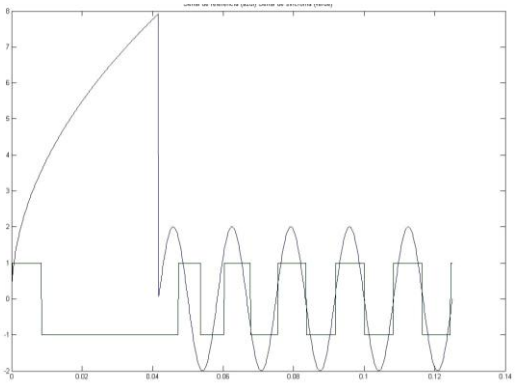

Fig. 12 PLL responses to a transient impulse.

VII. CONCLUSION

In this paper a simulation of a second-order SPLL has been presented with the aim of analyzing the performance in tracking phase of a disturbance reference signal.

The results demonstrate that the pulse generated by the PLL is able to track in phase with the reference signal. The technical characteristics of the reference signal were modified, in order to test the phase monitoring, obtaining a fast and efficient response allowing synchrony between the two signals.

Common electrical disturbances grid was used to generate changes in the reference signal and test the second-order PLL lock ability. The evidence shows that the proposed system is able to produce a sync signal in phase with the reference signal.

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