International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 3 Issue 6, June - 2014

Simulation of a Novel Phase-Shift Operated Interleaved Snubberless Current-Fed Half-Bridge Dc/Dc Converter

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***Abstract* - This paper proposes a phase-shift operated interleaved snubberless current-fed half-bridge dc/dc converter with single-phase unfolding inverter. It is suitable for grid-tied/utility interface as well as off-grid/standalone application based on the mode of control. Two snubberless current-fed half-bridge isolated dc/dc converters are interleaved in parallel input and series output configuration. The proposed converter attains clamping of the device voltage by secondary modulation, thus eliminating the need of snubber or active-clamp. Phase-shift operation is proposed to control these two converter cells, which generate a rectified sinusoidal pattern at the dc link. A simple H-bridge unfolding inverter with line frequency switching square-wave control is used to produce single-phase sine voltage. This not only simplifies the inversion stage in terms of modulation but also reduces the switching losses. Steady-state operation, analysis and design procedure are presented. Simulation results using PSIM 9.3 are obtained to verify the proposed analysis and design.**

***Keywords* - *Current-fed half-bridge (CFHB) converter, High frequency transformer (HFT), Interleaved, Phase-shift operation, Snubberless*.**

I. INTRODUCTION

In last few decades, the difference between global energy demand and limited availability of fossil fuels due to fast depletion has exponentially increasing which has resulted in change of focus towards renewable energy sources. In order to cover this increasing global energy demand and supply gap, solar energy is proving to be one of the most promising solutions.

Alternate/distributed energy sources like solar, wind, etc. produces unregulated and discontinuous output and, therefore cannot be used in its original form. A power conditioner is essential to obtain a regulated and stable output in useful form across the load. This also assists in extracting the maximum power from the source. These energy sources are integrated together with the energy storage for back-up power to form a distributed generating system focusing on long-term sustainability.

The distributed generation system is close to electricity users. Such a typical system is shown in Fig.1. Solar photovoltaic generation is a flexible power generation technique which is scalable from small-scale residential application to large-scale solar farms/power plants.

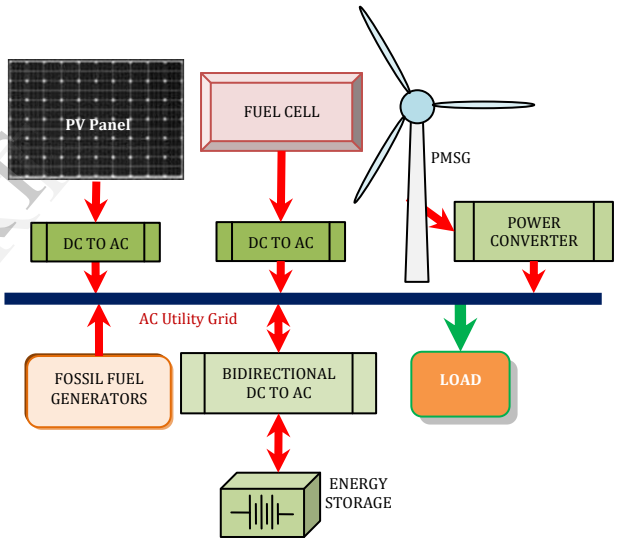

Fig.1: Hybrid distributed power generation system.

Photovoltaic power supplied to the utility grid is gaining more and more visibility, while the world's power demand is increasing. Not many PV systems have so far been placed into the grid due to the relatively high cost, compared with more traditional energy sources such as oil, gas, coal, nuclear, hydro, and wind. The price of the PV modules were in the past the major contribution to the cost of these systems. The price for the PV modules has dropped significantly over past few years due to mass production and expected to be cheaper in future. Solid-state inverters have been shown to be the enabling technology for putting PV systems into the grid.

The cost of the grid-connected inverter is, therefore, becoming more visible in the total system price. A cost reduction per inverter watt is, therefore, important to make PV-generated power more attractive. Focus has, therefore, been placed on new, cheap, and innovative inverter solutions, which has resulted in a high diversity within the inverters, and new system configurations.

Various circuit topologies for small distributed power generators are presented, compared, and evaluated against the requirements of power decoupling and dual-grounding, the capabilities for grid-connected or/and stand-alone operations is presented in [1]. In [2], various inverter topologies for connecting PV modules to a single-phase grid are presented, compared, and evaluated against demands, lifetime, component ratings, and cost.

A new class of converters based on the inductive input converters for the design of a power electronic interface for fuel cell applications is proposed in [3]. Flexible choice of components, low losses, high efficiency, and modular converter possibility are all interesting characteristics of these converters. [4] presents the implementation of an interleaved boost converter (IBC) using SiC diodes for PV applications. The converter consists of two switching cells sharing the PV panel output current. Their switching patterns are synchronized with 180◦ phase shift. In [5], a single-phase grid-connected transformerless photovoltaic inverter for residential application is presented. The inverter is derived from a boost cascaded with a buck converter along with a line frequency unfolding circuit.

In [6], a PV module integrated converter is implemented with a current fed two-inductor boost converter cascaded with a line frequency unfolder. The current source is a sinusoidally modulated two-phase buck converter with an interphase transformer. Different topologies of appropriate inverter systems in the medium power range of 20 kW and higher are presented briefly in [7]. The study includes transformerless inverters as well as two-stage inverter systems with high-frequency transformers.

A new active clamping CFHB converter is presented in [8] & [9]. [10] proposes a wide range ZVS active-clamped L-L type current-fed isolated dc–dc converter. In [11], a new ZCS-PWM current-fed dc–dc boost full-bridge converter is introduced and a comparison is made between two converter topologies - the standard ZVS active-clamp topology and a new ZCS topology.

A novel snubberless CFHB front-end isolated dc/dc converter-based inverter for PV applications is introduced in [12]. This converter attains clamping of the device voltage by secondary modulation, thus eliminating the need of snubber or active-clamp.

A novel direct current-fed interleaved phase-modulated single-phase unfolding inverter for fuel-cell applications is proposed in [13]. Two active-clamped ZVS CFHB isolated converters are interleaved in parallel input and series output configuration. Phase modulation is used to control these two converter cells, which generate a rectified sinusoidal pattern at the dc link. A simple H-bridge unfolding inverter with line frequency square-wave control is used to produce single-phase sine voltage.

In this paper, simulation of a phase-shift operated interleaved snubberless current-fed half-bridge dc/dc converter with unfolding inverter is presented. It consists of two converter cells connected in parallel input and series output configuration. Each converter cell is secondary modulated and two converter cells are operated with sinusoidal phase-shift between them at line frequency. Fig.2 shows the block diagram of the proposed topology.

The objectives of this paper are as follows: steady-state operation and analysis with secondary modulation technique and phase-shift operation for the proposed topology are discussed in Section II. A complete design procedure has been illustrated by a design example in Section III. Simulation results using PSIM 9.3 are given in Section IV to verify the proposed analysis and design.

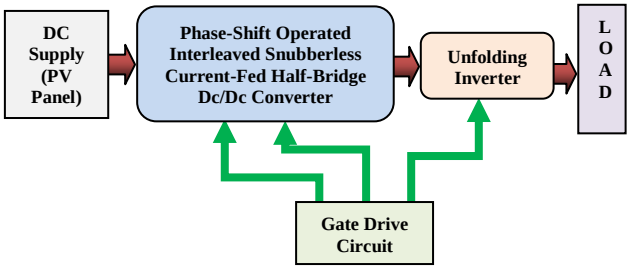

Fig.2: Block diagram of the proposed topology.

II. STEADY STATE OPERATION AND ANALYSIS

The proposed phase-shift operated interleaved snubberless CFHB dc/dc converter with unfolding inverter is shown in Fig.3. Two identical half-bridge current-fed dc/dc converter cells are connected in parallel to the input dc source. These two converters are modulated with a phase shift such that the phase difference between these two converters is a sine function at line frequency. Secondaries of the HFTs are connected in series followed by a full bridge rectifier. A low-pass filter is used to filter HF components of voltage to achieve rectified sinusoidal voltage across filter capacitor C_O at twice the line frequency. Single-phase ac voltage is obtained by simply unfolding the rectified sine wave using the H-bridge inverter with square wave control, switching at line frequency.

For PV application, maximum power point (MPP) tracking is performed by the front-end dc/dc converter either by varying the duty ratio or phase difference between the gate signals of two cells. Duty ratio is adjusted if the input voltage varies, and the output power is controlled by varying phase differences between the gate signals of two cells. In grid-tied mode, current injected into the grid is proportional to power available from the PV array. Control at the front end is implemented to optimize this injected current at MPP. Any traditional technique can be employed similar to the voltage-fed inverter.

The following assumptions are made for understanding the steady-state operation and analysis of the converter;

1) Inductors L_1 –L_4 are large enough to maintain constant current through them over a HF switching cycle.

2) Magnetizing inductance of the transformer is infinitely large;

3) All the components and devices are ideal.

4) Series inductors L_{S1} and L_{S2} represent the leakage inductance of the corresponding transformers, which are neglected during the analysis.

5) Components of both the converter cells are identical.

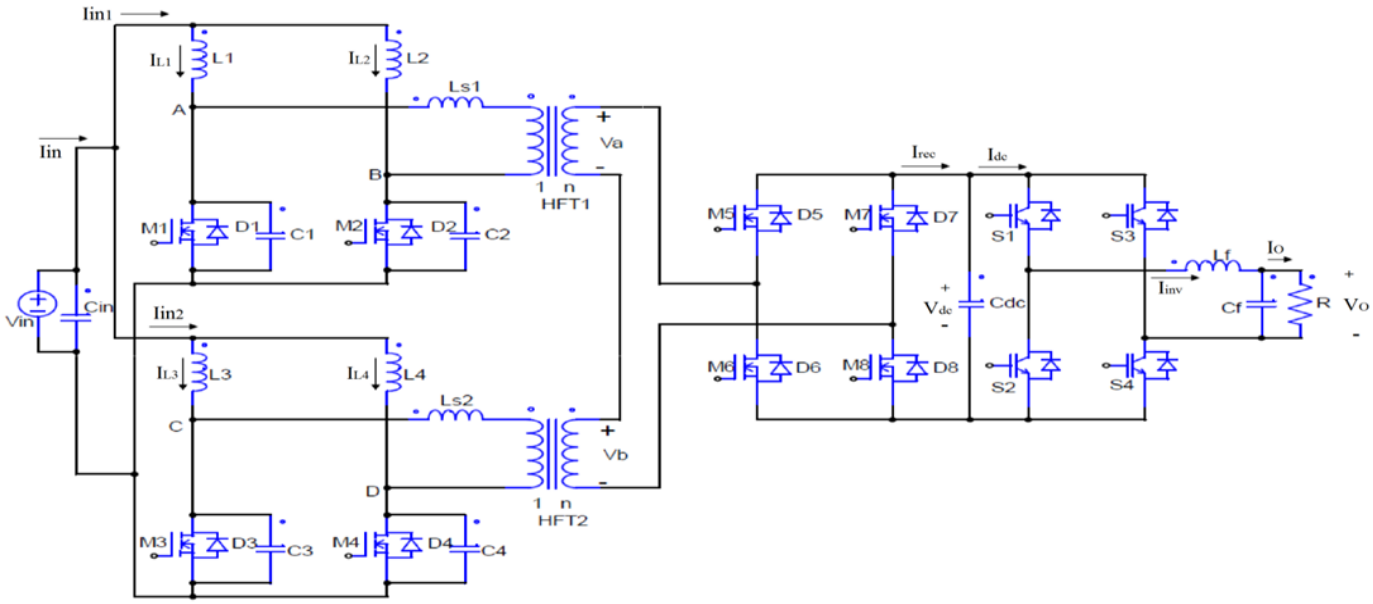

Fig.3: Proposed phase-shift operated interleaved snubberless current-fed dc/dc converter with single-phase unfolding inverter.

A. Secondary modulation

Since two converter cells are identical, for analysis purpose a single converter is considered as shown in Fig.4. In this section, steady-state operation and analysis with the ZCS concept will be explained.

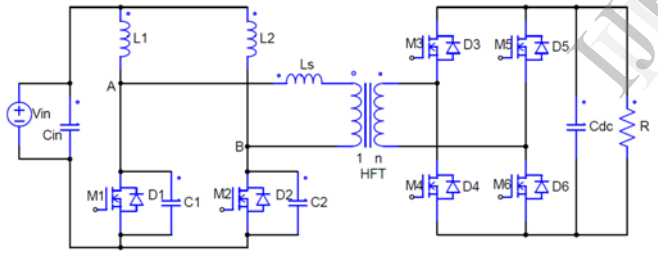

Fig.4: Current-fed half-bridge isolated dc/dc converter with full bridge on secondary.

The front-end current-fed half-bridge converter is controlled using fixed-frequency duty cycle modulation. Before the gating signal of the primary-side switch is removed to turn it OFF, two diagonal switches on the secondary side are turned ON. The reflected dc link voltage V_{dc}/n appears across the transformer primary. It diverts the current from the switch into the transformer, causing transformer current to increase and the primary switch current to decrease to zero. Once current decreases below zero, the body diode across the primary switch starts conducting and the gating signal is removed causing its ZCS turn-off or natural commutation.

The primary-side switches (M_1 and M_2) are operated with gating signals which are phase shifted by 180^0 with an overlap. The overlap varies with duty cycle that depends on the input voltage and load conditions. The duty cycles of the primary and secondary switches are denoted by d and d_r, respectively. Here, d is always greater than 50%, while d_r is always less than 50%. Switches M_3 and M_6 are operated with a duty ratio of d_r and switched off in synchronous with the switch M_2. Similarly, the turn-off of M_4 and M_5 is synchronized with the turn-off of switch M_1.

Steady-state operating waveforms of the converter (Fig.4) and the circuit conditions during different intervals in a half HF cycle are explained in detail using the equivalent circuits in [14].

Another converter is connected in input-parallel and output series configuration. Since two converter cells in proposed phase-shift operated interleaved snubberless CFHB dc/dc converter are identical (Fig.3), their operation using secondary modulation technique will be same. Switches are modulated in similar fashion with the same value of duty ratio d and d_r as the first converter, except the sinusoidal phase shift between the two converter cells.

B. Phase-shift operation

Now the phase-shift operation of the two converter cells in the proposed converter (Fig.3) will be explained.

Gate signals of switches M_1 and M_3 are phase shifted by time δ, which is given by

$$\delta = T_S/2 + \alpha \cdot \sin(\omega t) \quad (1)$$

where T_S is the time period of the HF cycle of the converter.

ω represents the frequency of the desired output sine wave in radian per second.

Magnitude of the output voltage is a function of α.

Similarly, switch pairs M_2 & M_4 have the same duty ratio and phase shifted by time δ.

When switch M_1 is turned off ($t_2 < t < t_3$ in Fig.5), voltage across the primary of the transformer, i.e., V_{AB}, is given by

$$V_{AB} = V_{in} /(1\text{-}d) \quad (2)$$

Similarly, when switch M_2 is turned off ($t_6 < t < t_7$ in Fig.5), voltage across the primary of the transformer, i.e., V_{AB}, is given by

$$V_{AB} = -V_{in} /(1\text{-}d) \quad (3)$$

From the voltage across the transformer primary for the second converter, i.e., V_{CD}, can be derived likewise. From the primary voltage, the voltage across the secondary of the transformer is calculated as a multiple of turns ratio n, which is the same for both the converter cells. The secondary of the transformers is connected in series and is rectified using a full-bridge diode rectifier. V_{rec} shows the voltage waveform at the rectifier output.

Voltages across the primary and secondary of the transformer, i.e., V_{AB}, V_{CD}, and $V_a + V_b$, are shown in Fig.5.

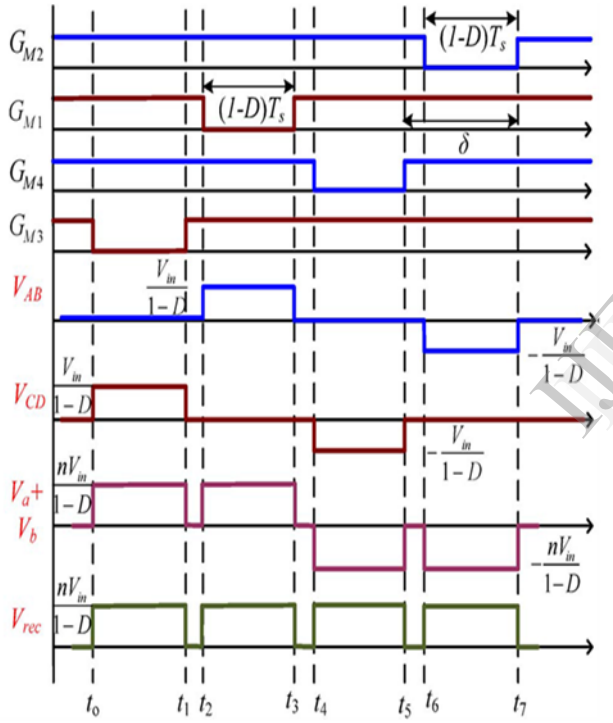

Fig.5: Waveforms showing gating signals for M_1–M_4 and voltages V_{AB}, V_{CD}, V_a+V_b, and V_{rec}.[D=d].

The rectifier is followed by a low-pass filter, which absorbs HF switching components, correspondingly resulting in average voltage V_{dc} across capacitor C_{dc}.

For $\alpha = (1-d)T_S$, an illustration has been carried out at different instances of angle ωt in [13].

From several cases discussed in [13] for different time delays, it can be observed that the voltage at the output of the filter linearly varies between the time delay of $T_S/2-(1-d)T_S$ and $T_S/2+(1-d)T_S$. Fig.6 shows the phase difference between V_a and V_b varying as a function of sine over a line frequency cycle. Effective voltage at the rectifier output is also shown. PWM unipolar voltage is obtained by phase-shift operation of two converter cells.

Voltage waveform V_{dc} is obtained as a function of δ given by

$$V_{dc} = \left|\left(\delta - \frac{T_S}{2}\right)\frac{4nV_{in}}{(1-d)T_S}\right| = \left|\frac{4nV_{in}.\alpha.\sin(\omega t)}{(1-d)T_S}\right| \quad (4)$$

Rectified sinusoidal voltage is achieved at the filter output for a time delay given by Eq.1 as explained. Single-phase sinusoidal voltage is obtained by switching S_1 to S_4 using line frequency square-wave control. During one cycle of the rectified voltage, switches S_1 and S_4 are turned ON. S_2 and S_3 are turned ON for the following cycle, as shown in Fig.7.

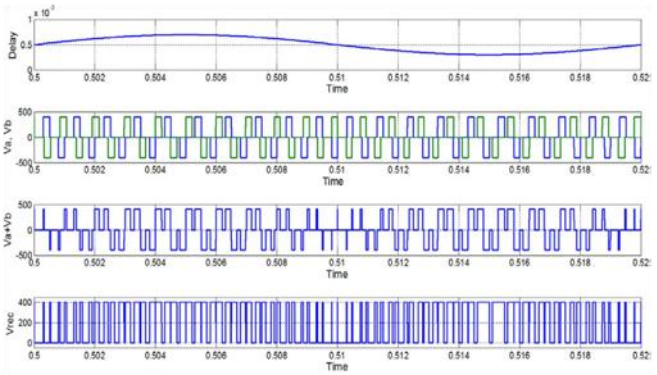

Fig.6: Waveforms of the converter for complete one cycle[13].

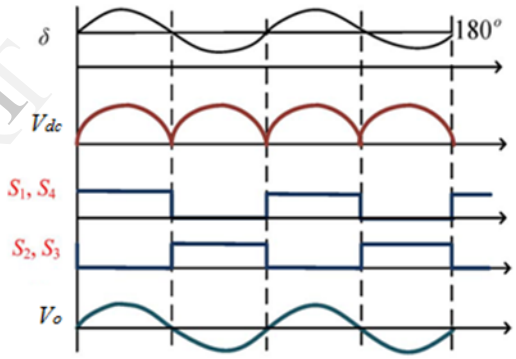

Fig.7: Waveforms showing operation of the unfolding inverter circuit[13].

Two parameters can be adjusted to regulate the output voltage and power, i.e., duty ratio d of the front-end converters and maximum delay α between the gating signals of two front-end converter cells. Duty ratio d can be varied within 0.5–0.8 if input voltage V_{in} varies. Output power can be controlled by varying α for a given value of d at the same value V_{in}. At variation in input voltage V_{in}, the voltage across the primary devices gets affected. The voltage across the switch is given by $V_{in}/(1-d)$. Therefore, with an increase in V_{in}, d is reduced to keep the voltage across the devices below maximum value. However, variation in d does not affect the maximum output voltage of the inverter, which remains independent of d given by $4nV_{in}$.

III. Design Of The Proposed Topology

In this section, the design procedure is illustrated by a design example for the following converter system specifications:

- ✓ input voltage V_{in} = 25V,
- ✓ peak output power P_o = 50 W,
- ✓ voltage at dc link V_{dc} = 230 V,

- ✓ output RMS voltage V_o = 162.63 V at f_o = 50 Hz,
- ✓ switching frequency of dc/dc converter f_s = 40 kHz,
- ✓ Switching frequency of unfolding inverter, f_{Si} = 50 Hz.

The duty ratio *d*, of dc/dc converters has to be maintained always above 0.5 to provide a current path to pass or circulate the input boost inductor currents, i.e., both the primary switches cannot be turned off at a time.

Duty ratio *d* is selected as 0.75, so that output voltage can be regulated even during variation in input voltage. Here, the secondary duty ratio d_r is set to 0.05.

1. Average input current: Average input current is $I_{in} = P_o/(\eta V_{in})$. Assuming ideal efficiency η of 100%, I_{in} = 2 A. Input current in each converter is half of this current since they are sharing equal current.

2. Boost inductors: The value of the boost inductors are given by

$$L_1 = L_2 = L_3 = L_4 = (V_{in} . d)/(\Delta I_{in} . f_S) \quad (5)$$

where ΔI_{in} is the boost inductor ripple current.

For ΔI_{in} = 0.2 A, $L_1 = L_2 = L_3 = L_4$ = 2.344 mH. Each boost inductor has average current rating of $I_{in}/4$ (= 0.5 A).

The maximum voltage across the inductors is equal to *Vdc/2n − V*in.

3. Maximum voltage across the primary switches is

$$V_{sw,pri} = V_{Ls} + (V_{dc} /2n) \quad (6)$$

The cost of the device increases with the voltage rating.

4. Peak current through the primary switch is $I_{in}/2$ and rated for voltage of $V_{dc}/2n$.

5. Input and output voltages of the converter are related as

$$V_{dc} = (2 . n . V_{in})/(1-d) \quad (7)$$

For *d* = 0.75, the proposed converter can boost up to four times.

6. High-frequency transformer design: Based on the primary and secondary winding currents, gauge of windings is chosen, and winding resistances are calculated.

For the given design specifications, turns ratio of HFT from Eq.7, is *n*= 1.15.

Peak value of the transformer primary current is

$$I_{Ls,peak} = (V_{dc} . d_r)/(2 . n . f_S . L_S) \quad (8)$$

7. Leakage inductance of the transformer or series inductance L_S is calculated using

$$L_{S1} = L_{S2} = (2 . V_{dc} . d_r)/(n . I_{in} . f_S) \quad (9)$$

For the given specifications, $L_{S1} = L_{S2}$ = 250µF.

The calculated value of $I_{Ls,peak}$ = 0.5 A.

8. Secondary switches: The peak current through the secondary switches is

$$I_{sw,sec,peak} = I_{in} / (4n) \quad (10)$$

The calculated value is $I_{S3,peak}$ = 0.435 A.

The maximum voltage across the secondary switches is equal to half of the dc link voltage V_{dc}.

9. DC link capacitor: Value of dc link capacitor C_{dc} is

$$C_{dc} = I_{in} . (d-0.5) / (4 . n . \Delta V_{dc} . f_S) \quad (11)$$

Where, ΔV_{dc} = allowable ripple in dc link voltage, and C_{dc} = 5.435 μF for ΔV_{dc} = 0.5 V. Its voltage rating is equal to V_{dc} = 230 V. Choose, C_{dc} = 5.435 μF / 20 = 0.271 μF.

10. *LC* Filter: Filter inductor is calculated, assuming voltage drop across it is less than 2% of the nominal voltage. Thus,

$$L_f = (V_{o,rms}. 0.02)/(2\pi. f_0. I_0) \quad (12)$$

where f_0 and I_0 are the output frequency and output current, respectively. The value L_f is obtained as 23.81mH (choose 22mH or 24mH). The filter capacitor is decided according to the cut-off frequency of the low-pass filter. For this application, one-tenth of converter switching frequency f_S is selected as the cut-off frequency. Capacitor is calculated as

$$C_f = 1/(4\pi^2 . f_c^2 . L_f) \quad (13)$$

where f_C is the cut-off frequency of the filter. For f_C = 4 kHz, capacitor C_f is obtained as 66.48 nF (choose 68nF).

11. Unfolding circuit: Voltage rating of the switches is selected based on the maximum voltage across C_{dc}, which is equal to peak value of maximum output voltage. RMS current rating of the switches are calculated as

$$I_{sw,inv,rms} = I_0 /\sqrt{2} = I_{in} / (4n\sqrt{2}) \quad (14)$$

Switches have to be rated for dc-link voltage (230V) and the current rating is 0.62A.

IV. Simulation Results

Fig.8 shows a PSIM model of proposed interleaved current-fed phase-modulated single-phase unfolding inverter.

Fig.9 shows the gating signals for primary switches, secondary switches.

Fig.10-15 shows the currents through various components of the circuit.

Fig.16-18 shows the voltage across various components of the circuit.

Fig.19&20 shows the result of FFT analysis of the voltage across the load and the current through the load.

From simulation results/waveforms, the efficiency and harmonics of the proposed converter is tabulated as follows;

TABLE I. EFFICIENCY

Circuit	Input power (Watts)	Output power (Watts)	Losses (Watts)	% η
Interleaved DC/DC converter	47.8035	45.9274	1.8761	96.075
Unfolding inverter	44.4553	44.45	0.0053	99.988
Proposed topology (overall)	47.8035	44.4378	3.3657	92.959

Note: η = Efficiency = Output power/Input power
Losses = Input power - Output power

TABLE II. HARMONICS

Parameter	Fundamental (50Hz)	THD (%)
Output Voltage (V_o)	225.7 V	6.57
Output Current (I_o)	0.3761 A	6.57

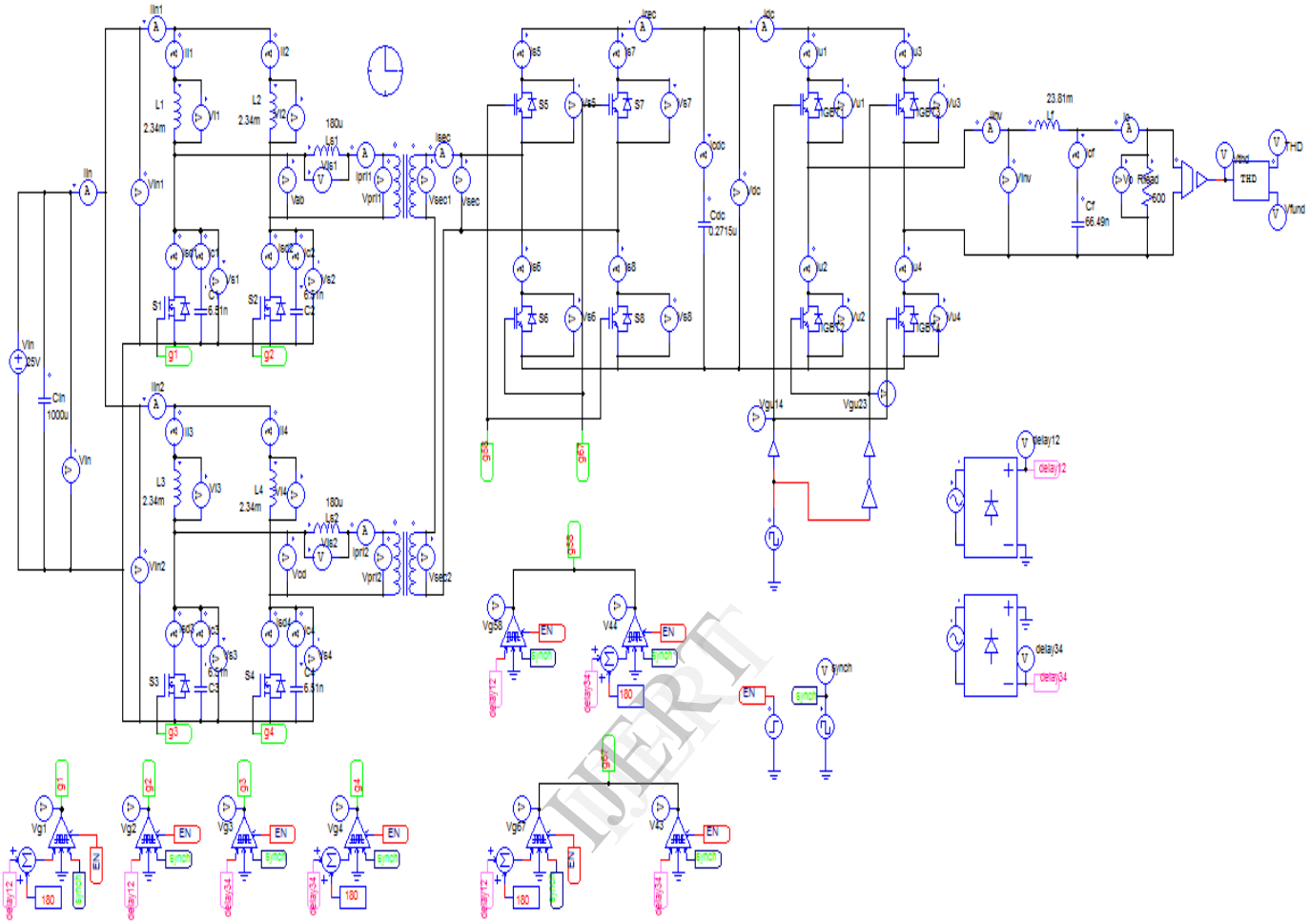

Fig.8: Proposed phase-shift operated interleaved snubberless CFHB dc/dc converter with single-phase unfolding inverter

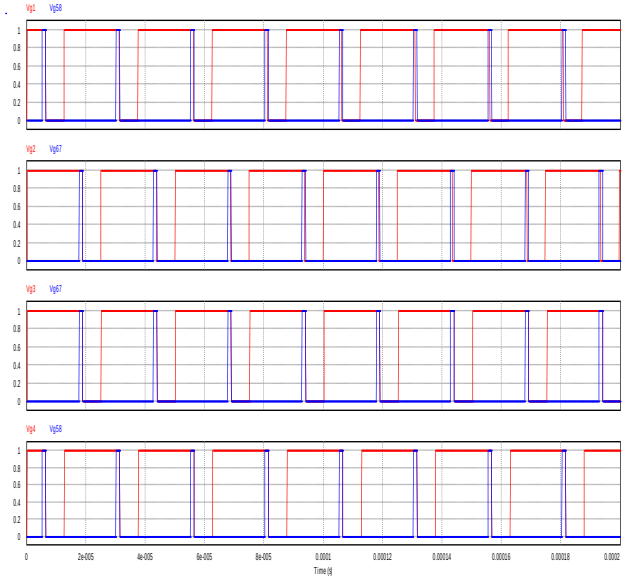

Fig.9: Gating signals for switches S_1 to S_4 (V_{g1}, V_{g2}, V_{g3} & V_{g4}) with gate signals of secondary switches S_5 to S_8 (V_{58} & V_{67}).

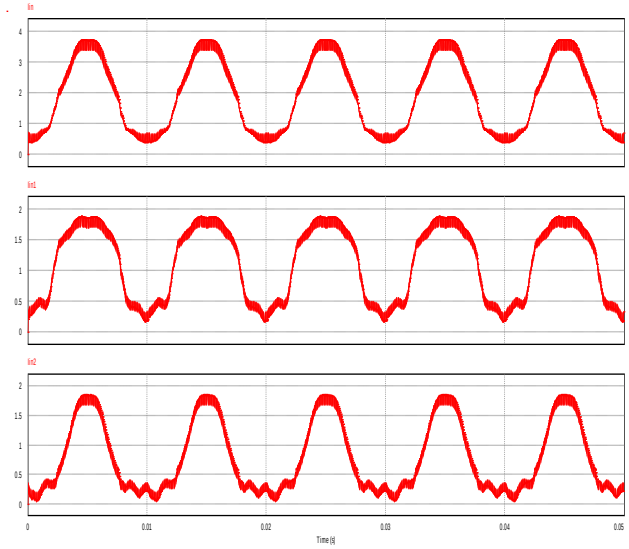

Fig.10: Shows input current to the proposed converter (I_{in}) and input current to the interleaved converter cells (I_{in1} & I_{in2}).

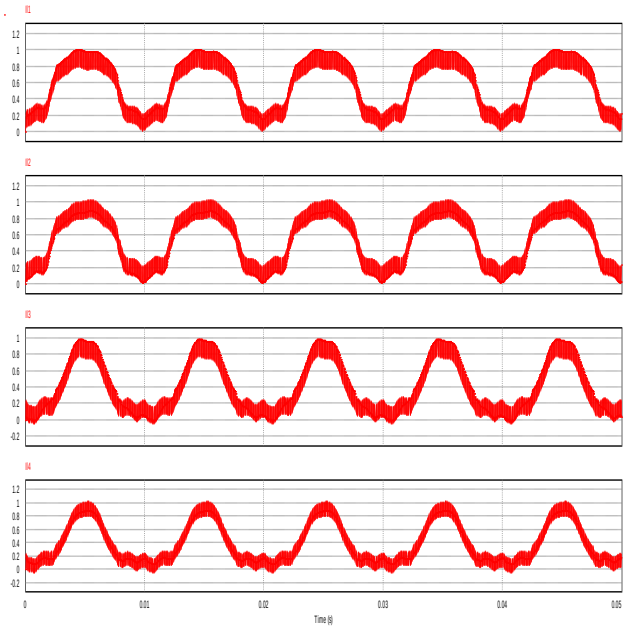

Fig.11: Current through boost inductors L_1 to L_4 (I_{L1}, I_{L2}, I_{L3} & I_{L4}).

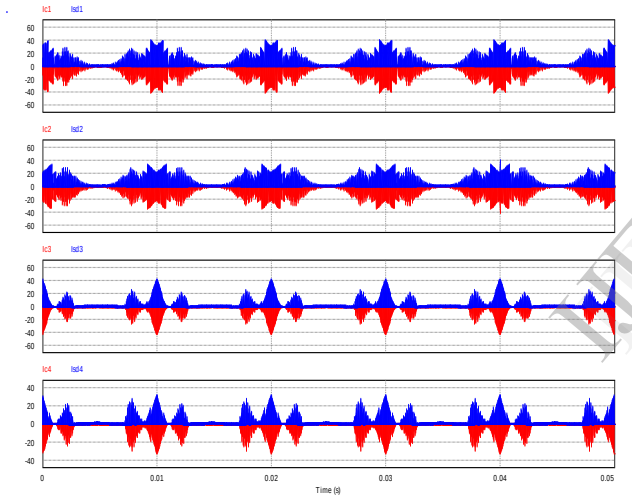

Fig.12: Currents through switches S_1 to S_4 (I_{sd1}, I_{sd2}, I_{sd3} & I_{sd4}) (blue) and currents through capacitor across the switches S_1 to S_4 (I_{c1}, I_{c2}, I_{c3} & I_{c4}) (red).

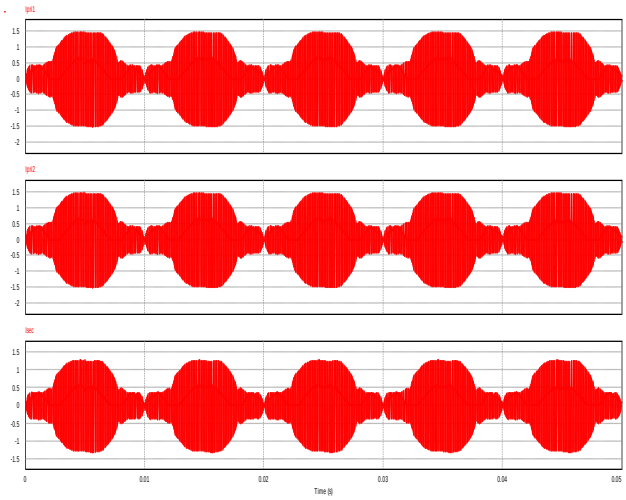

Fig.13: Currents through primary of HFTs (I_{pri1} & I_{pri2}) and currents through the series connected secondary of HFTs (I_{sec}).

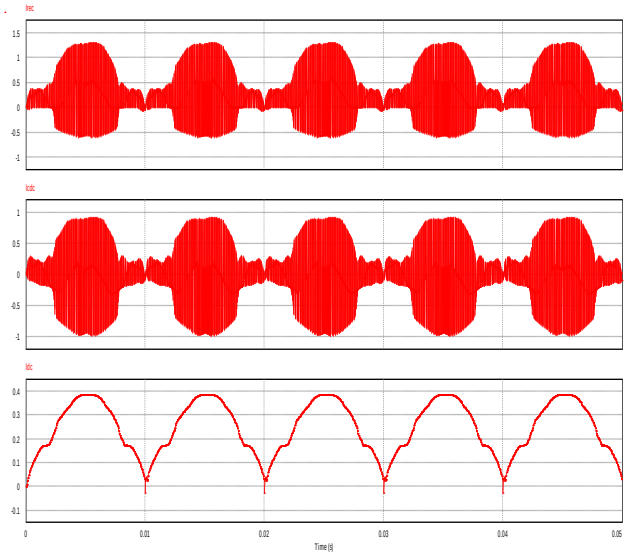

Fig.14: Current output from secondary full bridge (I_{rec}), current through DC-link capacitor (I_{cdc}) and current input to unfolding inverter (I_{dc}).

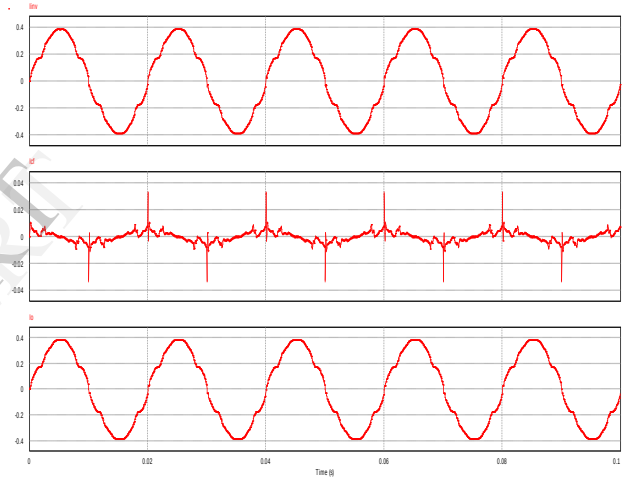

Fig.15: Current output from inverter (I_{inv}), current through the filter capacitor (I_{cf}) and output current through load (I_o).

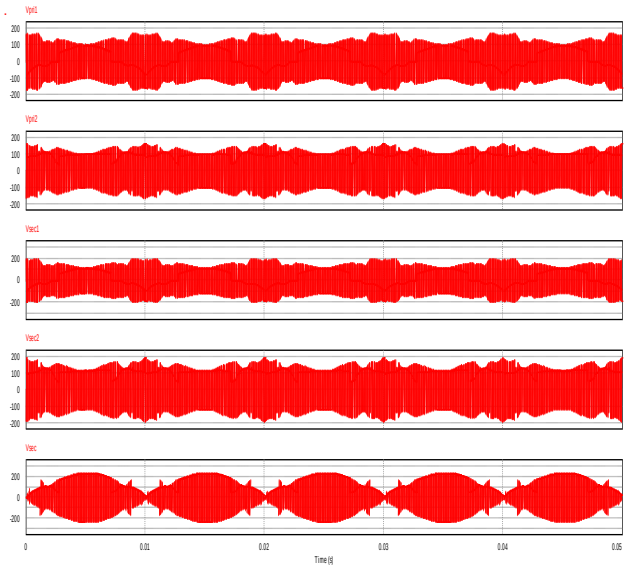

Fig.16: Voltage across primary and secondary of HFTs (V_{pri1}, V_{pri2}, V_{sec1}, V_{sec2} & V_{sec}).

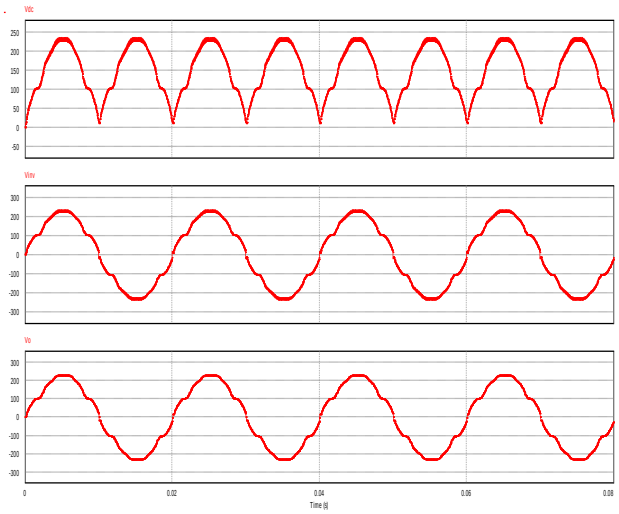

Fig.17: Voltage across DC-link (V_{dc}), unfolding inverter output voltage (V_{inv}) and output voltage across load (V_o).

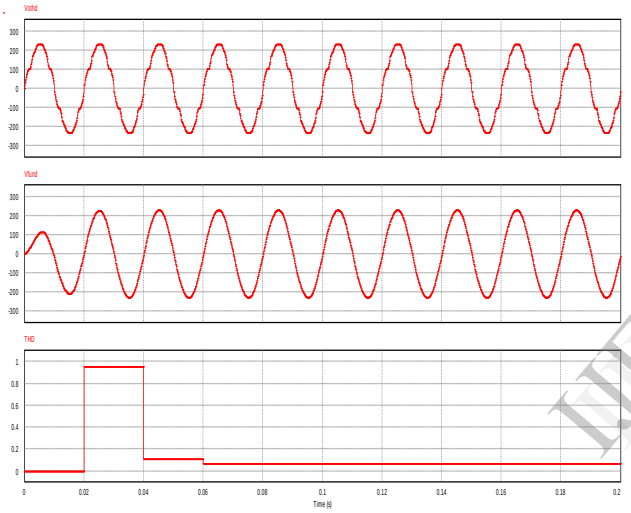

Fig.18: Voltage across load given as input to THD block (V_{othd}), fundamental component (50Hz) of V_{othd} (V_{fund}) and THD in V_{othd}.

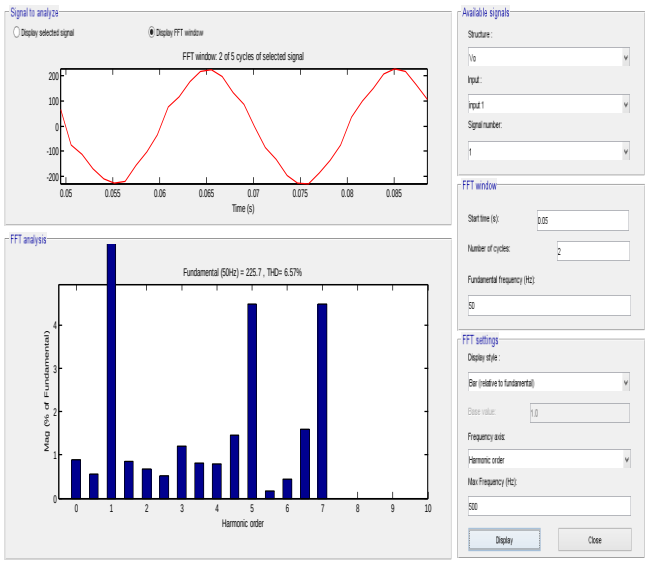

Fig.19: FFT analysis of output voltage V_o.

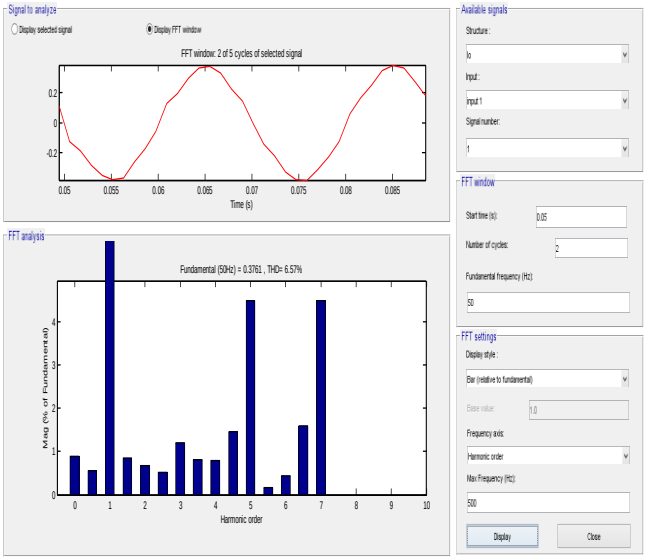

Fig.20: FFT analysis of output current I_o.

From Table I and Table II, it can be seen that the proposed topology has less losses and THD. By fine tuning the filter, THD can be further reduced. As the rating of the converter increases the efficiency increases and THD reduces.

V. SUMMARY AND CONCLUSION

This paper has proposed a novel current-fed interleaved converter that provides a secondary-side-modulation-based solution to the switch turn-off voltage spike problem. It attains clamping of the device voltage by secondary modulation, thus eliminating the need of snubber or active-clamp, making the proposed concept novel and snubberless. This reduces component count and peak current through the primary switches and transformers, has been reduced. Voltage of the primary-side switches is clamped at reflected output voltage. Therefore, a design with selection of reduced voltage rating devices is possible. Low voltage and current rating devices are less costly and result in compact converters. In addition, such devices have low ON-state resistance, resulting in reduced conduction losses, and enhance converter efficiency.

Detailed steady-state operation, analysis and design of the proposed current-fed half-bridge converter have been discussed. Phase modulation of two half-bridge current-fed converters has been proposed to generate rectified sinusoidal voltage at the dc link. This eases the design of the next dc/ac inversion stage to an unfolding circuit operating at the line frequency reducing the switching losses.

For the designed values and specifications, simulation has been carried out using PSIM 9.3.1. Simulation results/waveforms are analyzed and performances are tabulated.

In this paper off-grid system is considered. To make this system as grid connected, MPPT is incorporated between the

PV panel and the proposed converter. MPPT controls the duty cycle of the primary switches of the converter to maintain the input voltage constant. The phase of the grid voltage is taken as the feedback for synchronizing the gate pulses with the grid voltage.

The proposed converter can be commercialised since it is reliable and cost effective. It can be both off-grid and grid tied. Hence it is suitable for both small scale and large scale applications.

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