Simulation Model Of Wallace Tree Multiplier Using Verilog

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Abstract- This paper is about Desiging of Wallace tree Multiplier using Verilog. Now a Days Power consumption has become a very important issue in VLSI design. As multiplication is one of the most basic arithmetic operations. It is used in digital applications, central processing units, and digital signal processors. In most systems, the multiplier lies within the critical path and hence, due to probability and reliability issues, the power consumption of the multiplier has become very important. The main Foucus of this paper is to describe the 4*4 wallace Multipier using Verilog.

Keyword:- Wallace tree, Multiplier,Verilog,Model Sim, Simulation

1. Introduction

The basic building blocks of arithmetic circuits in digital signal processing systems are registers,multiplier and adders.Among of these , the multipliers are the most area, time, and power consuming components. Since Non-regularities in the construction of traditional multipliers result in a large amount of wasted area. There have been many researches in the past and in present for high Speed Optimized Multipliers. The basic building blocks of arithmetic circuits in digital signal processing systems are registers,multiplier and adders.Among of these , the multipliers are the most area, time, and power consuming components. There have been many researches in the past and in present for high Speed Optimized Multipliers. In a Simple term ,A Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers. Since Non-regularities in the construction of traditional multipliers result in a large amount of wasted area.

2. Working

The main aim of our research area first to describe the Functionality of the desired wallace tree using Verilog HDL. The multiplier takes in two 4-bit operands: the multiplier (MR) and the multiplicand (MD), and produces the 8-bit multiplication result of the two at its output . The Desired architecture of the multiplier primarily consists of four major modules. They are: 2's Complement Generator, Partial Product Generator, Wallace Tree and Carry Look-ahead Adder. The multiplier has been constructed in its simplest conceptual form. The 2's Complement Generator uses a Ripple Carry Adder constructed from Full-adder modules. The Partial Product Generator uses MD or –MD and MR or –MR for creating 4 partial products of 8 bit. The 4partial products are supplied to Wallace Tree and added appropriately.

The Wallace tree uses both Full Adder and Half Adders. The final 8-bit intermediate results are added using a Carry Look-ahead Adder.

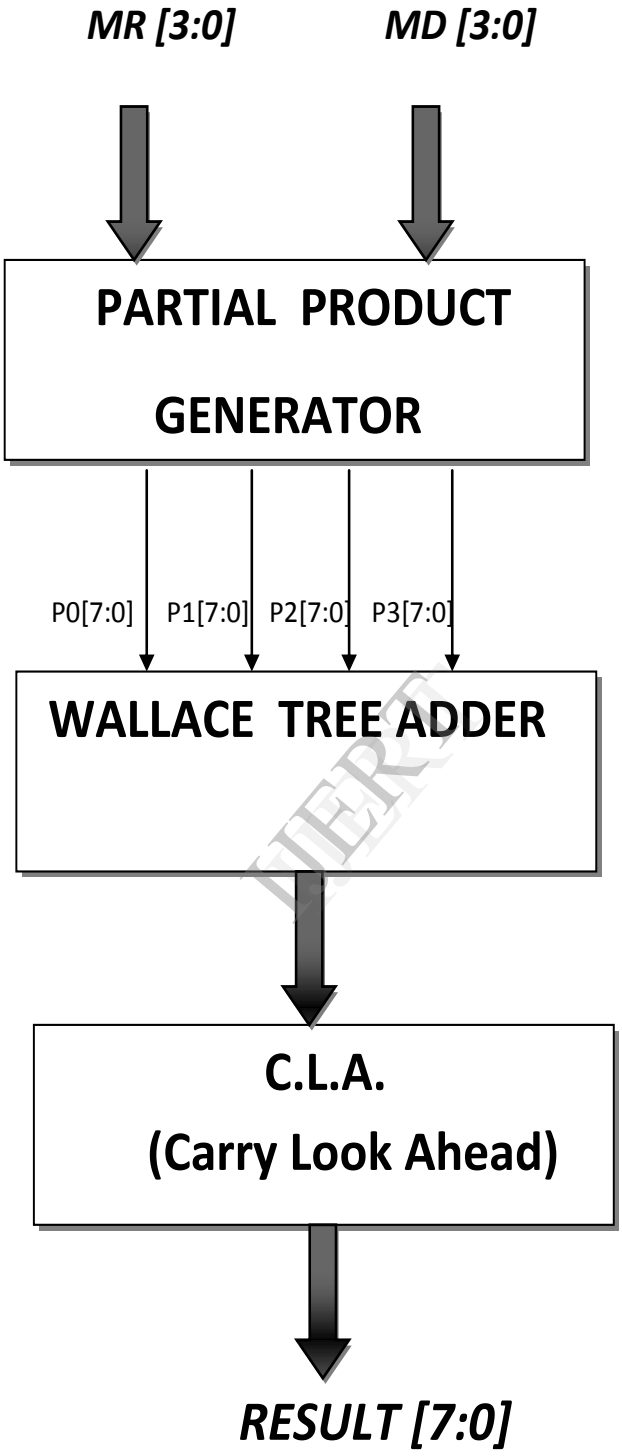

Figure1. Flow diagram for the Wallace tree multiplier

2.1 Function and Algorithm of the Modules

a) **2's Complement Generator:**

Function*:* The 2's Complement Generator Takes the multiplicand MD and MR as its input and produces –MD and - MR as its output in case of negative numbers.

Algorithm*:* 2's complement is generated by inverting all bits of the multiplicand and then adding 1 using a ripple carry adder.

b) **Partial Product Generator:**

Function*:* The Partial Product Generator generates appropriate partial products to be added with a Wallace tree.

Algorithm: The Partial Product Generator uses the table for each multiplier bit. Depending on the value of MD or -MD or MR or-MR is assigned to partial product . 4 bit is then extended till the 7th bit for appropriate sign extension.

c) **Wallace Tree:**

Function*:* The Wallace tree module adds the 4 partial products and generates final two intermediate operands for final addition

Algorithm:

$$
\begin{array}{r}
x_3\ x_2\ x_1\ x_0 \\
*\ y_3\ y_2\ y_1\ y_0 \\
\hline
P_{07}\ P_{06}\ P_{05}\ P_{04}\ P_{03}\ P_{02}\ P_{01}\ P_{00} \\
P_{16}\ P_{15}\ P_{14}\ P_{13}\ P_{12}\ P_{11}\ P_{10} \\
P_{25}\ P_{24}\ P_{23}\ P_{22}\ P_{21}\ P_{20} \\
P_{34}\ P_{33}\ P_{32}\ P_{31}\ P_{30} \\
\hline
z_7\ z_6\ z_5\ z_4\ z_3\ z_2\ z_1\ z_0
\end{array}
$$

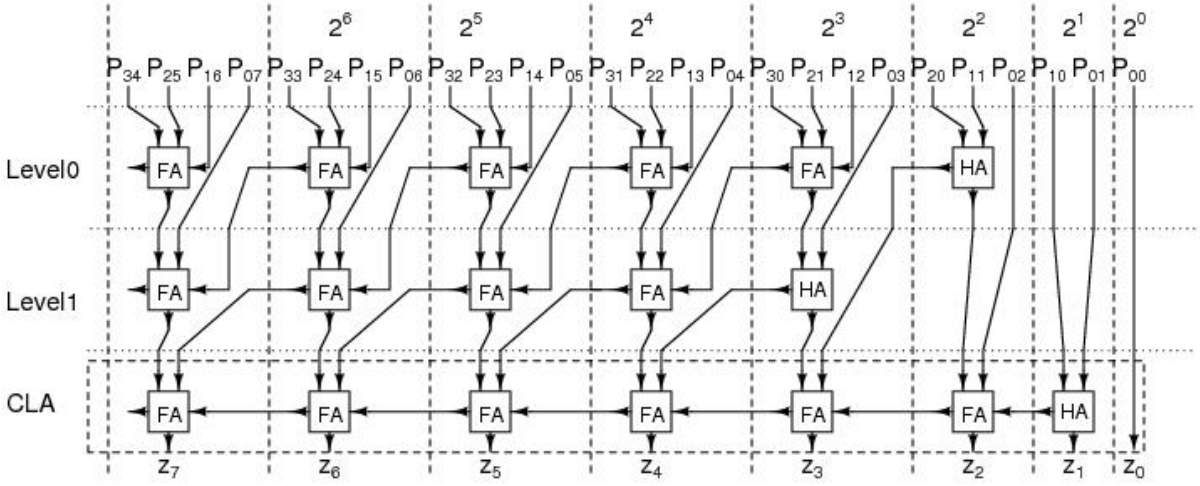

Figure2. Wallace tree Multiplier tree structure

d) **Carry Look-ahead Adder:**

Function*:* Carry Look-ahead Adder (CLA) add two numbers with very lower latency.

Algorithm*:* By extend the cin with the corresponding inputs, the carry and sum are independent of the previous bits.

3. Result

For acheving the Simulation model of Desired Wallace tree Multiplier Verilog HDL was used for the description. The Four module files were written in a verilog and then they instatiated in a main module. For a functional verification purpose test bench was also wriiten in verilog hdl. The test Bench generates two four bit inputs(Mr and Md) and shows the responce in 8 bit output waveform. Different input combinations were generated a test bench like two postive input numbers, one negative and one postive input number, two negative input numbers. For Simulation “Model Sim 6.5C” tool was used.

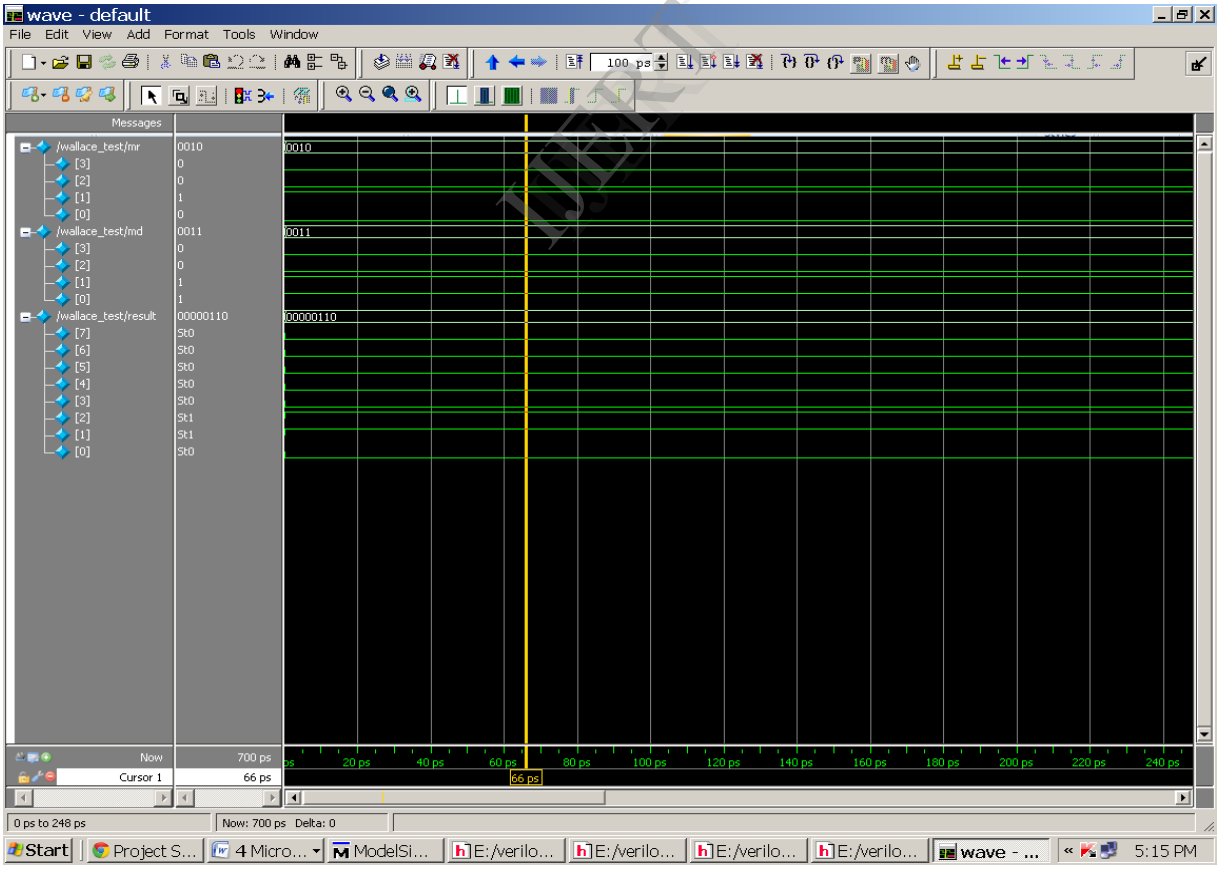

Figure3. Simuation result for Mr=2 and Md=3

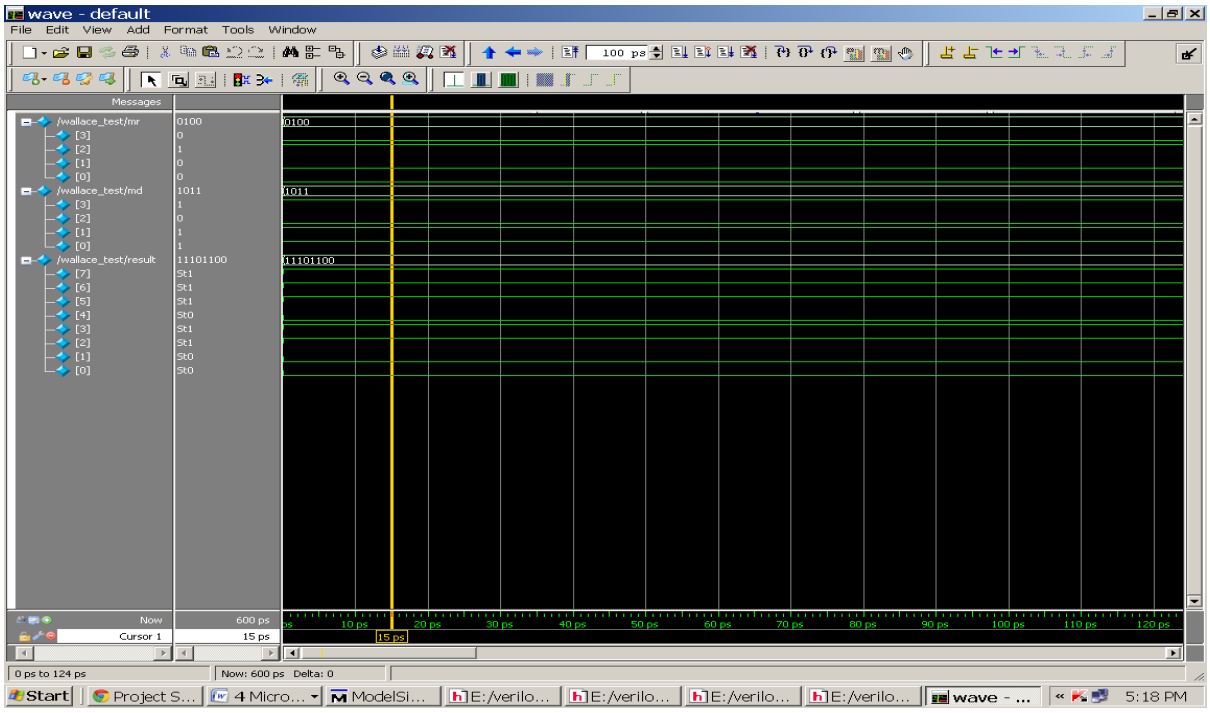

Figure4. Simulation Model for Mr=4 nad Md=-5

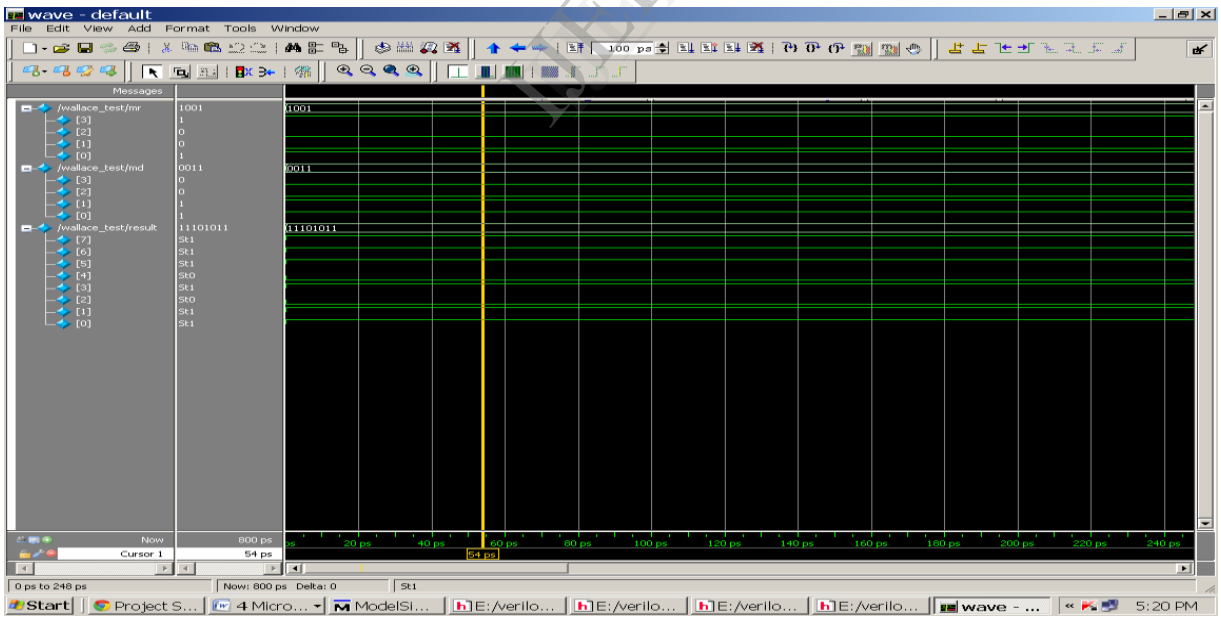

Figure5. Simulation Model for Mr=-7 and Md= 3

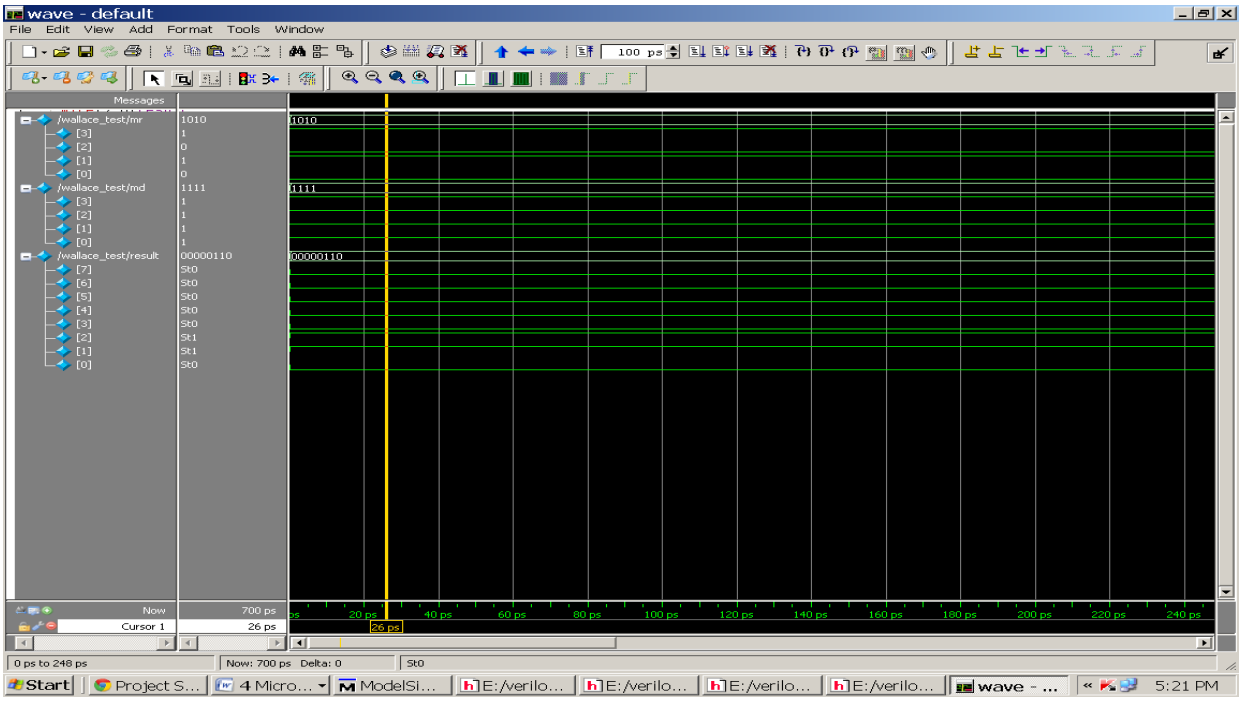

Figure6. Simulation Model for Mr=-6 and Md= -1

4. Conclusion and future work

The 4X4 wallace tree multiplier is sucessfully written in verilog and simulated in Model sim 6.5c. The simulation model is verified for all the conditions like when two numbers are positive , one number is negative and another is positive and both the numbers are negative. The future work is to Syntheszied the code and implementaion in FPGA.

5. REFERENCES

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Biographies

Ravi Payal received his BE degree from Dehradun institute of Technolgy (DIT) Dehradun in 2002 and MS in VLSI-CAD from Manipal University in 2013. Currently working at CDAC, Noida as a Senior Lecturer in School of Electronics.Teaching and Research area include VSLI.