International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 3 Issue 5, May - 2014

Simulation Methodology for 2D Mesh Memory-Router Architecture

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***Abstract*— As complexity in 2D Mesh Memory-Router architecture increases, energy consumption also increases which results in execution time delay which in turn leads to maximum latency and minimum throughput. Simulation methodology for Memory-Router helps to identify the unused cache block word that leads to reduce the dynamic energy consumption in the Network on Chip channels and routers and also minimizes the miss rates for the cache memory. Hence the communication between the nodes can be made faster due to which energy consumption in the memory elements within a chip as well as the router channels can be reduced by which better performance can be achieved.**

***Keywords*— Cache, NUCA, Singlecore, Router, Modelsim and Xilinx.**

I. INTRODUCTION

While process technology scaling continues providing more transistors, the transistor performance and power gains that is a part of the process scaling have largely ceased. Memory-Router designs achieve greater efficiency than traditional monolithic processors through concurrent parallel execution of multiple programs or threads. As the Core count in CMP systems increases, networks-on-chip (NoCs) present a scalable alternative to traditional, as in most current VLSI designs, power efficiency has also become a first-order constraint in NoC design. The energy consumed by the NoC itself is 28% of the per-tile power in the Intel Teraflop chip and 36% of the total chip power in MIT RAW chip. Use of spatial locality speculation to identify unused cache block words. It is easy to predict which words in each cache block fetch will be used and leverage that prediction to reduce dynamic energy consumption in the NoC channels and routers through reduced switching activity.

II. BLOCK DIAGRAM

2D Mesh CMP architecture includes 16 processors (4x4), each processor is taken in to consideration having a single core, L1 cache, L2 cache, Non Uniform Cache Architectuer (NUCA), Location cache and a router (Switch allocator and virtual channel) for communication between the nodes in an architecture to perform the operations like request in, physical address verification and then validation to know the cache miss rate/hit rate.

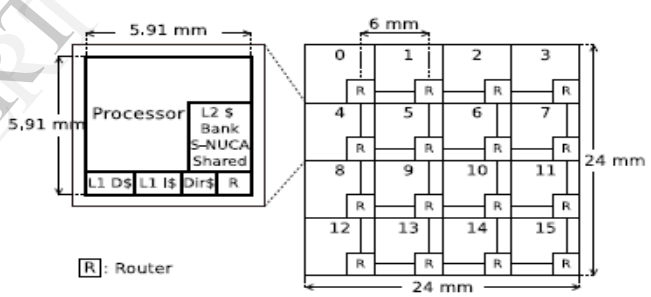

Fig. 1. Block diagram of 2D Mesh CMP

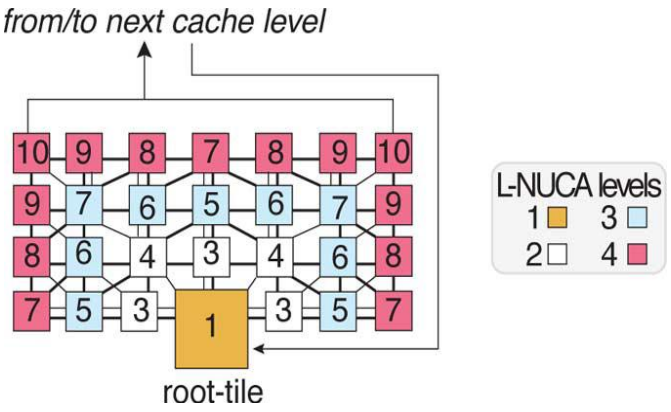

Fig. 2. Structure of NUCA

Use of NUCA results better performance and it is energy efficient. Here the communication starts from root-tile 1 and it can select any path to send the information to the destination hence the name non uniform cache architecture (NUCA). Here path selection in all possible ways, in this structure it is having 4 ways (way 0 –way 3), in coding and simulation only 3 ways are considered to transfer the data from root-tile to any destination.

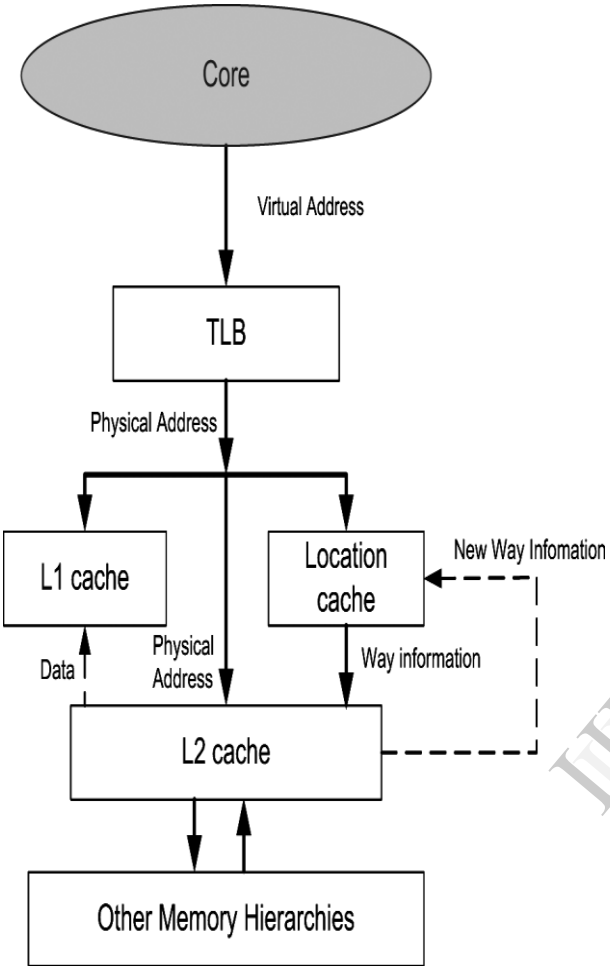

Fig. 3. Structure of Single core

The physical address generated by a core is verified by the L1 cache and then validation and transferred to next level. Translation Look aside Buffer (TLB) is a cache and it is a part of Memory Management Unit (MMU), use of TLB improves the translation speed of virtual address. The location cache is used to store the information related to L1 when it is busy and again reloaded into L1 when it will become free, so the location cache is for temporary storage

III. SIMULATION RESULTS

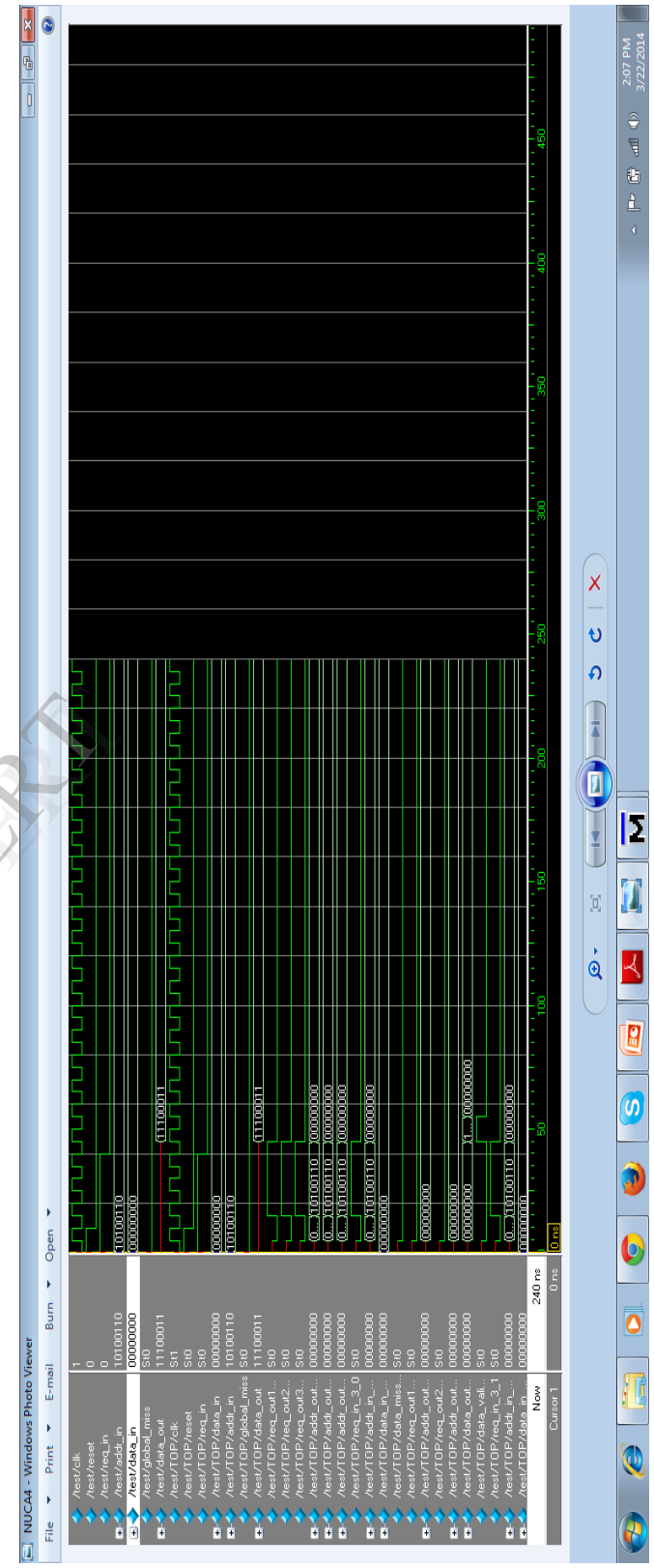

Fig. 4.Simulation result for NUCA

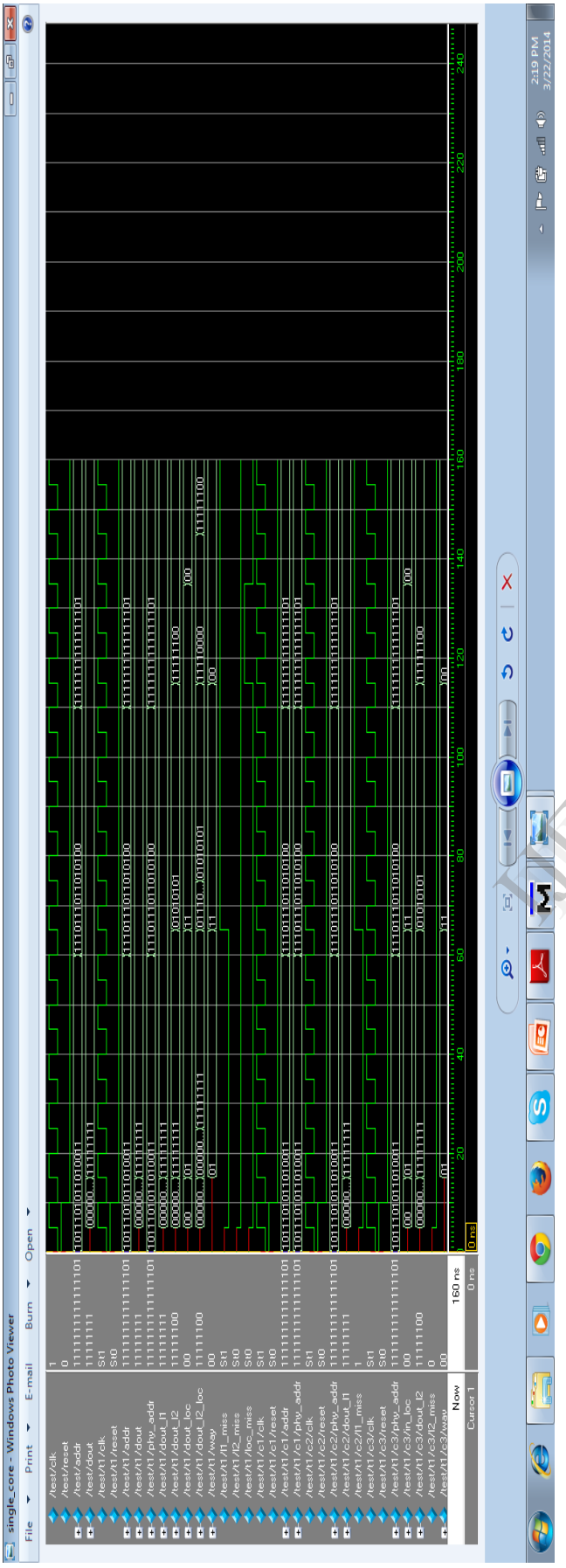

Fig. 5. Simulation result for Single core

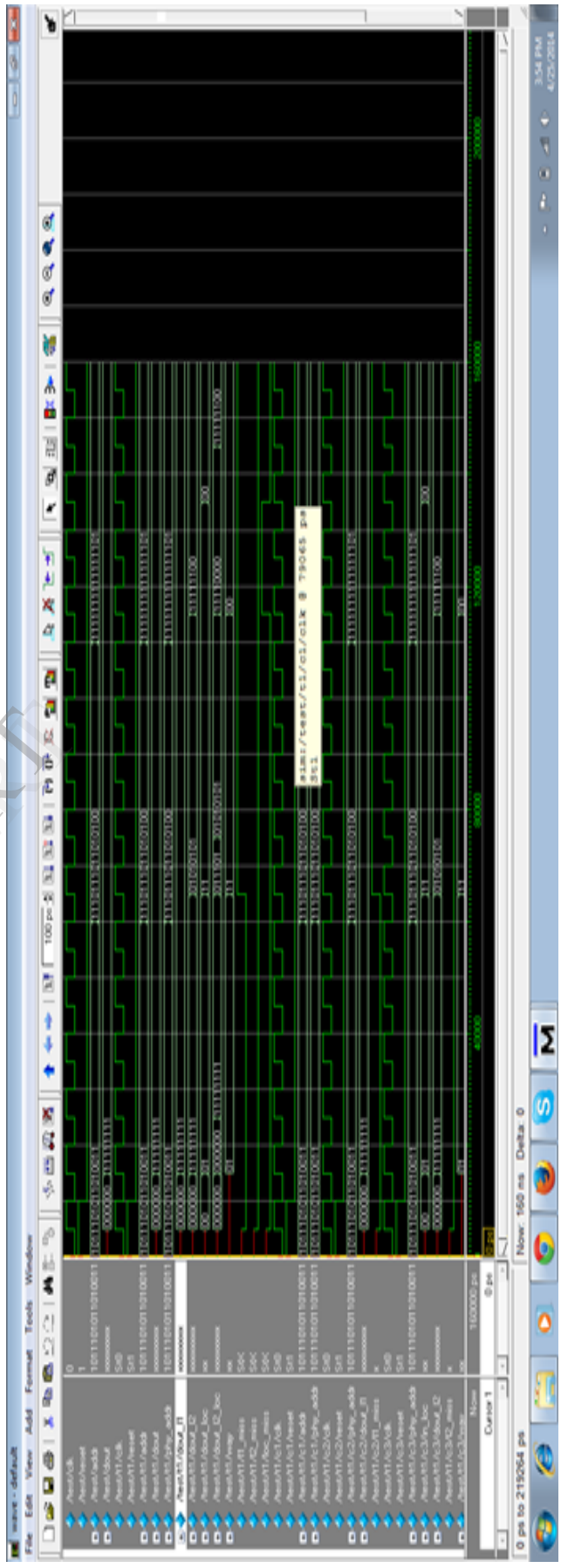

Fig. 6. Simulation result for Router

IV. CONCLUSION

This project introduces a simple and powerful mechanism to identify unused cache block words and can be utilize and hence easy to communicate the nodes and interconnection between processor cores to achieve an average of 20% reduction in the dynamic energy of the network with better performance

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