# Simulation & Implementation of ADC Using V to F Converter on FPGA


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**ABSTRACT**

*This paper proposes the Simulation and Implementation of ADC Using V to F converter on FPGA. An ADC can resolve a signal to only a certain number of bits of resolution called "Effective number of Bits "(ENOB).The VHDL code is present in this projects will enable you to see how to create simulation results of a particular accuracy. The example we present is for 8bit ADC, but we can easily modify the digital output word length for any desired accuracy of ADC.The 8bit ADC model is built around a function, ADC_8bit_5V_Unipolar.*



**Key words— Simulation on modelsim and Implementation on FPGA.**


### 1. INTRODUCTION

It was in the early 1980s that many experts predicted the demise of analog circuits. Digital signal processing algorithms were becoming increasingly more powerful while advances in integrated circuits (IC) technology provided compact, efficient implementation of these algorithms in silicon.

Why are analog designers in such great today? After all digital signal processing and IC technology have advanced tremendously since the early 1980s, making it possible to realize processor containing millions of transistor and performing billions of operations per second.

### 2. PROCESSING OF NATURAL SIGNAL

Naturally occurring signal are analog at least at a microscopic level. A high-quality microscopic picking up the sound of an orchestra generates a voltage whose amplitude may very from a few micro volts to hundred
of milli volts. The photocell in a video camera produces
a current that is as low as a few electrons per microsecond. A seismographic sensor has an output voltage ranging from a few micro volts for very small vibration of the earth to hundreds of milli volts foe heavy earth quick. Since all of these signals must evaluate undergo extensive processing in the digital domain, we observe that each of these system consists of an Analog to digital converter (ADC) and a Digital signal processing (DSP) {Fig 1.1a}. The design of ADC for high speed, high precision, and low power dissipation is one of many difficult challenges in analog design.

In practice, the electrical version of natural signal may be prohibited small for direct digitization by the ADC. The signals are also often accompanied by unwanted out-of-band interferers. The front end of figure 1.1a may there for modified as shown in fig 1.1b.where an amplifier boosts the signal level and an analog filter suppresses the out-of-band components. The design of high performance amplifier and filters is also a topic of active research today.

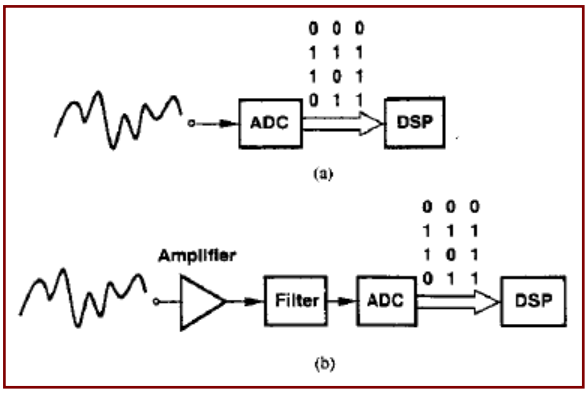



Figure. 1.1a

**3. ANALOG INTEGRATED CIRCUIT DESIGN**

Integrated-circuit design is separated into two major categories: analog and digital. To characterize these two design methods we must first define analog and digital signals. A *signal* will be considered to be any detectable value of voltage, current, or charge. A signal should convey information about the state or behavior of a physical system. An *analog signal* is a signal that is defined over a continuous range of time and a continuous range of amplitudes. An analog signal is illustrated in Fig. 1.1-1(a). A *digital signal* is a signal that is defined only at discrete values of amplitude, or said another way, a digital signal is quantized

to discrete values. Typically, the digital signal is a binary-weighted sum of signals having
only two defined values of amplitude as illustrated in Fig. 1.1-1(b) and shown in Eq. (1).
Figure 1.1-1(b) is a 3-bit representation of the analog signal shown in Fig. 1.1-1(a).

$$D = b_0 2^{-1} + b_1 2^{-2} + b_2 2^{-3} + \ldots + b_{N-1} 2^{-(N-1)} = \sum_{i=0}^{N-1} b_i 2^{-i} \qquad (1)$$

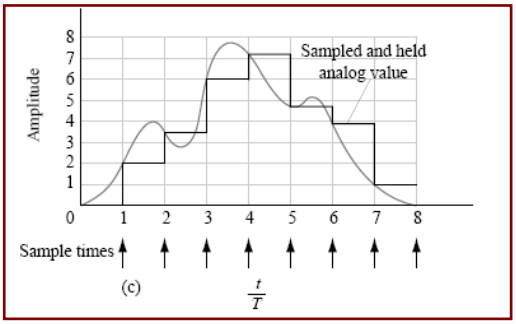



**Figure 1.1-1**

Signals. (a) Analog or continuous time. (b) Digital. (c) Analog sampled data or discrete time. T is the period of the digital or sampled signals.

The individual binary numbers, *bi*, have a value of either zero or one. Consequently, it is possible to implement digital circuits using components that operate with only two stable states. This leads to a great deal of regularity and to an algebra that can be used to describe the

function of the circuit. As a result, digital circuit designers have been able to adapt readily to the design of more complex integrated circuits.

Another type of signal encountered in analog integrated-circuit design is an analog *sampled-data* signal. An analog sampled-data signal is a signal that is defined over a continuous range of amplitudes but only at discrete points in time. Often the sampled analog signal is held at the value present at the end of the sample period, resulting in a sampled-and-held signal. An analog sampled-and-held signal is illustrated in Fig. 1.1-1(c).

**4. HIGH SPEED SAMPLING ADCS**

- Wide Acceptance in Signal Processing and Communications.
- Emphasis on Dynamic Performance.
- Trend to Low Power, Low Voltage, Single-Supply.
- More On-Chip Functionality: PGAs, SHA, Digital Filters, etc.
- Process Technology:
    - Low Cost CMOS: Up to 12-bits @ 10MSPS.
    - High Speed Complementary Bipolar: Up to 12-bits @ 70MSPS.
    - Statistical Matching Techniques Rather than Thin Film Laser Trimming.

## 5. VOLTAGE TO FREQUENCY CONVERTER

### INTRODUCTION

A voltage-to-frequency converter (VFC) is an oscillator whose frequency is linearly proportional to a control voltage. The VFC/counter ADC is monotonic and free of missing codes, integrates noise, and can consume very little power. It is also cheap and low-powered can be mounted on the experimental subject (patient, wild animal, artillery shell, etc.) and communicate with the counter by a telemetry link as shown in Figure 1.  very useful for telemetry applications, since the VFC, which is small,

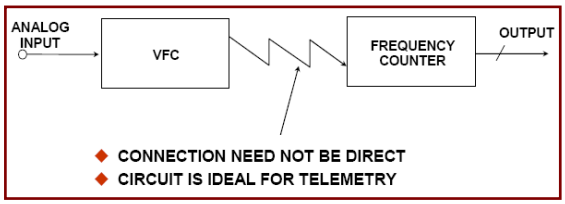



*Figure 1: Voltage-to-Frequency Converter (VFC) and Frequency Counter Make a Low-Cost, Versatile, High-Resolution ADC*

There are two common VFC architectures: the *current-steering multivibrator VFC* and the *charge-balance VFC* (Reference 1). The charge-balanced VFC may be made in *asynchronous* or *synchronous* (clocked) forms. There are many more VFO (variable frequency oscillator) architectures, including the ubiquitous 555 timer, but the key feature of VFCs is linearity—few VFOs are very linear.

The current-steering multivibrator VFC is actually a current-to-frequency converter rather than a VFC, but, as shown in Figure 2, practical circuits invariably contain a voltage-to-current converter at the input. The principle of operation is evident: the current discharges the capacitor until a threshold is reached, and when the capacitor terminals are reversed, the half-

cycle repeats itself. The waveform across the capacitor is a linear triangular wave, but the waveform on either terminal with respect to ground is the more complex waveform shown.

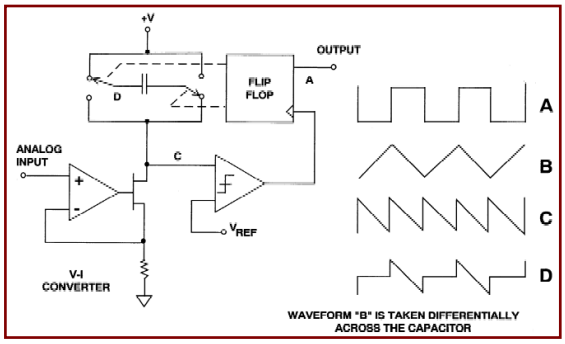
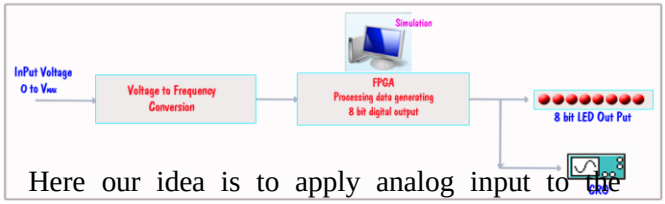



*Figure 2: A Current-Steering VFC*

Practical VFCs of this type have linearities around 14-bits, and comparable stability, although they may be used in ADCs with higher resolutions without missing codes. The performance limits are set by comparator threshold noise, threshold temperature coefficient, and the stability and dielectric absorption (DA) of the capacitor, which is generally a discrete component. The comparator/voltage reference structure shown in the diagram is more of a representation of the function performed than the actual circuit used, which is much more integrated with the switching, and correspondingly harder to analyze.

This type of VFC is simple, inexpensive, and low-powered, and most run from a wide range of supply voltages. They are ideally suited for low cost medium accuracy ADC and data telemetry applications.

## 6. BLOCK DIAGRAM

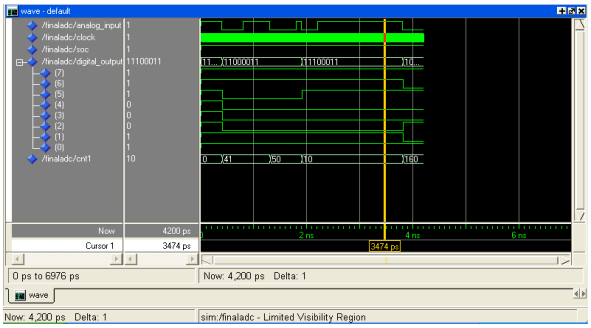



Here our idea is to apply analog input to the "voltage to frequency conversion" block. This block senses the changes in the input voltage and gives output frequency proportional to input voltage.

This frequency output we are applying as input to Spartan II FPGA. Here we have written module which will measure the pulse width and give 8-bit digital output corresponding to input voltage.

Our module can measure up to 4-bit precision.

## 7. SIMULATION RESULT.



## 8. PIN ASSIGNMENT.

Design Object List - I/O Pins

| I/O Name | I/O Direction | Loc | Bank | I/O S |
|---|---|---|---|---|
| soc | Input | p49 | BANK5 | |
| digital_output<7> | Output | p75 | BANK5 | |
| digital_output<6> | Output | p81 | BANK4 | |
| digital_output<5> | Output | p82 | BANK4 | |
| digital_output<4> | Output | p83 | BANK4 | |
| digital_output<3> | Output | p84 | BANK4 | |
| digital_output<2> | Output | p86 | BANK4 | |
| digital_output<1> | Output | p87 | BANK4 | |
| digital_output<0> | Output | p88 | BANK4 | |
| clock | Input | p80 | BANK4 | |
| analog_input | Input | p48 | BANK5 | |



## 9. CONCLUSION

Initially the idea was to implement the project on FPGA using pulse width modulation circuit, but lack of available pulses forced to think over an alternative. Then finally settled on a method to implement the ADC using Voltage to frequency converter. The frequency input from the AFO will be given to Spartan II FPGA kit. Measuring the ON period of a particular frequency as the frequency is varied from AFO. 8-bit digital output is displayed after conversion, based on the ON period of frequency applied. And achieved 4-bit precision.

The present work can be extended to get up to 8-bit precision.

## 10. REFERENCES

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