Simulation 0f Dual Half Bridge DC-DC Converter Fed Drives

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***Abstract* – In this project we are implement a novel ZVS dual half bridge DC-DC converter for servo drives using anfis.so we can give both high power and digitally controlled combines two half-bridge inverters to operate as a full-bridge power stage using phase-shifting control, but with zero circulating current with closed loop function for more efficiency. Each inverter operates at 50% duty cycle and generates a symmetrical and isolated square output voltage and to achieve wide-range Zero Voltage Switching (ZVS) and maximum efficiency. For low output voltage regulation and converter startup, Pulse Width Modulation (PWM) control is used. The topology can also optimally utilize magnetic components and reduces semiconductor stress. The digital controller uses for continues monitoring and controlling of the PWM pulses depend upon the load for minimizing the loss of current and voltage.**

***Index Terms* - Dual half-bridge, full bridge, phase-shifted, zero voltage switching (ZVS).**

I. INTRODUCTION

To extend the soft-switching range and reduce switching loss at light loads, a resonant inductor is usually added to the converter's primary side. The inductor stores extra energy to extend the soft-switching range and reduce the reverse-recovery current of the secondary-side rectifier diodes. However, this extra energy can also cause a higher voltage spike across the rectifier diodes. A simple but effective clamping circuit can be used to mitigate this problem. The clamping circuit substantially minimizes the converter's voltage ringing on both the primary and secondary sides and captures most of the transient energy on the primary side, which is utilized for soft switching and recycled back to the converter's dc input. For low output-voltage applications, such as 48 V or below, synchronous MOSFETs (SyncFETs) are often used to replace secondary rectifier diodes to minimize conduction loss. If the SyncFETs remain active, a converter can maintain continuous conduction mode (CCM) operation and a relatively stable duty cycle. Depending on the load, the converter's output-inductor current can be positive, zero, or negative at the end of a switching cycle. Both positive and negative currents actually help the primary switches to achieve soft switching. At a certain load point, the output inductor current returns to zero at the end of each switching cycle. For this case, the primary can only rely on its magnetizing current for soft switching. Properly sizing magnetizing inductance and keeping Sync FETs active are good ways to achieve ZVS over a wide load range. At a very light load (especially at zero load), however, the negative current may become so significant that too much energy is cycled back to the primary side, resulting in efficiency loss.

A load-dependent circulating current is one of the major drawbacks of the existing ZVS full-bridge dc–dc converters. The circulating current passes through most of the converter's power train during the 1 − D period, while no energy is transmitted from the primary side to the secondary side. This causes a substantial power loss. Some resonant networks have been introduced to eliminate the circulating current. However, the resonant network also removes the necessary circulating energy, which is needed for ZVS. These types of circuits would work well for low-frequency applications where low parasitic capacitance devices, such as insulated-gate bipolar transistors, are often used.

II .DUAL HALF BRIDGE DC–DC CONVERTER

A modified open-loop half-bridge bus converter can have a configuration like that shown in Fig. Its output is a current doubler filter and its power transformer's secondary center tap is connected to power ground. When the primary switches,S_1 and Q_2 , operate complementally at a 50% switching duty cycle, the inverter outputs a symmetrical square voltage waveform. Because the secondary winding of the inverter's transformer is center-tapped, it can be viewed as two interleaved forward-converter outputs connected in parallel but with a 180◦ phase offset between the two outputs. This allows the current doubler filter to fully cancel its output current ripple such that both the power transformer and the output inductors operate in an optimal 50% duty-cycle condition. With transformer design techniques that consider magnetizing inductance and proper dead-time control for the bridge primary switch, the primary switch's parasitic capacitance can be fully discharged by the transformer's leakage inductive energy before the switches are turned ON. With this control, the converter can maintain ZVS over a wide

load range. This open-loop bus converter is one of few topologies that can achieve both high efficiency and power density. If two of such converters are combined to operate like a full-bridge structure and share a single output filter, a new topology concept a dual half-bridge dc–dc converter is created. A detailed dual half-bridge configuration is shown in Fig.

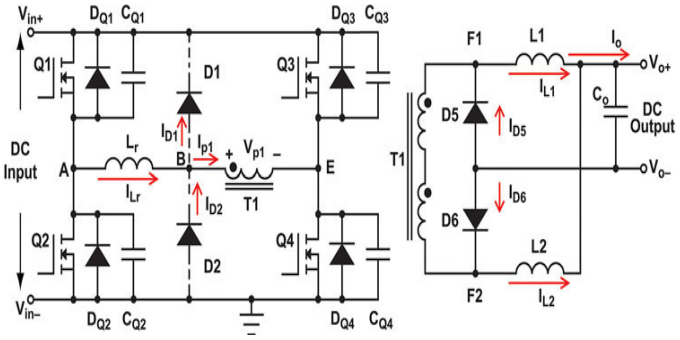

Fig.1. Existing open-loop dual half-bridge bus converter.

The circuit shown in Fig. 4 has two half-bridge inverters; However, under phase-shift control, one provides a leading phase while the other supplies a lagging phase. They are identified as such, where the action of the leading half-bridge initiates each output pulse and the lagging half-bridge terminates it. A resonant inductor L_r and two clamping diodes D_1 and D_2 can be added to the leading inverter to perform the same function as in a conventional phase-shifted full bridge if needed. The inductor stores extra energy to extend the soft-switching range and reduce the reverse-recovery current of the secondary-side rectifier diodes, while the clamping circuit minimizes converter voltage ringing on both the primary and secondary sides of the transformer. The two inverters can vary their phase offset from zero to 180◦ .When the phase offset is 0◦ , the two inverters are in phase and operate in parallel, which works in the exact same way as a modified open-loop bus converter. At this operating point, the converter's duty cycle is 50%. When the phase offset is 180◦ ,the two inverters still output two square voltage waveforms, but since they are now out of phase, they superimpose on the current doubler filter input nodes F1 and F2 , making the converter's duty cycle effectively 100% and the output current very close to dc. Key waveforms with the phase-shift control are shown in Fig.

The two inverters are still operating in open-loop bus converter mode. During the time t_{lag} and the phase-lag offset ; each inverter transfers power to a different half-side of the current-doubler output filter. During 180◦ − ; the two inverters transfer power to the same half-side of the filter. The current of the other half-side of the filter is freewheeled by diodes D_7 or D_8 .If the power transformer's turn radio is n:1:1, the converter input–output voltage relationship is described as

$$Vo = 0.5 \times Vin \times 0.5 + \phi/360◦/n \qquad (1)$$

and the converter's duty cycle is

$$D = 0.5 + \phi/360◦ \qquad (2)$$

This converter actually transfers power from the primary side to the secondary side during both D and 1 − D periods. This important feature indicates that power is always flowing from primary to secondary at any moment. It is also the reason why there are no circulating currents on the primary side, and substantiates the possibility that this converter could be suitable for high-density designs.

Since ϕ can only vary from zero to 180◦, the minimum regulated output voltage will be $0.5 \times Vin/n$. To have a lower regulated voltage, which happens during power-supply startup, over load, and short circuit, the converter needs to switch to PWM mode control. Fig. shows the switching between phase-shift mode and PWM mode. By using PWM control, the converter can regulate its output down to 0 V, but the two inverters will lose soft switching. A dc–dc power-supply startup normally takes less than 100 ms, so hard switching during this time will have very little effect on overall circuit performance and efficiency. To avoid component damage, it is a common practice for a converter to respond to a short circuit by shutting down and restarting for a few seconds several times. A converter's thermal constant is usually much longer than a few seconds, so hard switching should not cause thermal stress during this operation. Another possible cause for damage is overload. When overload occurs, constant power or current control could allow a converter's output to stay somewhere below half of the maximum output voltage, $0.5 \times$ in $/n$. Under this scenario, the converter will have to deliver maximum current while operating under hard switching. If it lasts too long, thermal stress could be an issue. However, such cases are usually managed with shutdown controls. For a 48-V output rectifier, for example, the maximum output voltage is usually designed at 60 V or below. Downstream dc–dc modules or backup batteries would shut down the system before the 48-V bus voltage drops down to 30 V. If this is the case for a given application, the dual half-bridge converter topology could be a good candidate for the design.

When using diodes for rectification, the converter's output induct or current can become discontinuous when the load becomes light enough and its control loop could adjust the switching duty cycle below 50%. With the decrease of the duty cycle, the half-bridge's top- and bottom-side MOSFETs have a much larger equivalent dead time. During dead time, because of the circuit's parasitic capacitance and leakage energy, the half-bridge's switching node briefly rings, then settles down at half of the dc-bus voltage. If the bus voltage is half-nominal,

the switching losses are reduced to approximately one-fourth what they would be at the nominal input voltage when the switches are turned ON. Because switching loss dominates the total loss at light loads, this natural characteristic of a half bridge topology would help improve efficiency. And because the two inverters have the same switching duty cycle and operate independently, one inverter can actually be turned OFF to further reduce the switching loss by half. This is another important feature of this topology.

III. PROPOSED CIRCUIT OPERATION

To better address the complete operating sequence of this topology, refer once more to the dual half-bridge converter with the diode rectification circuit shown in Fig. The converter's two half-bridge inverters always operate at a 50% switching duty cycle when the output voltage is regulated above half of its maximum input voltage. The magnetizing currents of the power transformers reach a constant and stable peak value at the end of each half switching cycle, assuming that there is no magnetic flux walking and that the circuit operates in CCM. When one half-bridge's switch is turned OFF and before the complementary switch is turned ON, the magnetizing current and reflected-output current fast charge and discharge the switching devices' parasitic capacitance until the voltage across the power transformer windings decreases to zero. Both leading and lagging inverters work in the same way in this first part of the commutation period. After that, the lagging inverter continues its commutation by utilizing its magnetizing energy since its transformer secondary is basically open, while the leading inverter relies on the energy of its power-transformer leakage inductance and resonant inductor to activate a resonance between the inductance and the switches' parasitic capacitance.

A transformer's properly sized magnetizing inductance can usually store enough energy for the lagging bridge to achieve ZVS regardless of the output load. Because magnetizing current only applies to the lagging bridge's parasitic capacitance, the voltage slew rate of the lagging-bridge's switching node becomes much softer during this commutation period compared with a conventional phase-shifted full-bridge converter. The operating sequence of the circuit can be divided into five time intervals beginning with *t*1 which is the end of the last cycle in the sequence.

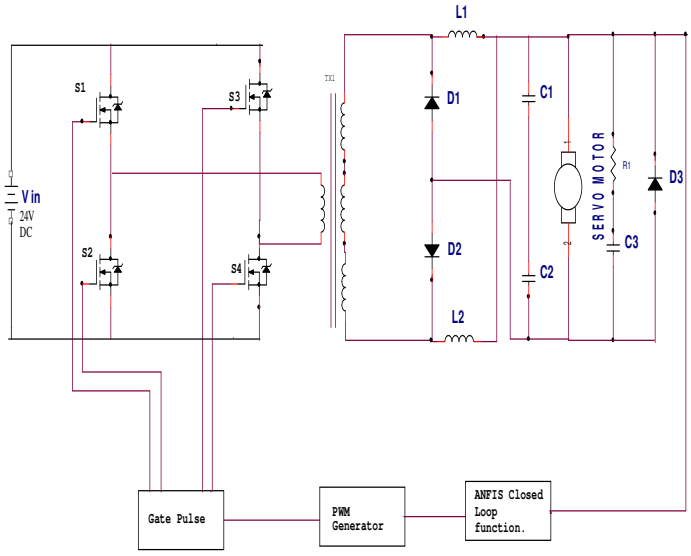

Fig.2. Proposed circuit diagram of closed loop dual half-bridge dc–dc converter fed servo motor

Mode 1 with t1 ≤ t < t2

During this period, switches Q1 and Q4 are ON. The t1 time is the moment when freewheel diode D7 ends its reverse recovery. The reverse-recovery current of diode D7 is reflected to transformer T1's primary. Most of its corresponding energy, residing in inductor Lr, is captured by clamping diode D1. The rest of the energy residing in the primary- and secondary-side leakage inductance of T1 cannot be captured by the clamping diode, and could cause some voltage ringing at node N1. To minimize the voltage ringing, the leakage inductance of T1 should be minimized. The captured current (ID1) circulates within the loop formed by Q1, Lr and D1 and begins to decline due to the conduction loss of the loop. Half-bridge capacitors, C1 and C2, are connected to T1 and T2's primary windings, respectively. Their voltages are coupled to the secondaries and then applied to the output filter through the output rectifiers (D3 and D6). Energy is transferred from the primary sides to the secondary sides during this time period, therefore the inductor currents (IL1and IL2) are increasing. C1 and C2 equally divide the bus voltage. Since the two transformers' primary currents cancel each other when they pass through capacitors C1 and C2, the capacitor voltage ripple can be controlled to a small value, with relatively small capacitance. The capacitors' peak-to-peak ripple can be calculated by the following equation.where D is the converter's duty cycle, C is the total capacitance of half-bridge capacitors C1 and C2, n is the transformer turns ratio, and fs is the switching frequency. The capacitor ripple reaches its peak value at full power with a 0.5 converter duty cycle.

Mode 2 with t2 • t • t3

At t2, transistor Q4 is turned off. After Q4 is turned off, capacitor C Q4 is charged up almost linearly by the reflected L2 current (IL2). After its voltage surpasses C2's voltage and transformer leakage energy is fully discharged, the voltage across transformer T2 reverses its polarity and becomes positive. Free wheel diode D8 conducts and takes over the IL2 current from D6 such that D6 becomes electrically disconnected. The leading bridge maintains its previous state and continues to apply a voltage to node F1 through diode D3, while both output rectifiers D5 and D6 of the lagging bridge remain open. During this period, capacitor CQ4 is continuously charged up by T2's magnetizing current. The worst-case scenario is when the load is zero. The magnetizing inductance is the only current to charge CQ4 and discharge CQ3.

Mode 3 with t3 < t < t4

During this period, the two inverters share their output current (IL1). Because the two transformer outputs (VM1and VM2) have almost the same voltage, the current shifting from the leading half bridge to the lagging half bridge is usually slow. Therefore, the leading half bridge usually shares more output current than the lagging half bridge during this time period. In the meantime, free wheel diode D8 maintains its previous state such that conducting currents IL1 and IL2 start to decrease as Vo applies to L2 with reverse polarity. The decrease of IL2 and the increase of IL1 lead to a partial current-ripple cancellation, minimizing output ripple voltage.

Mode 4 with t4 • t < t5

At t4, Q1 is turned off. Parasitic capacitance CQ2 is discharged. Parasitic capacitance CQ1 is charged by the resonant inductor current (ILr) which includes T1's magnetizing current, the reflected inductor current (IL1) shared by the leading inverter and the captured reverse recovery current of freewheel diode D7 in Mode 1. With the current sharing shifting from the leading inverter to the lagging inverter, ILr decreases. D3 maintains conduction until ILr decreases to the magnetizing current value. During this period, CQ2 can be completely discharged if the converter output current reaches a certain level and the resonant inductor (Lr) has sufficient energy stored. If the stored energy is not sufficient, D3 turns off softly before CQ2 is completely discharged. The voltage across T1 (Vp1) starts to decrease and eventually reverses its polarity. Output inductor current (IL2) is still passing through D8 for CCM, so T1's secondary is essentially shorted by D4 and D8. Therefore, T1's magnetizing current (energy) cannot further contribute to the discharge of CQ2.

Mode 5 with t5 ≤ t < t6

After Q2 is turned on at t5, the inductor current (ILr) decreases to zero quickly and then begins to build up in the opposite direction. When its reflected current at the secondary surpasses output current (IL2) and D8's reverse-recovery current, D8 stops conducting at t6. Time t6 is the end of one half-cycle. The process then repeats for the next half-cycle with the complementary components operational. Each complete switching cycle consists of two complimentary half-cycles. During startup, overload or light load, the converter needs to operate in PWM mode. For this mode, as described previously, the converter is effectively a hard-switching half bridge with two paralleled inverters and a modified current-doubler output. The PWM gate signals applied to the two inverters are in phase.

IV.SIMULATION RESULTS

A 24–230 V, dc–dc converter was designed to validate the concept and demonstrate the circuit performance. The Anfis controller is located on the secondary side. It generates both converter-bridge gate signals and SyncFET drive signals. The bridge gate signals are passed to the primary side by TI digital isolator ISO7240, while SyncFETs are driven directly by the TPS2814. The output rectification circuit was rearranged as shown in Fig. so that both diodes and FETs could be tested on the same power board with a common ground. Freewheel devices *D*3 and *D*4 remain diodes to allow the circuit to operate in discontinuous conduction mode and avoid the voltage spike caused by the negative-output inductor current. *D*3 and *D*4 can be replaced by FETs to decrease conduction loss. For this case, the rectifier FETs and freewheel FETs should have some turn-on overlapping to avoid any voltage spike. This provides the efficiency data when the output rectification used diodes as well as SyncFETs. The curves show that the 230-V output circuit is able to achieve 95.2% maximum efficiency with diode-based output rectification, 96% maximum efficiency with a SyncFET rectification circuit, and 92% efficiency at 20% load. When the load was below 7% of the full load, the converter was switched to PWM mode and one half bridge was actually turned OFF to prevent significant loss. Peak-current mode control can be used to eliminate the capacitor if necessary. The circuit parameters and components used in this test were the following:

1) Primary power MOSFETs
2) Freewheel diodes
3) Output inductor
4) Magnetizing inductance
5) DC blocking capacitor
6) Secondary rectifier
7) Resonant inductor
8) Power transformer turns radio
9) Half-bridge capacitors
10) Switching frequency

11) The anfis controller digital power controller. Fig .shows the transformer primary voltage and current experimental waveforms with a 50% load.

Both the leading and lagging inverters do not have circulating current, and their voltages and currents are in phase. Fig. shows the simulation diagram and results.

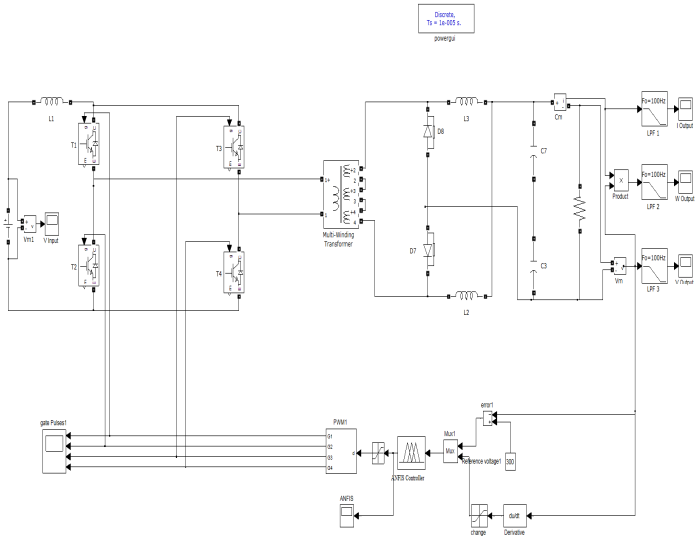

Fig.3. simulation diagram of dual half-bridge dc–dc converter fed servo motor

The following fig shows the input voltage, gate pulse, output voltage, output current, output power, and anfis output.

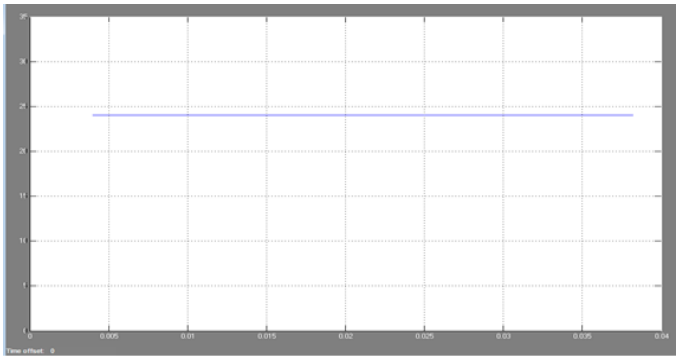

Fig 4. Input voltage Waveform

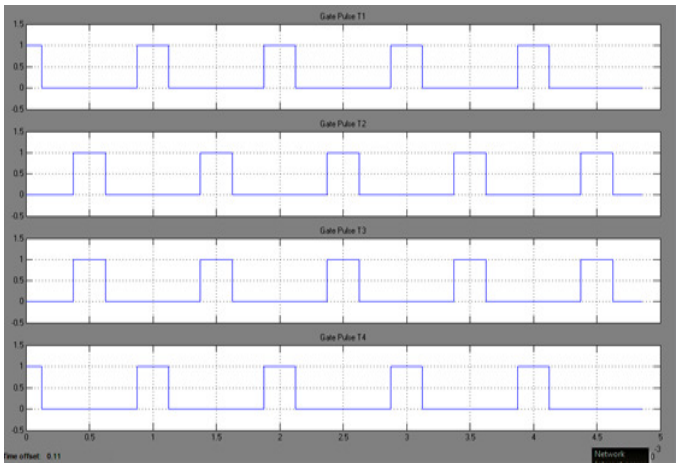

Fig 5. Gate pulse Waveform

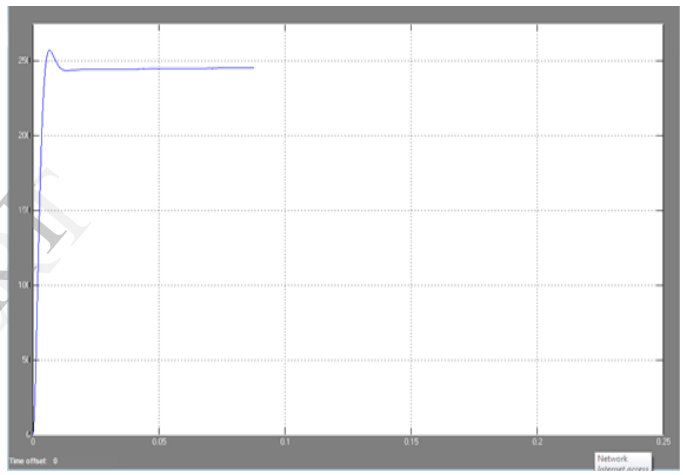

Fig 6. Output voltage Waveform

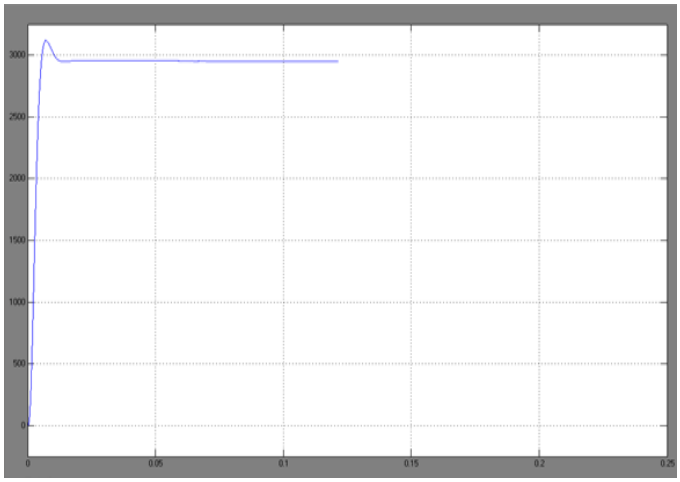

Fig 7. Output power Waveform

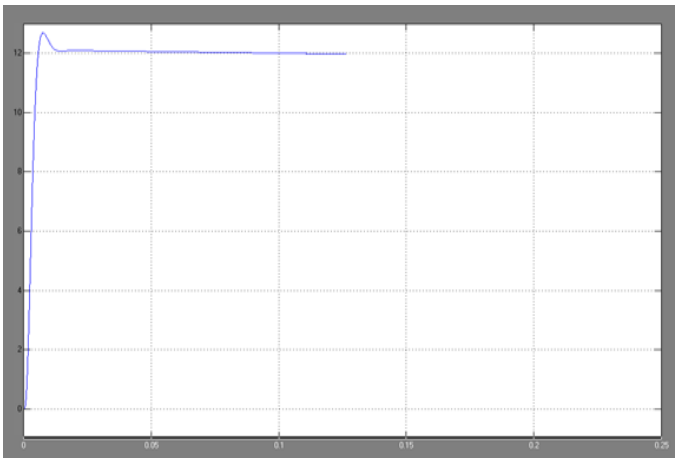

Fig 8. 0utput current Waveform

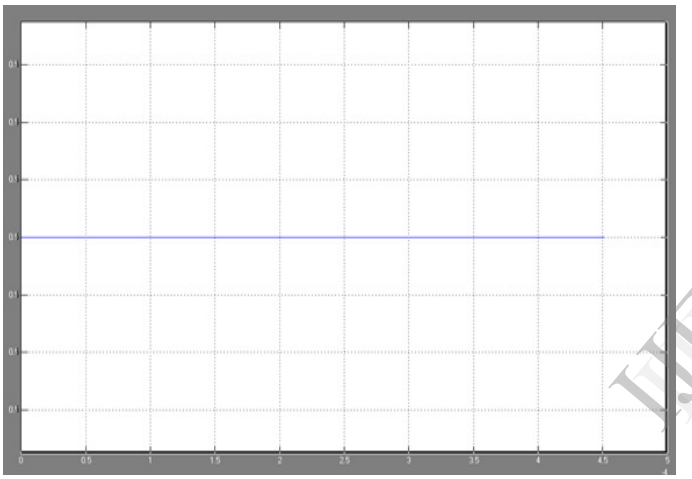

Fig 9. Anfis Waveform

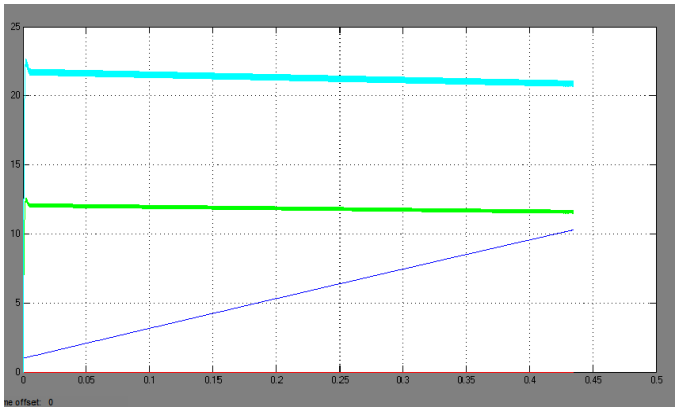

Fig 10. Motor output Waveform

V.CONCLUSION

This project explored a different approach to achieving the following goals: load-independent and wide range ZVS with efficiency improvement at both heavy and light loads, no circulating current and reactive power, 100% time utilization for power transformation and optimal use of magnetic components, and minimum semiconductor device stress. These are the necessary design elements for high power density and peak efficiency. Light-load efficiency can also be improved by turning OFF one half-bridge inverter. The dual half-bridge topology is most suitable for ac–dc power-supply designs that have a pre-regulated intermediate dc bus and dc–dc converter designs that need to use diodes for output rectification. From a packaging point of view, this topology is also a good candidate for high-power, high-density, and low-profile designs.

REFERENCES

[1] Zhong Ye, "Dual Half-Bridge DC–DC Converter With Wide-Range ZVS and Zero Circulating Current ," IEEE Trans. Power Electron., vol. 28, no. 7, July 2013.

[2] X. Zhang, W.Chen, X. Ruan, and K. Yao, "A novel ZVS PWM phaseshifted full-bridge converter with controlled auxiliary circuit," *Proc. Appl.Power. Electron. Conf., Feb. 2009, pp. 1067–1072.*

[3] Zhong Ye, "Phase-shifted dual-bridge DC/DC converter with wide-rangeZVS and zero circulating current," U.S. Patent Appl. No. 12315166, Nov.2008.

[4] Y.Jang and M. M. Jovanovic, "A new family of full-bridge ZVS converters,"in *Proc. Appl. Power Electron. Conf. Exhib., Feb. 2003, vol. 2,*pp. 622–628.

[5] E. S. Kim and Y. H. Kim, "A ZVZCS PWM FB DC-DC converter using amodified energy-recovery snubber," *IEEE Trans. Ind. Electron., vol. 49,*no. 5, pp. 1120–1127, Oct. 2002.

[6] B. Andreycak, "Phase shifted, zero voltage transition design considerations and the UC3875 PWM controller," Texas Instruments, Dallas, TX, TI Literature No. SLUA107.

[7] X. Wu, J. Zhang, X. Xie, and Z. Qian, "Analysis and optimal design considerations for an improved full bridge ZVS DC-DC converter with high efficiency," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1225– 1234, Sep. 2006.

[8] E. S. Kim and Y. H. Kim, "A ZVZCS PWM FB DC-DC converter using a modified energy-recovery snubber," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1120–1127, Oct. 2002.

[9] X. Wu, J. Zhang, X. Xie, J. Zhang, R. Zhao, and Z. Qian, "Soft switched full bridge DC-DC converter with reduced

circulating loss and filter requirement," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1949–1955, Sep. 2007.

[10] P. Imbertson and N. Mohan, "Asymmetrical duty cycle permits zero switching loss in PWM circuits with no conduction loss penalty," *IEEE Trans. Ind. Appl.*, vol. 29, no. 1, pp. 121–125, Jan.–Feb. 1993.