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Seven Level Hybrid Cascaded H-Bridge Multilevel Inverter

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***Abstract*—The poor quality of voltage and current of a PWM inverter fed induction machine is due to the presence of har- monics and hence there is significant level of energy losses. The Multilevel inverter is used to reduce the harmonics. The inverters with a large number of steps can generate high quality voltage waveforms.A cascaded H-bridge multilevel inverter that can be implemented using only a single dc power source and capacitors. Standard cascaded multilevel inverters require n dc sources for 2n + 1 levels. Without requiring transformers, the scheme proposed here allows the use of a single dc power source with the remaining n-1 dc sources being capacitors .which is referred to as hybrid cascaded H-bridge multilevel inverter. HCMLI using only a single dc source for each phase is promising for high- power Motor drive applications, as it significantly decreases the number of required dc power supplies, provides high-quality output power due to its high number of output levels, and results in high conversion efficiency and low thermal stress as it uses a fundamental frequency switching scheme. The number of switches can also be reduced from the previous topologies by using this method..**

***Index Terms*—Hybrid cascade multilevel inverter, Cascaded Multilevel Inverter, Fundamental Frequency Modulation, Pulse width modulation,Switching loss reduction,Total harmonic dis- tortion**

I. INTRODUCTION

MULTILEVELinverter structures are superior as a choice of electronic power conversion for medium voltage and high power applications since it has improved output wave- form which in turn reduces its respective harmonic content.It reduces the EMI and eliminate the need of filters. In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium- voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16,6.9 kV). For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms.

One of the biggest problems in power quality aspects is the harmonic contents in the electrical system. Generally, harmon- ics may be divided into two types: 1) voltage harmonics, and 2) current harmonics. Current harmonics is usually generated by harmonics contained in voltage supply and depends on the type of load such as resistive load, capacitive load, and inductive load. Both harmonics can be generated by either the source or the load side. Harmonics generated by load are caused by nonlinear operation of devices, including power converters, arc-furnaces, gas discharge lighting devices, etc. Load harmonics can cause the overheating of the magnetic cores of transformer and motors. On the other hand, source harmonics are mainly generated by power supply with non- sinusoidal voltage waveform. Voltage and current source harmonics imply power losses, Electromagnetic Interference (EMI) and pulsating torque in AC motor drives.Thus the reduction of harmonics become one of the major issue in these electrical and electronic systems. thus the concept of using multilevel inverters were introduced in to various fields after its evolution.

The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the sig- nificant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources.The so-called multilevel starts from three levels. As the number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels ,however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. three capacitor voltage synthesis-based multilevel inverters are introduced, i.e. 1) Diode-Clamped Multilevel Inverter 2) Flying-Capacitor Multilevel Inverter 3) Cascaded-Inverters with Separated DC Sources.

Unlike the diode clamp or flying capacitors inverter, the cascaded inverter does not require any voltage clamping diodes or voltage balancing capacitors. This configuration is useful for constant frequency applications such as active frontend recti- fiers, active power filters, and reactive power compensation. Choosing appropriate conducting angles for the H bridges can eliminate a specific harmonic in the output waveform.

There are several types of multilevel inverters but the one considered in This paper is the Hybrid cascaded multilevel inverter (HCMLI). The structure of the HCMLI is not only simple and modular but also requires the least number of components compared to other types f multilevel inverters. This in turn, provides the flexibility in extending the HCMLI to higher number of levels

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without increase in circuit complexity as well as facilitates packaging.

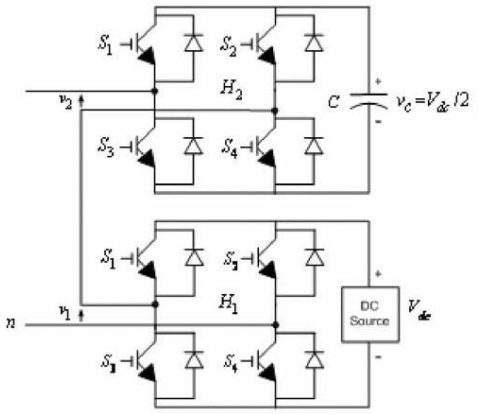

Fig. 1. Single phase structure of a Multilevel cascaded H-bridge inverter.

II. MULTILEVEL INVERTER ARCHITECTURE

Each phase of a cascaded multilevel inverter requires n dc sources for 2n + 1 levels. For many applications, obtaining so many separate dc sources may preclude the use of such an inverter. To reduce the number of dc sources required when the cascaded H-bridge multilevel inverter is applied to a motor drive ,a scheme is proposed in this paper that allows the use of a single dc source (such as battery or fuel cell) as the first dc source with the remaining n-1 dc sources being capacitor in the cascaded H-bridges multilevel inverter, which is referred to as the hybrid cascaded H-bridge multilevel inverter (HCMLI). the proposed HCMLI has a low number of dc sources and retains the low switching-frequency advantage. The control goal of the HCMLI needs to maintain the balance of the dc voltage level of the capacitors while producing a nearly sinusoidal three-phase output voltage using a low-switching frequency harmonic elimination method.

III. WORKING PRINCIPLE OF SEVEN LEVEL HCLMI

A 7-level hybrid cascaded H-bridge multilevel converter has two H-bridges for each phase, one H-bridge is connected to a DC source, another H-bridge is connected to a capacitor as shown in Fig 1. The DC source for the first H-bridge (H_1) could be a battery or fuel cell with an output voltage of V dc, and the DC source for the second H-bridge (H_2) is the capacitor voltage to be held at V c. The output voltage of the first H-bridge is denoted by V_1, and the output of the second H-bridge is denoted by V_2 so that the output voltage of the cascaded multilevel converter is

$$V(t) = V_1(t) + V_2(t).$$

By opening and closing the switches of H_1 appropriately, the output voltage V_1 can be made equal to V_{dc}, 0, or V_{dc} while the output voltage of H_2 can be made equal to $+V_{dc}/2$, 0, and $V_{dc}/2$ by opening and closing its switches appropri- ately. To regulate the capacitors voltage to guarantee the output power quality, 7-level fundamental switching scheme has been proposed. This switching scheme uses a possible cycle to output $-(V_{dc}+V_c)$, $-V_{dc}$, $-(V_{dc}-V_c)$, 0, $(V_{dc}-V_c)$, V_{dc}, $(V_{dc}+V_c)$

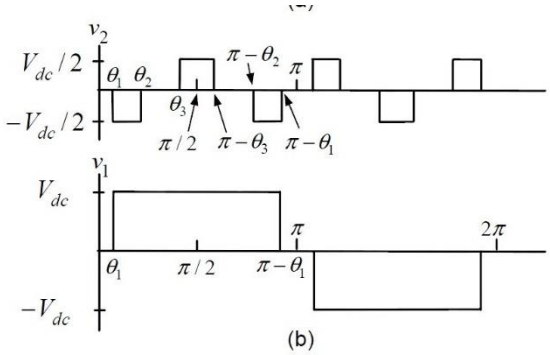

Fig. 2. H-Bridge Voltages V_1 And V_2 Which Achieve The Same Output Voltage Waveform $V = V_1 + V_2$.

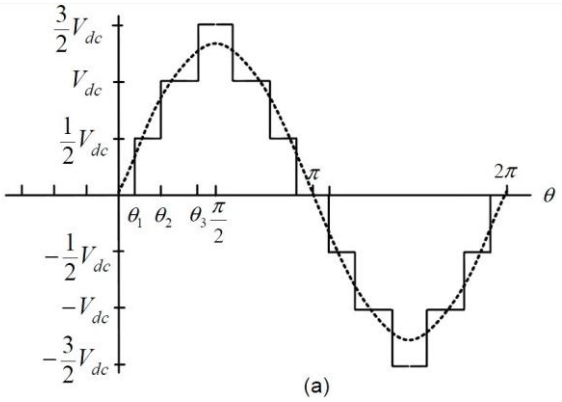

Fig. 3. Output Waveform Of An 7-Level Hybrid Cascade Multilevel Inverter.

voltage levels.And the DC source is charging the capacitor si- multaneously when producing $-(V\ dc-V_c)$ and $(V\ dc-V_c)$ which is called a charging cycle. Similarly, the switching scheme uses another possible cycle to output $-(V\ dc+V_c)$, $-V_{dc}$, $-V_c$, 0, V_c,V_{dc}, $(V\ dc+V_c)$ voltage levels, and the capacitor can be discharged simultaneously which is called a discharging cycle. Then the capacitors voltage can be regulated by charging and discharging when the multilevel converter is running. When

$+V_{dc}/2$ is chosen, the output voltage waveform is a 7-level waveform.

By opening and closing the switches of H_1 appropriately, the output voltage V_1 can be made equal to $-V_{dc}$, 0,V_{dc} or while the output voltage of H_2 can be made equal to $+V_{dc}/2$, 0, or $V_{dc}/2$ by opening and closing its switches appropriately. Therefore, the output voltage of the inverter can have the values $-3V_{dc}/2$, $-V_{dc}$, $-V_{dc}/2$, 0, $V_{dc}/2$, V_{dc}, $3V_{dc}/2$ which is seven levels. Thus output seven level voltage can be achieved by adding V_1 and V_2 in two different ways.The output seven level voltage waveform obtained by adding the two voltage level is represented in figure3.

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Fig.2 shows how the waveform of Fig.3 is generated.Let θ be the angular range for the operation of H-bridges.If For θ_1 $\theta <$ θ_2, V_1 = V_{dc} and V_2= $V_{dc/2}$ are chosen. The fact that the output-voltage level $V_{dc/2}$ can be achieved in two different ways is exploited to keep the capacitor voltage regulated.which is explained in the figure4. For obtaining 7 level in this HCMLI capacitive source

θ	v_1	v_2	$v = v_1 + v_2$
$0 \le \theta \le \theta_1$	0	0	0
$\theta_1 \le \theta \le \theta_2$	0	$V_{dc}/2$	$V_{dc}/2$
$\theta_1 \le \theta \le \theta_2$	V_{dc}	$-V_{dc}/2$	$V_{dc}/2$
$\theta_2 \le \theta \le \theta_3$	V_{dc}	0	V_{dc}
$\theta_3 \le \theta \le \pi/2$	V_{dc}	$V_{dc}/2$	$3V_{dc}/2$

Fig. 4. Output Voltages For A 7-Level Inverter.

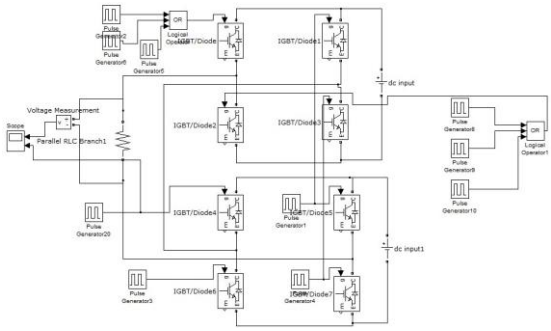

Fig. 5. Seven Level Hybrid Cascaded H-Bridge Multilevel Inverter For Single Phase Induction Motor.

should have a value half to the dc input supply is selected. Capacitance value is decided based on the following factors. 1)The capacitance value is chosen large enough so that the variation of its voltage around its nominal value is small (generally speaking, one can choose the capacitorload time constant to be ten times than that of the fundamental period)
2) the capacitor charging energy is greater than or equal to the capacitor discharge energy in a cycle.

IV. SIMULATION ANALYSIS

The simulation results of hybrid cascaded h-bridge seven level multilevel inverter for single phase induction motor and the simulation results for three phase circuit is also given. The hybrid cascaded H-bridge MLI for single phase circuit is given in figure5. The single phase circuit consist of two H- bridges. Each bridge consist of four IGBTS. The two bridges are connected together, also a load resistor is connected across the bridges. The output is taken across the load resistor. The two bridges consists of seperate input dc sources. a proper switching sequence is selected for producing the seven levels at the output by opening and closing the switches of the two H-bridges. Here pulse generators are used for producing the necessary pulse width and phase delay. if necessary pulse generators are combined together through OR gates to produce the required pulses. a seven level waveform is obtained as the output of the given circuit.

For extending a hybrid cascaded H-bridge multilevel inverter for single phase circuit in to three phase circuit, three single phase circuits are connected together through one end terminal. And through the other end they are connected to a three phase star connected load. the voltage across the three phases are measured and is viewed through a scope. For

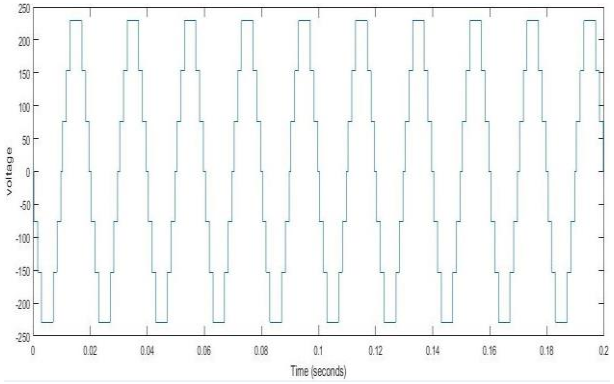

Fig. 6. Output Waveforms For Single Phase seven level Circuit.

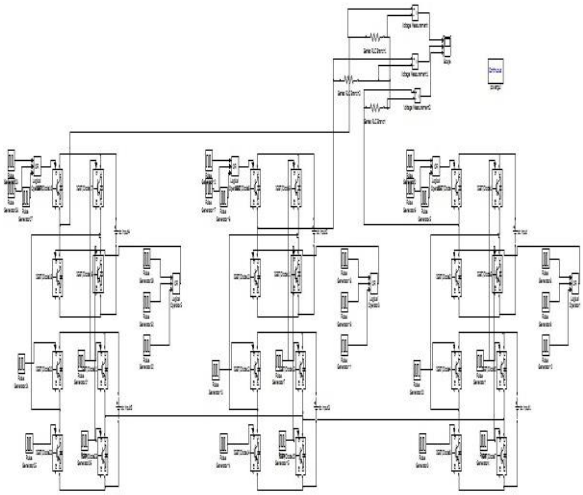

Fig. 7. Hybrid Cascaded H-Bridge Multilevel Inverter For Three Phase Induction Motor

obtaining the three phase circuit output we wanted to maintain 120° phase shift across the three single phase circuits. thus seven level output voltage waveforms which are phase shifted by 120° is obtained in the three phases as output.Which is shown as the simulated output of the three phase circuit is given in figure 8.
The output waveform of a three phase hybrid cascaded multilevel inverter which is 120° phase displaced with each other is represented in figure 8. Here simulation is done for obtaining an output voltage of 230 in both single and three phase circuits.
The HCMLI three phase circuit is connected to an asynchronous machine model is simulated and is represented in fig- ure9. A constant torque and the outputs from three single phase circuits are fed as an input to the asynchronous machine. The various parameters of stator, rotor, also mechanical parameter can be included in the measurement by selecting parameters using the bus selector. Here stator currents through three phases is

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measured. And their phase shifted output waveform obtained is shown as the simulated result. The three phase

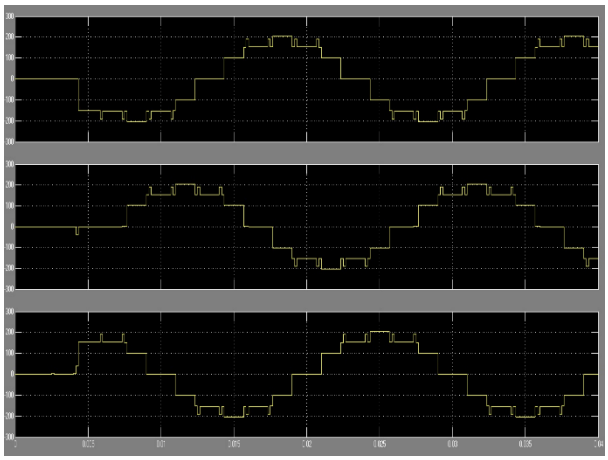

Fig. 8. Output Waveforms For Three Phase Circuit

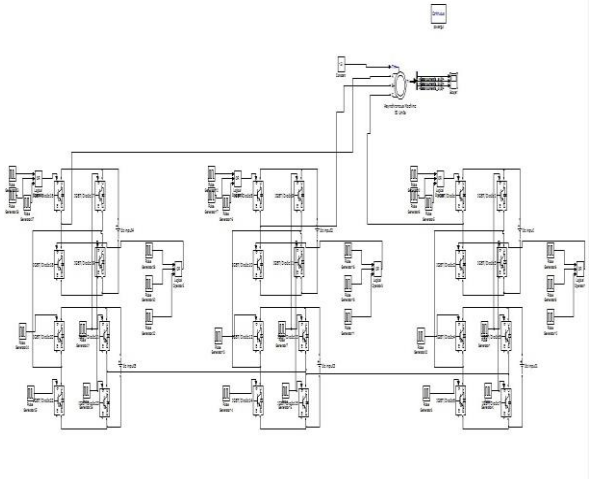

Fig. 9. Hybrid Cascaded H-Bridge Multilevel Inverter Three Phase Circuit Connected to an Induction Motor.

HCMLI connected to an induction machine is represented as figure 9. And their stator current output waveforms are represented by using figure 10. Here measurement is taken on 5.4HP,400V,50Hz,1430RPM Asynchronous machine and its stator parameters are plotted by using this method. In all these circuits pulse width and phase delays are adjusted using pulse generators method.Which is method used in this paper for simulation.

The stator currents represented in figure10 which are dis-placed 120° to each other in their all three phase.Similarly rotor parameters,mechanical parameters of induction motors can be plotted by using their simulation.

V. HARDWARE IMPLEMENTATION

The hardware circuit of the prototype is divided into two parts: the microcontroller based control circuit and power circuit. The power circuit consists of two H-bridges, each H- bridge consisting of four MOSFET named IRF830.Also the

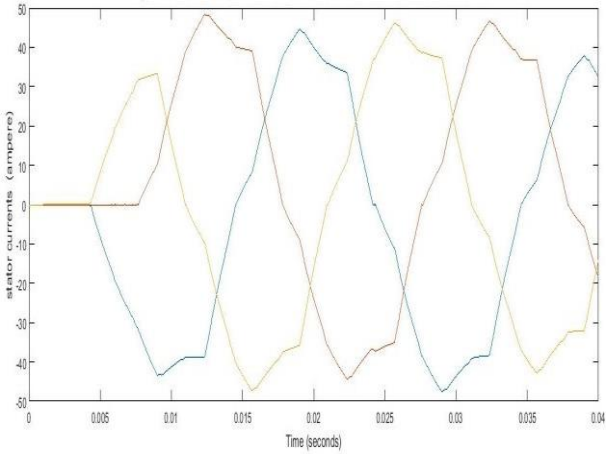

Fig. 10. Output Stator Current Waveforms For A Three Phase Circuit Connected To An Induction Motor.

section consists of a single dc source for the H1 bridge and capacitive source for the H_2 bridge. The control circuit section consisting of an easily programmable and erasable 89C51 microcontroller and four fan I c's(IC7392).The assembly lan- guage program burned in to the microcontroller determines the duration of gate pulses of each MOSFETs, thus the switching of H-bridge.FAN7392 is a high speed power MOSFET and IGBT gate driver and fan I c's acts as an interface between the H-bridge and 89C51 microcontroller.

The main portions of the HCMLI is Power circuit and Control circuit. These circuits are explained in this section.The power circuit mainly consists of two H-bridges. which are cascaded together. Here each H-bridge consists of four switch- ing devices. That is four MOSFETs(IRF830).Thus the power circuit totally consists of eight switches. The MOSFETs in the power circuits are driven using fan I c's(IC 7392).Each fan I c is capable of driving two MOSFETs. Fan I c's are the part of the control circuit. Here the switching action of the MOSFETs of the power circuit provides the necessary output voltage waveform across the load terminals. Which is determined by the gate signals generated by the control circuit consisting of 89C51 microcontroller. Here a portion of the power circuit consisting of a single H-bridge having four switches driven using two fan I c's are represented in figure11

The control circuit mainly consists of a microcontroller 89C51.Which is easily programmable and erasable for 1000 cycles. And four fan I c's (IC 7392).Which are used for the gate driving of high speed MOSFETs. And these fan I c's acts as an interface between the 89C51 and the

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power circuit. An assembly language program is written and it is burned in to the 89C51.The width of the gating signals required for triggering MOSFETs is determined by the 89C51.Thus by changing the program written in the 89C51 it is possible to change the switching pattern of the power circuit. Crystal oscillator is provided in this circuit to give necessary clock input to the microcontroller. A reset switch is also provided in this circuit. Which is used for resetting the operation of the microcontroller. The 89C51 used in the control circuit is schematically represented in figure12.

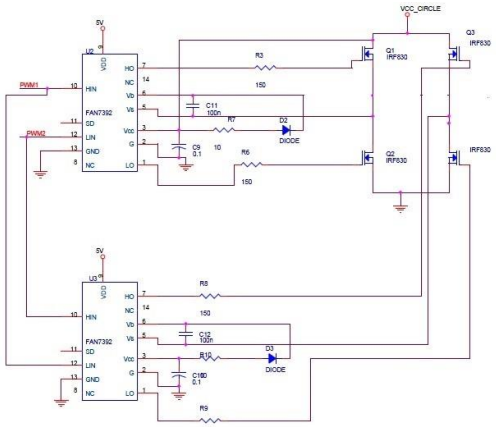

Fig. 11. Power Circuit Consisting Of H-Bridge Controlled By Fan I cs

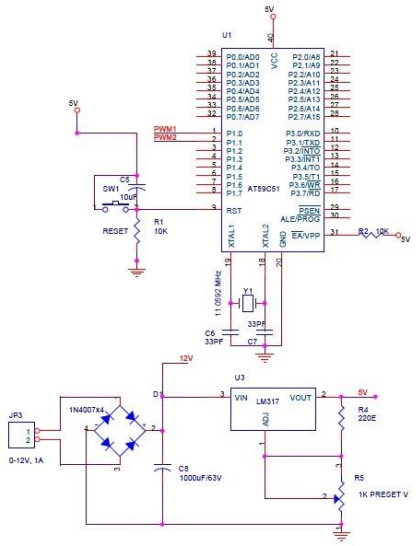

Fig. 12. Control Circuit Consisting Of AT89C51 Microcontroller

The voltage required for the working of the 89C51 is 5V.This can be generated from a 12V dc supply by using a voltage regulator LM317 by varying the variable resistor of voltage regulator. Diode bridge circuit and capacitors are necessary when the input supply is ac.The hardware circuit is represented in figure13.

VI. RESULTS AND DISCUSSIONS

The gating signals required for triggering the switches of bridge H_1 is represented in figure14. This gating signals for switches from S1-S4 is measured in the DSO. This gating signals are measured from the pin no 1-4 of 89C51 microcon- troller using the DSO or these signals can be measured from the Fan I cs.

The gating signals required for triggering the switches of bridge H_2 is represented in figure15. This gating signals for switches from S5-S8 is measured in the DSO. This gating signals are measured from the pin no 5-8 of 89C51 micro- controller using the DSO or these signals can be measured from the Fan I cs. These gating signals determines the proper

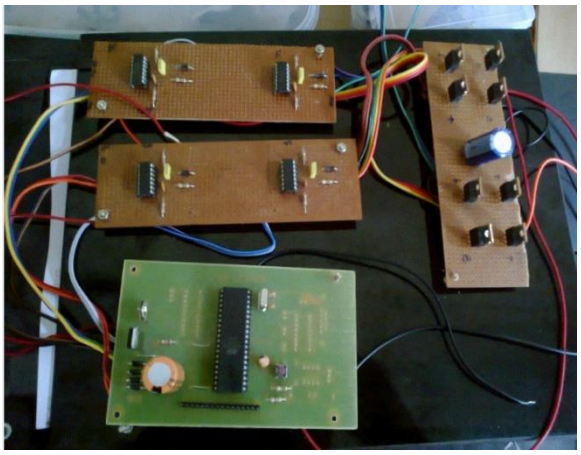

Fig. 13. 7 Level Hybrid Cascaded H-Bridge MLI.

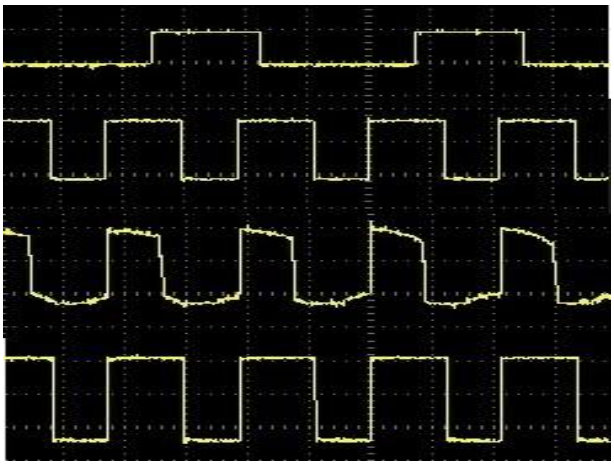

Fig. 14. The Gating Signals For Switches S_1-S_4 Obtained In DSO

switching strategies of H-bridges and their output waveforms also.

The HCMLI circuit is wired. Input supply of 12V dc is supplied to the input terminals of 89C51.The two output terminals of H-bridges are connected across the probes of the

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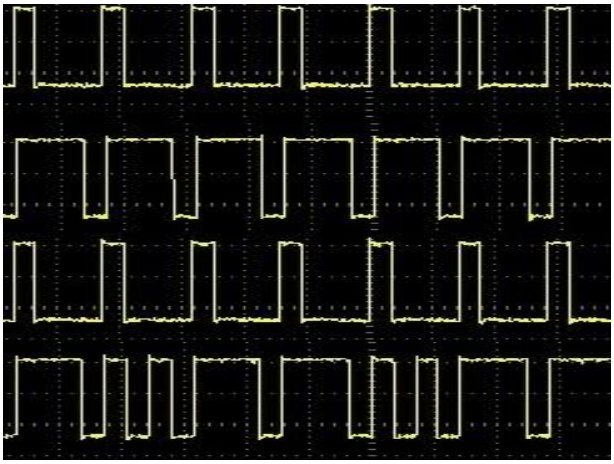

Fig. 15. The Gating Signals For Switches S5-S8 Obtained In DSO

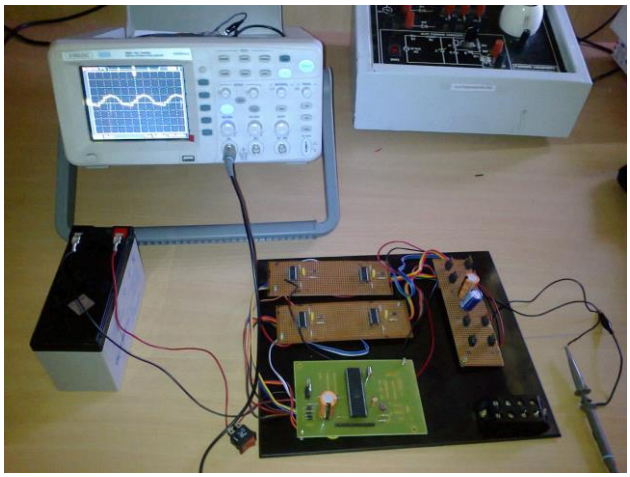

Fig. 16. Seven Level HCMLI Experimental Setup With Output Waveform

Fig. 17. 7 Level Output Voltage Waveform

DSO .The output of HCMLI is seen across its output terminals. By making necessary adjustments in the DSO a seven level voltage waveform is obtained in the DSO. Which is the required result. The output waveform obtained by connecting the seven level hybrid cascaded multilevel inverter in the DSO is represented in figure15.

In this experiment by cascading the output voltages of two H-bridges here output is produced. Here output waveform is produced with reduced number of switches and dc input sources by this method. Also a reduced harmonic waveform can be generated by using this circuit. By changing the ratings of switches used, capacitor value, and small changes in the microcontroller program this low power rated prototype can be extended to high power single phase and three phase cir- cuits.The seven level output voltage waveform is represented in figure17.

VII. CONCLUSION & SCOPE OF FUTURE WORK

Hybrid Cascaded multilevel inverter topology here proposed, requires only a single DC power source. All others are capacitors. The voltage level of the capacitors can be controlled. The requirement of transformers can be eliminated. Harmonics in the output waveform can also be reduced by using this method. The components used in this HCMLI method is less than the previous MLI topologies, hence it is a cost effective method to produce reduced harmonics output waveform. Circuit for both single phase and three phase circuits are simulated and output wave form is also obtained. Induction motor is connected to the three phase circuit and the circuit is simulated. Hence obtained the different stator current waveforms for the circuit. Hard ware circuit for seven level hybrid cascaded multilevel inverter is designed and wired. The developed circuit is tested and seven level waveform is obtained.

By using the hybrid cascaded multilevel inverter topology the number of switches required for producing the same level of output waveforms is reduced compared to the previous multilevel inverter topologies. The number of dc sources required in this topology also reduced. Hence it is a cost effective method used for producing higher number of output voltage levels with reduced amount of harmonic content. Thus its application will increases in the field of medium voltage and high voltage drives in future. Also its applications will increases in the fields of better power(signal)quality.In this context, high performances and efficient torque and flux control are obtained, enabling a DTC solution for hybrid multilevel inverter powered induction motor drives intended for electric vehicle propulsion. Simulations and experiments show that the proposed multilevel inverter and control scheme are effective and very attractive for embedded systems such as automotive applications. The main merit of the new topology is to reduce the lower total harmonic distortion, lower elec- tromagnetic interference generation and high output voltage. This topology is extended to three phase systems from single phase systems and it will increase in future also.

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