Security Cash Withdrawal Through Mobile Phone Using Embedded System And GSM Technique

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1. ABSTRACT

The *Salvos* is an Australian word which defines the secured Army. The use of mobile handheld devices is expanding rapidly both within the business and individual context. These devices are now essential tools that offer competitive business advantages in today's growing world of ubiquitous computing environment. The technology advancement has made it possible to embed more facilities in mobile phones. While they provide benefits, they also pose new risks on security either by the information they contain or information that they can access remotely.

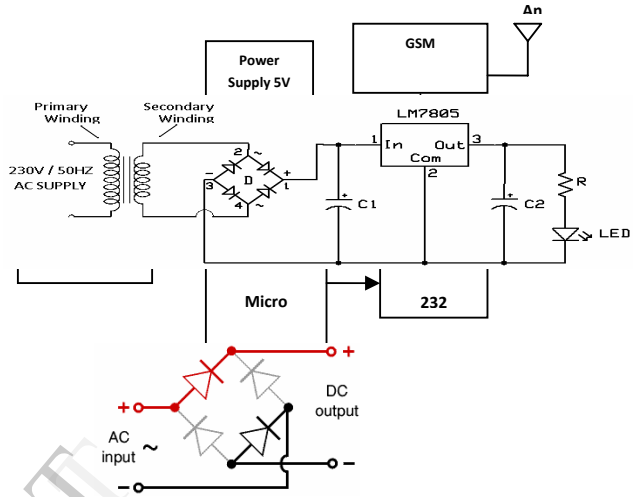
Secure cash transaction is of serious concern in growing use of cash cards and internet transactions. Cash withdrawal cards, chip and pin facility is one of the facilities which have increasingly been used for business and social activities. However, there has been limited research focus on security and flexibility.

This paper will introduce the concept of physical browsing and development of a system that will allow users to use their mobile phones to securely withdraw cash from ATM machines. The paper presents the architecture for the M-Cash withdrawal application and relevant technologies and security issues have been presented and relevant procedures and steps for fully implementing the application have been analyzed.

2. PROJECT DESCRIPTION

This ATM Management Project adding some applications gives extra features to the customers. In This project we have used AT89c51 microcontroller, SIMMCOM GSM module, KEIL IDE tool, 2x16 LCD display. Initially the ATM module gets the password from the user mobile and it matches with the initial password. If it matches, then an ATM module allows the use entering the Amount. Otherwise ATM module will informs the bank that wrong user trying to access the bank. If the users entered the amount, ATM module sends this amount to the authority user mobile and waits for the ACK message from the Authority mobile. If the ACK message is OK, then Process will be successfully completed. Otherwise it will inform the bank and also users Mobile that wrong user trying to Access the bank.

BLOCK DIAGRAM



DC POWER SUPPLY

Each of the blocks is described in more detail below:

Transformer - steps down high voltage AC mains to low voltage AC.

Rectifier - converts AC to DC, but the DC output is varying.

Smoothing - smooth's the DC from varying greatly to a small ripple.

Regulator - eliminates ripple by setting DC output to a fixed voltage.

TRANSFORMER

Transformer consists of two highly inductive coils wound on iron or steel core. It has two windings they are Primary & Secondary windings. The winding coil connected to the AC supply is called primary winding where as the order one is called Secondary winding.

As soon as the primary winding is connected to the single phase ac supply ,an ac current starts flowing through it.

The ac primary current produces an alternating flux □ in the core.

Most of this changing flux gets linked with the secondary winding through the core.

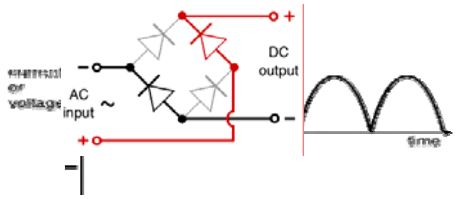
The varying flux will induce voltage into the secondary winding according to the faraday's law of electromagnetic induction.

RECTIFER

There are several ways of connecting diodes to make a rectifier to convert AC to DC. The bridge rectifier is the most important and it produces full-wave varying DC. A full-wave rectifier can also be made from just two diodes if a centre-tap transformer is used, but this method is rarely used now that diodes are cheaper. A single diode can be used as a rectifier but it only uses the positive (+) parts of the AC wave to produce half-wave varying DC. Rectifier diodes are used in power supplies to convert alternating current (AC) to direct current (DC), a process called rectification. They are also used elsewhere in circuits where a large current must pass through the diode. All rectifier diodes are made from silicon and therefore have a forward voltage drop of 0.7V which shows maximum current and maximum reverse voltage for some popular rectifier diodes.

The IN4001 is suitable for most low voltage circuits with a current of less than 1A. There are several ways of connecting diodes to make a rectifier to convert AC to DC. The bridge rectifier is one of them and it is available in special packages containing the four diodes required. Bridge rectifiers are rated by their maximum current and maximum reverse voltage. They have four leads or terminals: the two DC outputs are labeled + and -, the two AC inputs are labeled

The diagram shows the operation of a bridge rectifier as it converts AC to DC. Notice how alternate pairs of diodes conduct.



Dc +5v Regulated Power Supply Schematic Diagram

SMOOTHING

Smoothing is performed by a large value electrolytic capacitor connected across the DC supply to act as a reservoir, supplying current to the output when the varying DC voltage from the rectifier is falling. The diagram shows the unsmoothed varying DC (dotted line) and the smoothed DC (solid line).The capacitor charges quickly near the peak of the varying DC, and then discharges as it supplies current to the output.

VOLTAGE REGULATER

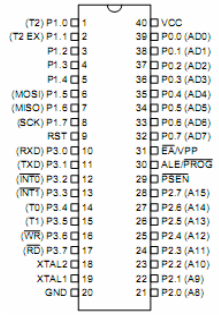
It is usually having three legs, converts varying input voltage and produces a constant regulated output voltage. They are available in a variety of outputs. The most common part numbers start with the numbers 78 or 79 and finish with two digits indicating the output voltage. The number 78 represents positive voltage and 79 negative one. The 78XX series of voltage regulators are designed for positive input. And the 79XX series is designed for negative input. The LM78XX series typically has the ability to drive current up to 1A. For application requirements up to 150mA, 78LXX can be used. As mentioned above, the component has three legs: Input leg which can hold up to 36VDC Common leg (GND) and an output leg with the regulator's voltage. For maximum voltage regulation, adding a capacitor in parallel between the common leg and the output is usually recommended. This eliminates any high frequency AC voltage that could otherwise combine with the output voltage. See below circuit diagram which represents a typical use of a voltage regulator.

This circuit is a small +5V power supply, which is useful when experimenting with digital electronics. Small inexpensive wall transformers with variable output voltage are available from any electronics shop and supermarket. Those transformers are easily available, but usually their voltage regulation is very poor, which makes then not very usable for digital circuit experimenter unless a better regulation can be achieved in some way. The following circuit is the answer to the problem. This circuit can give +5V output at about 150 mA current, but it can be increased to 1 A when good cooling is added to 7805 regulator chip. The circuit has over overload and thermal protection.

3. INTRODUCTION TO ATMEL89S52

The 8051 microcontroller is packaged in 40 pin Dual in line package (**DIP**).Out of 40 pins,16 pins are single function pins and 24 pins may be used for one or two entirely different function.

PIN DIAGRAM OF 8051



PIN CONFIGURATION

Single Function Pins (16 pins)

Pin No	Designation	Function
20	Vss	Supply pin, Ground.
40	Vcc	Supply pin, +5V
9	RST	Reset Input.
18,19	XTAL 1,XTAL 2	Crystal Input Pins.
29	PSEN	Program Store Enable.
30	ALE	Address Latch Enable.
31	EA	External Enable.
1 to 8	P1.0 to P1.7	I/O Pins Port1.

DUAL FUNCTION PINS (24 PINS)

Out of 32 I/O lines of four ports,8 lines of port 1 are used as single I/O function only. The remaining 24 pins of port 0, port2 and port 3 are used for dual functions. Port 0 pins used for I/O function and lower address and data multiplexed port for external memory. Port 2 pins used for I/O function and higher address for external memory. Port 3 pins used for I/O functions and alternative uses.

VCC

Pin 40 provides supply to the chip. The voltage source is +5v.

GND

Pin 20 is ground

RST

Pin 9 is RESET pin. It is an active high input pin and normally low. Upon applying a high pulse to this pin, 8051 terminate all activities and go to reset condition.

EA

Pin 31 is external enable pin(EA). When this pin is connected to VCC the CPU access internal memory. When EA pin connected to ground, the CPU access the program/data from external memory.

PSEN

This is an output pin. PSEN stands for Program Store Enable. An active low pulse in this pin enables the external ROM. This pin is connected to OE of external ROM chip.

ALE

This is an active high output pin.ALE stands for Address Latch Enable.ALE used to demultiplex the lower byte address of external memory and data from port 0. When ALE is high, port 0 is connected to external memory address latch. When ALE is low, port 0 carries the data.

ALU

The ALU performs the arithmetic and logic operations. The operations performed by ALU of 8051 are addition, subtraction, multiplication, division, logical AND, OR, EX-OR, Compare, Complement and left/right rotations. The registers A and B are used to hold the data during and arithmetic/logical operations. After an operation the result is stored in the A-register and the flags are set or reset according to the result of the operation.

PORT 0:

Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance inputs. Port 0 may also be configured to be the multiplexed low order address/data bus during accesses to external program and data memory. In this mode P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pull-ups are required during program verification.

PORT 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups Port 1 also receives the low-order address bytes during Flash programming and verification.

PORT 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pull-ups and

can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pull-ups when emitting 1s. The 8051 microcontroller is packaged in 40 pin Dual in line package (**DIP**).Out of 40 pins,16 pins are single function pins and 24 pins may be used for one or two entirely different function.

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Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

PORT 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pull-ups. Port 3 also serves the functions of various special features of the AT89C51 as listed below: Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

SPECIAL FUNCTION REGISTERS (SFR)

There are many special function registers are widely used in 8051 microcontroller. The SFR can be accessed by their names or by their addresses. For example, register A has address EO_H and register B has been designated as address FO_H. The special function registers addressed between 80_H and FF_H. Not all the address spaces to FF is used by the SFR. The unused locations 80H of FFH are reserved and must not be used by the 8051 programmer.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

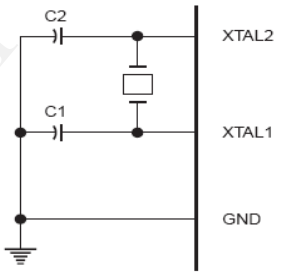
XTAL2

Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

OSCILLATOR CONNECTIONS

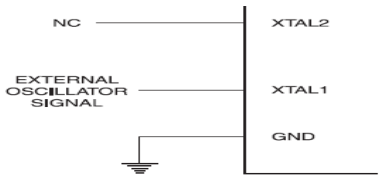


Idle mode

In idle mode, the CPU puts itself to sleep while all the on chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and the entire special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

EXTERNAL CLOCK DRIVE

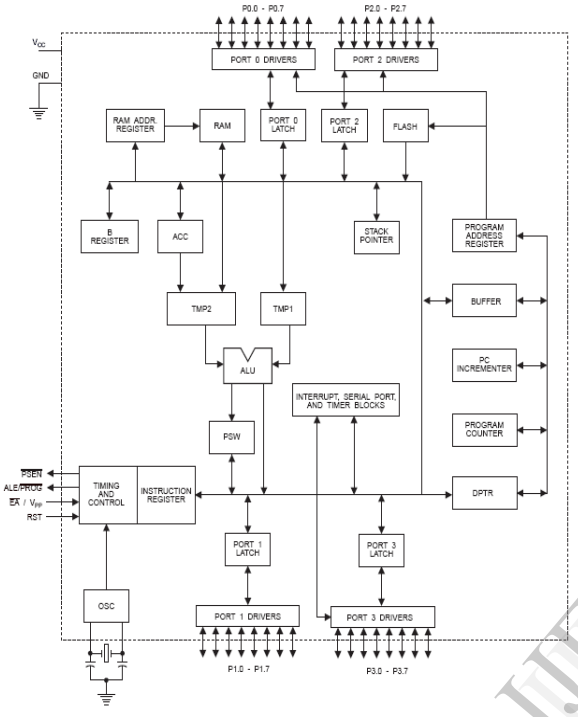
CONFIGURATION



Power-down mode

In the power-down mode, the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset.

4. BLOCK DIAGRAM



The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, five vector two-level interrupt architecture, a full duplex serial port, and on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next +hardware reset

PROGRAM MEMORY LOCK BITS

On the chip are three lock bits which can be left un-programmed (U) or can be programmed (P) to obtain the additional features listed in the table below. When lock bit 1 is programmed, the logic level at the EA pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of EA be in agreement with the current logic level at that pin in order for the device to function properly.

	Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

PROGRAMMING THE FLASH

The AT89S52 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (VCC) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers. The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

The AT89C51 code memory array is programmed byte-by byte in either programming mode. To program any nonblank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.

PROGRAMMING ALGORITHM

Before programming the AT89S52, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89S52, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise EA/VPP to 12V for the high-voltage programming mode.
5. Pulse ALE/PROG once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

DATA POLLING

The AT89S52 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

READY/BUSY

The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

PROGRAM VERIFY

If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

CHIP ERASE

The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/PROG low for 10ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

READING THE SIGNATURE BYTES

The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel

(031H) = 51H indicates 89C51

(032H) = FFH indicates 12V programming

(032H) = 05H indicates 5V programming

PROGRAMMING INTERFACE

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self timed and once initiated, will automatically time itself to completion. All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

SPECIAL FUNCTION REGISTERS

A map of the on-chip memory area called the Special Function

Register (SFR). Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

TIMER 2 REGISTERS

Control and status bits are contained in registers T2CON and T2MOD for Timer 2. The register pair (RCAP2H, RCAP2L) is the Capture/Reload registers for Timer 2 in 16-bit capture mode or 16-bit auto-reload mode.

INTERRUPT REGISTERS

The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the six interrupt sources in the IP register.

DATA MEMORY

The AT89C52 implements 256 bytes of on-chip RAM. The upper 128 bytes occupy a parallel address space to the Special Function Registers. That means the upper 128bytes have the same addresses as the SFR space but are physically separate from SFR space. When an instruction accesses an internal location above address 7FH, the address mode used in the instruction specifies whether the CPU accesses the upper 128 bytes of RAM or the SFR space. Instructions that use direct addressing access SFR space.

For example, the following direct addressing instruction accesses the SFR at location 0A0H (which is P2).

MOV 0A0H, #data

Instructions that use indirect addressing access the upper 128 bytes of RAM. For example, the following indirect addressing instruction, where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

MOV @R0, #data

Note that stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space.

TIMER 0 AND 1

Timer 0 and Timer 1 in the AT89C52 operate the same way as Timer 0 and Timer 1 in the AT89C51.

TIMER 2

Timer 2 is a 16-bit Timer/Counter that can operate as either a timer or an event counter. The type of operation is selected by bit C/T2 in the SFR T2CON (shown in Table 2). Timer 2 has three operating modes: capture, auto-reload (up or down counting), and baud rate generator. The modes are selected by bits in T2CON, as shown in Table 3. Timer 2 consists of two 8-bit registers, TH2 and TL2. In the Timer function, the TL2 register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency. In the Counter function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since two machine cycles (24 oscillator periods) are required to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. To ensure that a given level is sampled at least once before it changes, the level should be held for at least one full machine cycle.

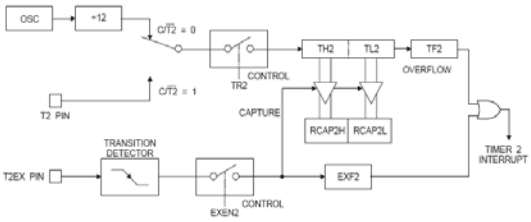
CAPTURE MODE

In the capture mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 is a 16-bit timer or counter which upon overflow sets bit TF2 in T2CON. This bit can then be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can generate an interrupt.

AUTO-RELOAD (UP OR DOWN COUNTER)

Timer 2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit located in the SFR T2MOD (see Table 4). Upon reset, the DCEN bit is set to 0 so that timer 2 will default to count up. When DCEN is set, Timer 2 can count up or down, depending on the value of the T2EX pin.

TIMER IN CAPTURE MODE:



Timer 2 automatically counting up when DCEN = 0. In this mode, two options are selected by bit EXEN2 in T2CON. If EXEN2 = 0, Timer 2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L. The values in Timer in Capture ModeRCAP2H and RCAP2L are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if enabled. Setting the DCEN bit enables Timer 2 to count up or down, as shown in Figure 3. In this mode, the T2EX pin controls the direction of the count. Logic 1 at T2EX makes Timer 2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively. Logic 0 at T2EX makes Timer 2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers. The EXF2 bit toggles whenever Timer 2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.

PROGRAMMABLE CLOCK OUT

A 50% duty cycle clock can be programmed to come out on P1.0, as shown in Figure 5. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed to input the external clock for Timer/Counter 2 or to output a 50% duty cycle clock ranging from 61 Hz to 4MHz at a 16 MHz operating frequency. To configure the Timer/Counter 2 as a clock generator, bit C/T2 (T2CON.1) must be

cleared and bit T2OE (T2MOD.1) must be set. Bit TR2 (T2CON.2) starts and stops the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L), as shown in the following equation

$$\text{Clock-Out Frequency} = \frac{\text{Oscillator Fequency}}{4 \times [65536 - (\text{RCAP2H,RCAP2L})]}$$

In the clock-out mode, Timer 2 roll-overs will not generate an interrupt. This behavior is similar to when Timer 2 is used as a baud-rate generator. It is possible to use Timer 2 s a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and clock-out frequencies cannot be determined independently from one another since they both use RCAP2H and RCAP2L.

UART

The UART in the AT89C52 operates the same way as the UART in the AT89C51.

INTERRUPTS

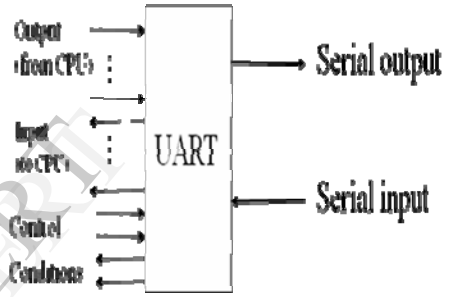
The AT89C52 has a total of six interrupt vectors: two external interrupts (INT0 and INT1), three timer interrupts (Timers 0, 1, and 2), and the serial port interrupt. These interrupts are all shown in Figure 6. Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once. Note that Table shows that bit position IE.6 is unimplemented. In the AT89C51, bit position IE.5 is also unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products. Timer 2 interrupt is generated by the logical OR of bits TF2 and EXF2 in register T2CON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and that bit will have to be cleared in software. The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle. However, the Timer 2 flag, TF2, is set at S2P2 and is polled in the same cycle in which the timer overflows.

UART (UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER)

1. A **universal asynchronous receiver/transmitter** (usually abbreviated **UART**) is a type of "asynchronous receiver/transmitter", a piece of computer hardware that translates data between parallel and serial forms. UARTs are commonly used in conjunction with other communication standards such as EIA RS-232.
2. A UART is usually an individual (or part of an) integrated circuit used for serial communications over a computer or peripheral device serial port. UARTs are now commonly included in microcontrollers. A dual UART or **DUART** combines two UARTs into a single chip. Many modern ICs now come with a UART that can also communicate synchronously; these devices are called **USARTs**.

ASYNCHRONOUS COMMUNICATION HARDWARE

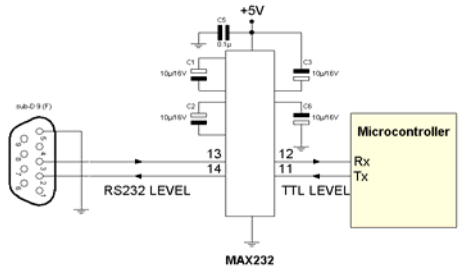
1. Data within a DTE is usually stored and moved in a parallel fashion.
2. Data sent across the channel is generally sent serially.
3. The parallel/serial conversion of data is done by a device known as UART (Universal Asynchronous Receiver / Transmitter).



5. INTERFACING THE SERIAL / RS232 PORT

AT command	Meaning
+CMGS	Send message
+CMSS	Send message from storage
+CMGW	Write message to memory
+CMGD	Delete message
+CMGC	Send command
+CMMS	More messages to send

The Serial Port is harder to interface than the Parallel Port. In most cases, any device you connect to the serial port will need the serial transmission converted back to parallel so that it can be used. This can be done using a UART. On the software side of things, there are many more registers that you have to attend to than on a Standard Parallel Port. (SPP)



6. GSM MODEM

General packet radio service (GPRS) is a packet oriented mobile data service on the 2G and 3G cellular communication systems **GLOBAL SYSTEM FOR MOBILE COMMUNICATIONS (GSM)**. The service is available to users in over 200 countries worldwide. GPRS was originally standardized by European Telecommunications Standards Institute (ETSI) in response to the earlier CDPD and i-mode packet switched cellular technologies. It is now maintained by the 3rd Generation Partnership Project (3GPP).

A GSM modem is a specialized type of modem which accepts a SIM card, and operates over a subscription to a mobile operator, just like a mobile phone. From the mobile operator perspective, a GSM modem looks just like a mobile phone.

When a GSM modem is connected to a computer, this allows the computer to use the GSM modem to communicate over the mobile network. While these GSM modems are most frequently used to provide mobile internet connectivity, many of them can also be used for sending and receiving SMS and MMS messages.

Due to some compatibility issues that can exist with mobile phones, using a dedicated GSM modem is usually preferable to a GSM mobile phone. This is more of an issue with MMS messaging, where if you wish to be able to receive inbound MMS messages with the gateway, the modem interface on most GSM phones will only allow you to send MMS messages. This is because the mobile phone automatically processes received MMS message notifications without forwarding them via the modem interface.

It should also be noted that not all phones support the modem interface for sending and receiving SMS messages. In particular, most smart phones, including Blackberries, I-Phone, and Windows Mobile devices, do not support this GSM modem interface for sending and receiving SMS messages at all at all. Additionally, Nokia phones that use the S60 (Series 60) interface, which is Symbian based, only support sending SMS messages via the modem interface, and do not support receiving SMS via the modem interface.

A wireless modem is a type of modem which connects to a wireless network instead of to the telephone system. When a mobile Internet user connects using a wireless modem, they're attached directly to the wireless ISP (Internet Service Provider) and can then access the Internet.

GSM SIGNALS
GSM MODEM OUT LOOK

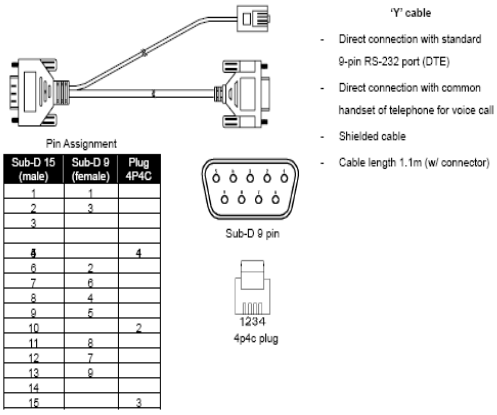
FEATURES OF GSM MODEM

1. Voice / Fax / SMS and Data
2. Quad Band 850 / 900 / 1800 1900 MHz
3. Accepts Standard SIM Card
4. Miniature size 88 x 60 x 26mm
5. Can Be Used On Standard GSM Network
6. RS232 Interface
7. One user programmable input / Output Port
8. GSM100T: TCP/IP stack available for data and internet
9. AT command set:
10. GSM 07.05 and 07.07 and WAVECOM
11. GPRS Class B Class 10:
12. 36Kbps download / 24Kbps upload

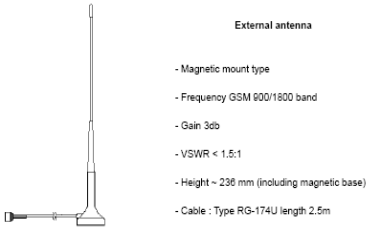
Compact "Plug And Play" Quad band GSM modems can be directly connected to the serial port of a desktop or notebook computer through the RS232 interface. A standard SIM card can be inserted in the integral card-holder within the metal enclosure.

The modems' metal casing makes it an appropriate solution for tough industrial applications such as Telemetry ,Wireless Local Loop (payphones) or as part of a fleet management system. The small size makes it simple to integrate in a space constraint environment. The modem is supplied with power cable. Other accessories available are an antenna (with 1m coax cable), RS232 connecting cable with Telephone interface, DIN Rail mounting adaptor and power supply unit.

GSM MODEM INTERFACE WITH PC



7.EXTERNAL ANTENNA



8. HARDWARE PROPERTIES

Devices which use serial cables for their communication are split into two categories. These are DCE (Data Communications Equipment) and DTE (Data Terminal Equipment.) Data Communications Equipment are devices such as your modem, TA adapter, plotter etc while Data Terminal

The electrical specifications of the serial port are contained in the EIA (Electronics Industry Association) RS232C standard. It states many parameters such as –

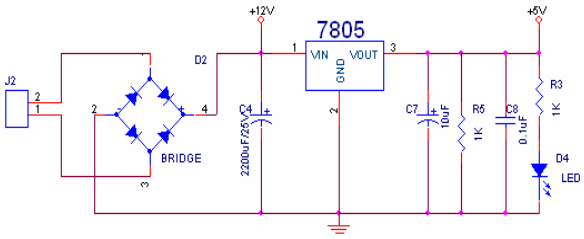
1. A "Space" (logic 0) will be between +3 and +25 Volts.
2. A "Mark" (Logic 1) will be between -3 and -25 Volts.
3. The region between +3 and -3 volts is undefined.
4. An open circuit voltage should never exceed 25 volts. (In Reference to GND)
5. A short circuit current should not exceed 500mA. The driver should be able to handle this without damage. (Take note of this one!)

It is interesting to note however, that the RS232C standard specifies a maximum baud rate of 20,000 BPS, which is rather slow by today's standards. A new standard, RS-232D has been recently released.

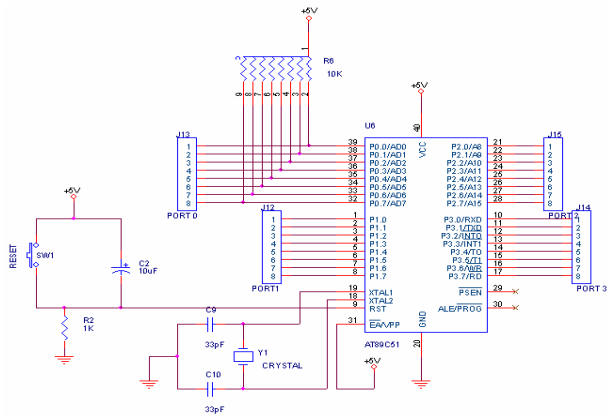
Serial Ports come in two "sizes", there are the D-Type 25 pin connector and the D-Type 9 pin connector both of which are male on the back of the PC, and thus you will require a female connector on your device. Below is a table of pin connections for the 9 pin and 25 pin D-Type connectors. Serial Pin outs (D25 and D9 Connectors)

D-Type-25 Pin No.	D-Type-9 Pin No.	Abbre-viation	Full Name
Pin 2	Pin 3	TD	Transmit Data
Pin 3	Pin 2	RD	Receive Data
Pin 4	Pin 7	RTS	Request To Send
Pin 5	Pin 8	CTS	Clear To Send
Pin 6	Pin 6	DSR	Data Set Ready
Pin 7	Pin 5	SG	Signal Ground
Pin 8	Pin 1	CD	Carrier Detect
Pin 20	Pin 4	DTR	Data Terminal Ready
Pin 22	Pin 9	RI	Ring Indicator

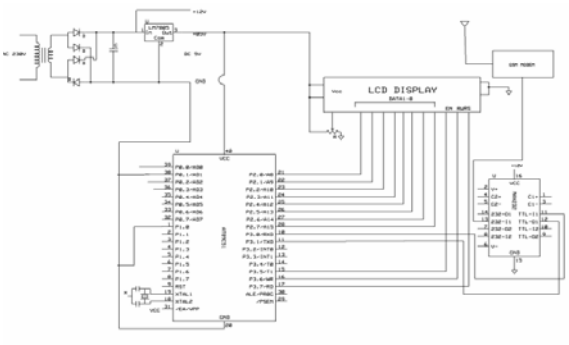
9. POWER SUPPLY DIAGRAM



10.MICROCONTROLLER INTERFACING DIAGRAM



11. OVER ALL CIRCUIT DIAGRAM



12. SOFTWARE REQUIREMENTS

1. Keil C Complier.
2. Embedded C Programming.

13. COMMERCIAL APPLICATION

The Salvos are easy to interface with existing ATM Machine. This makes profit to all the Bank ATM's care taker. By using this system we can include a technology that, taking photograph of cash withdrawer's at ATM'S center in JPG format and sends to Bankers and to the Users mail. In case of continuous trying to hack the ATM card of others, we can lock the door of that ATM center and provide minimum shock to the hacker through door by using RTOS as well as sends alert to the Bank care takers, nearby Police Station and ring Voice alarm in ATM center which helps to understand the situation by outside person.

14. CONCLUSION

The Salvos conclude that "Secure cash transaction is of serious concern in growing use of cash cards and internet transactions. Cash withdrawal cards, chip and pin facility is one of the facilities which have increasingly been used for business and social activities is done successfully with limited research focus on security and flexibility".

15. FUTURE RESEARCH

We are in research of implementing the Automatic ATM care system by " Keypad – Dialing".

Developing a Voice recognition instead of text message.

In case of emergency by setting the security questions which is very confidently the user can change the user mobile no in ATM Machine accordingly.

16. REFERENCE

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