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RTL-to-GDSII Implementation of a Fractional N-Pll

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Abstract: **- Phase-Locked Loops (PLLs) are fundamental mixed-signal components used in communication, radar, and clock-generation systems to generate low-jitter, frequency-stable signals. Conventional Integer-N PLLs, though robust, are limited in frequency resolution because their output step size is fixed by the reference frequency, preventing simultaneous achievement of wide tuning range and fine granularity required in modern RF applications. To address these limitations, this work implements a Fractional-N PLL architecture that decouples channel spacing from the reference frequency through fractional division. This approach enables fine frequency steps on the order of tens of kilohertz while maintaining wideband tunability, thereby improving spectral purity and resolution for radar systems. The design employs a mixed-signal methodology, integrating high-performance analog blocks with digitally assisted modulation and calibration techniques to meet stringent specifications for phase noise, area, and power.**

Key-Words: **- Fractional-N PLL, Ground Penetrating Radar (GPR), Delta-Sigma Modulator, Mixed-Signal Design, SCL 180 nm.**

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1 INTRODUCTION

A Phase-Locked Loops (PLLs) are essential mixed- signal building blocks used in modern communication, radar, and clock-generation systems. A PLL establishes a feedback mechanism in which a tunable oscillator aligns its phase and frequency with a stable reference signal, thereby producing a clean, low-jitter output. Conventional Integer-N PLL architectures, while simple and robust, inherently limit frequency resolution because the output frequency step size is directly constrained by the reference frequency. As a result, they are unable to simultaneously achieve wide tuning range and fine frequency granularity both of which are critical in advanced RF and sensing applications. To overcome these constraints, this work implements a Fractional- N-PLL architecture, which decouples the channel spacing from the reference frequency through fractional division techniques. This enables significantly finer frequency steps—on the order of tens of kilohertz— while maintaining wideband coverage. Such fine resolution is particularly important for reducing phase error, improving spectral purity, and enhancing radar system resolution. The proposed design follows a mixedsignal implementation strategy, integrating high-performance analog components with digitally controlled modulation and calibration blocks to meet stringent requirements on phase noise, area, and power.

2 LITERATURE REVIEW

Recent advancements in Recent advancements in Fractional-N PLL design have largely focused on improving noise performance, spur suppression, and power efficiency through innovations in divider architectures, charge-pump linearity, and digitally assisted control. A fourth-order MASH ΔΣ modulator is proposed in [1], providing improved noise shaping and significantly reduced fractional spurs with minimal area overhead. Practical implementation guidelines for Fractional-N synthesis are outlined in [2], highlighting techniques for spur mitigation and fine frequency tuning in real-world systems. Low-power multimodulus divider architectures introduced in [3] further enhance high-speed operation while reducing jitter contributions in the feedback path, making them well-suited for wide-tuning applications. In addition, a programmable charge-pump design presented in [4] improves linearity and jitter performance by enabling digitally controlled current adjustment and PVT compensation. Complementing these developments, a digitally assisted DTCbased Fractional-N PLL in [5] demonstrates fine time resolution, low in-band noise, and strong spur suppression through calibrated digital-to-time conversion. Collectively, these works indicate a clear trend in modern PLL research: the transition toward hybrid digital–analog architectures that leverage precise digital calibration to enhance analog linearity and stability. Techniques such as digitally assisted charge-pump tuning, advanced ΔΣ modulation, and DTC-based phase interpolation have

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contributed to substantial gains in spectral purity, jitter performance, configurability, and power efficiency. These advancements form the foundation for meeting the stringent requirements of next- generation wireless standards, high-speed serial links, and low-power communication systems.

3 PROPOSED SYSTEM ARCHITECTURE

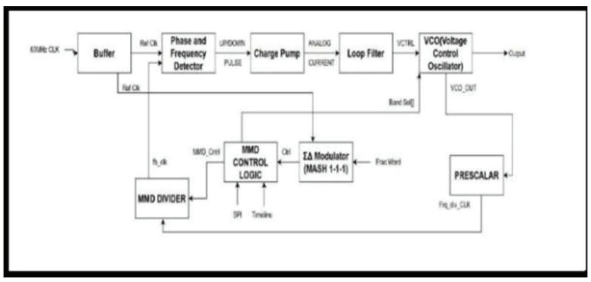

Fig. 1 Block Diagram

3.1 **Analog Subsystem**

a. Reference Buffer: Isolates the external 60 MHz crystal input to provide a clean reference clock.
b. Phase-Frequency Detector (PFD) & Charge Pump (CP): A dead-zone-free PFD drives a matched CP. The CP current is programmable to maintain constant loop dynamics across different frequency bands.
c. Loop Filter (LF): A passive filter design is optimized via MATLAB co-simulation to provide a tunable bandwidth between 100 kHz and 1 MHz.
d. Multi-Band LC VCO: To cover the wide 0.55 2.7 GHz range, a switched LC-VCO with four overlapping bands is employed. Coarse tuning is achieved via digital band selection, while fine-tuning uses varactor control

3.2 **Digital Subsystem**

a. Prescaler & MMD: A high-speed CML prescaler divides the GHz signal down for the Multi-Modulus Divider (MMD). The MMD supports programmable N/N+1division sequences.
b. Delta-Sigma Modulator: A MASH 1-1-1 digital modulator controls the MMD. It shapes quantization noise out-of-band to achieve the required resolution while suppressing spurious tones.
c. Control Logic: The system includes an SPI interface for FPGA communication, enabling atomic reconfiguration, band calibration, and lock detection.

4 PROPOSED METHODOLOGY

The project follows a rigorous RTL-to-GDSII mixed-signal flow:

1. Behavioural-Modelling: Initial verification uses Verilog-models to simulate loop dynamics, phase noise shaping, and lock times.
2. Analog Design (Virtuoso): The PFD, CP, Loop Filter, and Multiband LC VCO are designed in Cadence Virtuoso. The VCO is split into four cores to ensure coverage across PVT variations.
3. Digital Design (Genus): The MASH 1-1-1 modulator and MMD logic are synthesized in Cadence Genus. This includes the SPI registers and band-select FSM.
4. Physical Design: The final phase involves layout and signoff, including floor-planning to isolate sensitive analog blocks

5 DESIGN

5.1 Phase-Frequency Detector (PFD)

The PFD is implemented using a standard tri-state architecture. A critical non-ideality in conventional PFDs is the "dead zone," a region of negligible phase error where the detector fails to generate control pulses, essentially breaking the feedback loop and increasing low-frequency noise. To eliminate this, a programmable delay element is introduced into the reset path. This modification forces the PFD to generate minimum-width current pulses even when the phase error is zero, ensuring that the charge pump switches fully activate. This linearization technique guarantees that the loop remains closed and responsive to minute phase deviations, thereby improving the in-band phase noise performance.
The Phase-Frequency Detector (PFD) is implemented using a sequential logic architecture comprising two edge triggered D-Flip-Flops (DFFs) and an asynchronous reset path via an AND gate. This tri-state topology provides an extended detection range of $\pm 2\pi$ radians and frequency discrimination capabilities.

5.1.1 Dead Zone Analysis:

Ideally, the PFD transfer characteristic is linear across the detection range. However, a critical non-ideality known as the "dead zone" occurs near zero phase error ($\Delta \varphi \approx 0$). This phenomenon arises due to the finite rise and fall times of the

Charge Pump (CP) switches and the inertial delay of the internal logic.
Within this region, the generated UP and DOWN pulses are insufficient to fully turn on the CP switches, resulting in zero gain ($K\_PFD \rightarrow 0$). This opens the feedback loop, leading to increased low- frequency phase noise (jitter).
The theoretical PFD gain (K_PFD) in the linear region is defined by the Charge Pump current (I_CP): K_PFD = 1_CP/2π (A/rad)

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5.1.2 Delay-Based Linearization

To eliminate the dead zone, a programmable delay element is introduced in the delay path. This modification prevents the immediate resetting of the DFFs when both UP and DOWN outputs go high. Instead, it forces the generation of minimum-width coincident current pulses (t_min) even when the phase error is zero. The reset delay ensures that the pulse duration exceeds the switching threshold of the Charge Pump transistors. The condition for the minimum delay is given by:

$$\tau\_rst \geq t\_rise + t\_fall + t\_settling$$

Where, t_rise and t_fall are the switching times of the CP current sources.

Consequently, the transfer function is linearized around the origin, shifting the operation from the "dead zone" to a region of constant gain. The effective output current average (I_avg) becomes:

$$I\_avg = (I\_CP / 2\pi) \cdot \Delta \varphi$$

The Reset dominant path dictates that the total reset time must be less than half the reference period: $f\_max \leq 1 / (2 (t\_prop + \tau\_rst))$

Where t_prop is the inherent propagation delay of the DFFs and the AND gate. This design selects a programmable delay to satisfy equation while maximizing the operating margin defined in Equation.

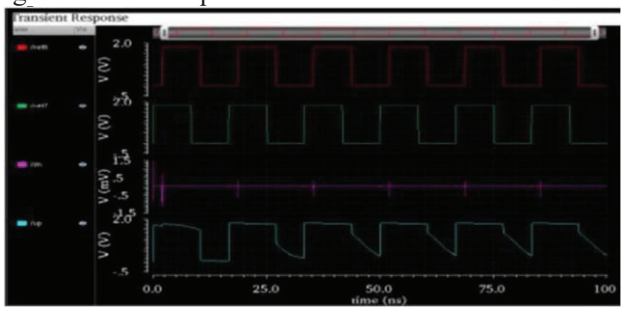

Fig.2 PFD Output

2.Charge Pump (CP): The charge pump utilizes a drain-switched topology to minimize charge injection errors. In Fractional-N architectures, any mismatch between the sourcing (Up) and the sinking (Down) currents manifests directly as periodic reference spurs at the output. Additionally, channel- length modulation can cause these currents to drift as the output voltage varies. To mitigate these effects, the design employs a high-swing cascode current mirror architecture supplemented by an active unity-gain feedback amplifier. This auxiliary amplifier forces the drain voltages of the current sources to track the output voltage, effectively boosting the output impedance and ensuring perfect current matching. Furthermore, the charge pump current is made digitally programmable. This allows the system to scale the gain in tandem with the division settings, compensating for loop gain variations without altering the passive filter components.

$$I\_(out)(t) = \begin{cases} +I\_(CP), & UP=1 \\ -I\_(CP), & DN=1 \\ 0, & \text{"otherwise"} \end{cases}$$

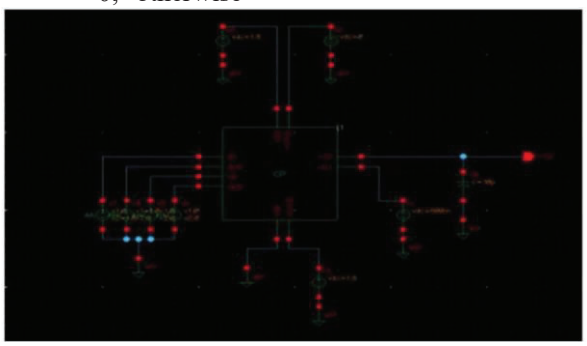

Fig.3 CP SCHEMATIC

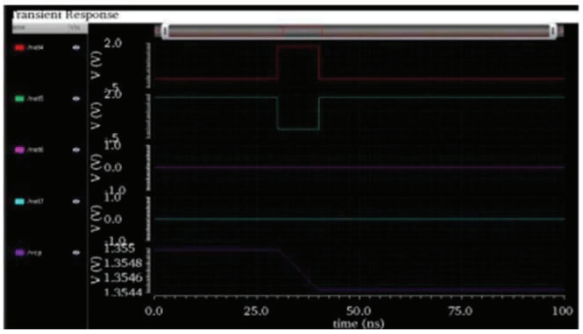

Fig.4 CP Output 1

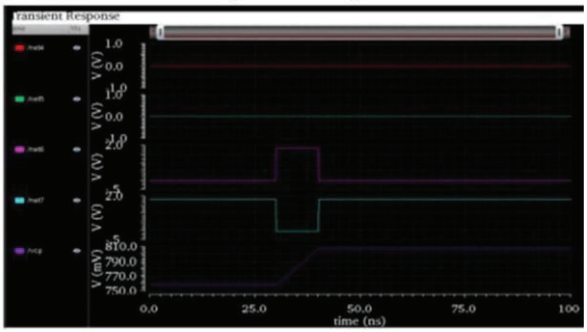

Fig.5 CP Output 2

2. Loop Filter (LF): A third-order passive loop filter is implemented to suppress reference spurs and attenuate the high-frequency quantization noise generated by the SigmaDelta modulator. The filter topology is critical for defining the closed-loop transfer function. The design challenge lies in the wide tuning range; as the frequency division ratio increases, the natural frequency of the loop typically degrades, leading to stability issues or slow locking. To maintain a constant loop bandwidth and a stable phase margin across all frequency bands, the filter impedance is co-designed with the programmable charge pump. By dynamically

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adjusting the charge pump current to offset changes in the VCO gain and division ratio, the loop dynamics are normalized, ensuring consistent settling time and jitter performance regardless of the operating frequency. 4.Wideband Multi-Core LC Voltage-Controlled Oscillator (VCO): To address the trade-off between the wide 5:1 tuning range (0.55 2.7 GHz) the design employs a Quad-Core Switched LC-VCO architecture. A single resonator would require excessive varactor range, degrading the tank Q-factor; partitioning the range into four optimized cores preserves Q and minimizes AM-to-PM conversion.

1. **Topology and Startup**: Each core utilizes a complementary cross-coupled NMOS- PMOS topology. This structure generates the differential negative resistance required to compensate for tank losses
2. **Dual-Mode Frequency Tuning**:
   a. **Coarse Tuning**: A **3-bit binary-weighted Switched Capacitor Array (SCA)** digitally steps the centre frequency. This centres the operation of the fine-tuning elements, preventing nonlinearities.
   b. **Fine Tuning**: Accumulation-mode MOS varactors, driven by the loop filter voltage provide the continuous tuning necessary for phase locking. This architecture ensures high spectral purity and mitigates frequency pushing by keeping the varactors in their linear region

The design of the LC-VCO for **Band-1 (0.55 GHz 1.018 GHz)** centers around an oscillation frequency of f0 = 0.81875 GHz. The core analysis involves the LC tank resonance, the required negative resistance for start-up, and the tuning sensitivity (KVCO).

A. Tank Resonator Design
The oscillation frequency is determined by the parallel resonance of the tank inductance (L) and the total capacitance (C_tot). Given a total capacitance of C_tot = 1.3 pF, the angular frequency is calculated as:
The required tank inductance is derived from the resonance condition
w0 = 1/ (LC_tot
L = 1 / (5.145 10^9)^2 (1.3 10^-12)
nearly 29.0 nH

To sustain oscillation, the energy loss in the tank, represented by the equivalent parallel resistance (Rp), must be compensated by the active core. Assuming a tank Quality Factor (Q) of 10, Rp is determined by

$$Rp = Q \cdot \omega_0 \cdot L$$

$$Rp = 10 \cdot (5.145 \times 10^9) \cdot (29 \times 10^{-9}) \approx 1492\ \Omega$$

For a differential cross-coupled pair, the small-signal negative conductance (G_neg) must satisfy G_neg ≥ 1/Rp. Since G_neg = gm/2, the critical transconductance (gm) is:

$$gm \geq 2 / Rp = 2 / 1492 \approx 1.34\ mS$$

This corresponds to a negative resistance magnitude of |R_neg| = 2/gm ≈ 1492 Ω, ensuring marginal startup. Assuming a transistor efficiency (gm/ID) of 10 V^{-1}, the required bias current per transistor is:

$$ID = gm / (gm/ID) \approx 134.1\ \mu A$$

C. VCO Tuning Sensitivity (KVCO)

The tuning sensitivity, or gain, is a function of the varactor sensitivity (dC/dV). With a sensitivity of 0.5 pF/V, the KVCO is approximated as:

$$KVCO = |df / dVdc| = (f_0 / 2\ C_{tot}) \cdot |dC / dV|$$

$$KVCO \approx (0.81875 \times 10^9 / (2 \cdot 1.3 \times 10^{-12})) \cdot (0.5 \times 10^{-12})$$

$$KVCO \approx 157.45\ MHz/V$$

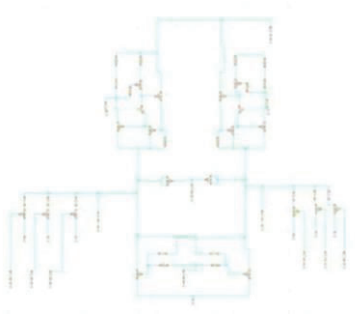

Fig.6 VCO SCHEMATIC

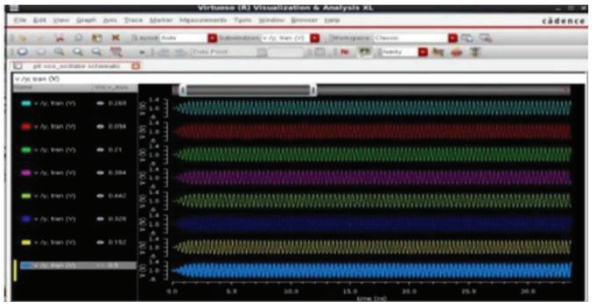

Fig.7 VCO Output

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Fig.8 VCO response -1

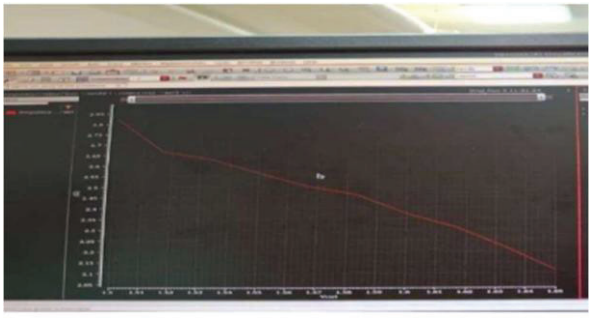

Fig.9 VCO response-2

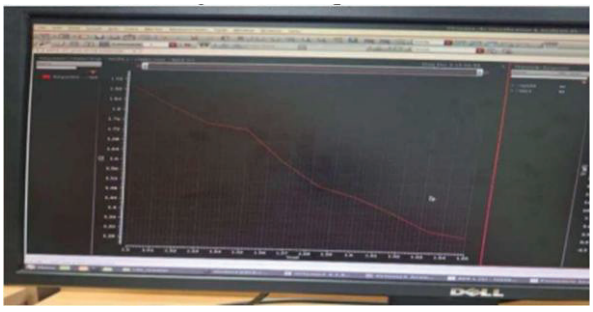

Fig.10 VCO response-3

5. MMD and Sigma-Delta Modulator

Precise frequency synthesis is achieved using a MultiModulus Divider (MMD) driven by a digital Noise-Shaping Modulator.

i) **MASH 1-1-1 Modulator:** This digital block utilizes a cascaded architecture to perform high-order noise shaping. It dithers the instantaneous division ratio to create a fractional average, pushing the resulting quantization noise power to higher offset frequencies. This high-pass noise shaping is essential, as it moves the noise energy into the stopband of the low-pass loop filter, preventing it from degrading the spectral purity of the carrier

ii) **Multi-Modulus Divider (MMD):** The divider is composed of a chain of dual-modulus cells capable of seamless switching. Unlike integer dividers that reset periodically, the MMD supports dynamic modulus control without introducing glitches or cycle slips. This allows the divider to respond instantaneously to the pseudo-random sequence generated by the modulator, enabling the fine frequency resolution required for the radar application.

iii)

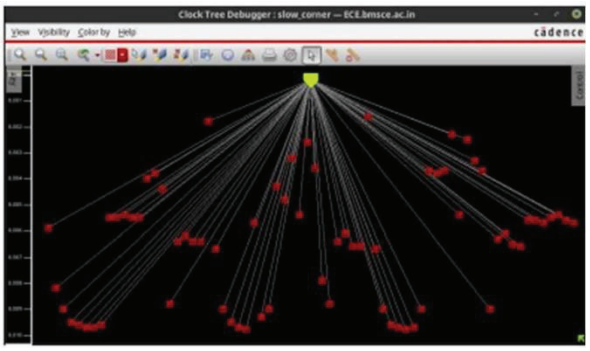

Fig.11 CLOCK TREE DEBUGGER

6 RESULT

The final result is obtained by the integration of all the design blocks.

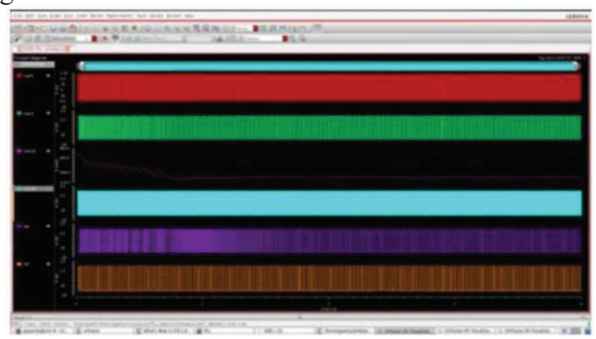

Fig.12 PLL OUTPUT

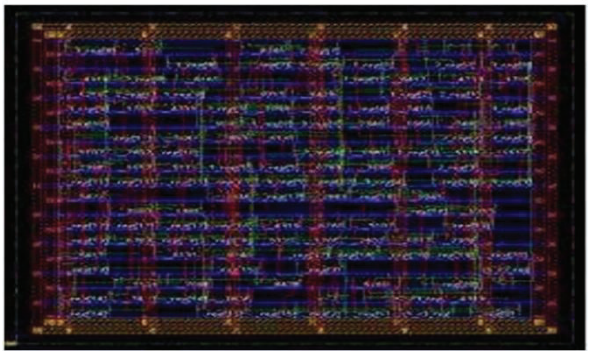

Fig.13 PLL LAYOUT

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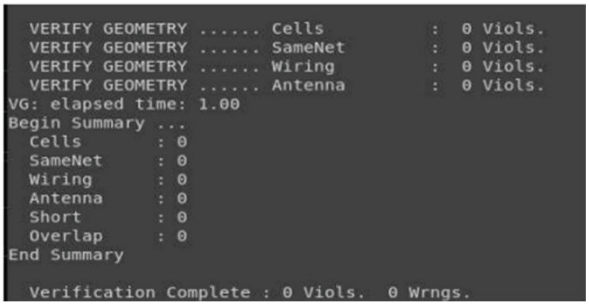

Fig.14 DRC VERIFIED

7 CONCLUSION

The design and implementation of the wideband Fractional- N PhaseLocked Loop developed in this work successfully address the stringent performance requirements of Ground Penetrating Radar (GPR) and other high-frequency RF applications. By integrating a quad-core switched LC-VCO, a high-order MASH 1-1-1 ΔΣ modulator, a programmable charge pump, and a high-speed multimodulus divider, **the proposed PLL achieves a tuning range of 0.55–2.7 GHz**, a fine frequency resolution of 40 kHz.These results indicate that the architecture is capable of generating spectrally clean and highly stable oscillation signals suitable for precision subsurface imaging and other wideband RF systems.

The mixed-signal design methodology—combining transistor-level analog circuitry with synthesized digital logic—was instrumental in achieving the required specifications. Behavioral simulations validated loop stability and the effectiveness of noise shaping, while **post-layout analyses confirmed that the design maintained both functional correctness and spectral performance** in the presence of parasitic effects. The **quad-core VCO architecture** ensured stable Q-factor characteristics and minimized KVCO- induced noise amplification, while the digitally programmable charge pump maintained consistent loop bandwidth across varying division ratios. Moreover, the combined operation of the MASH modulator and multi-modulus divider enabled high- resolution frequency synthesis without introducing deterministic fractional spurs, thereby ensuring robustness in both steady-state and transient conditions.

Overall, the implemented PLL demonstrates strong performance, stability, and flexibility, despite being realized in a mature **180 nm SCL CMOS technology**. The results validate the architectural choices and design strategies adopted throughout the development process, highlighting the effectiveness of digitally assisted analog techniques in modern frequency synthesizer design. This work not only meets its intended specifications but also establishes a solid.

This implementation demonstrates that a carefully optimized **RTL-to-GDSII flow can deliver the high-performance** frequency synthesis required for next-generation subsurface imaging systems

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