

Robust Low Leakage Controlled Keeper by Current Comparison Domino for Wide Fan in Gates

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Abstract

A new design for low leakage and noise immune wide fan-in domino circuits is presented. The proposed technique uses the between the leakage current the OFF transistors and the switching current of the ON transistors of the pull down network to control the PMOS keeper transistor, yielding reduction of the contention between keeper transistor and the pull down network from which previously proposed, techniques have suffered. Moreover, using the stacking effect leakage current is reduced and the performance of the current mirror is improved. Results of simulation in high performance 16nm predictive technology model (PTM) demonstrate that the proposed circuit exhibits about 39% less power consumption, and nearly 2.57 times improvement in noise immunity with a 41% die area overhead for a 64-bit OR gate compared to a standard domino circuit. Substantial increase in leakage current and threshold voltage fluctuations are making design of robust wide fan-in dynamic gates a challenging task. Robustness of high fan-in domino circuits is degraded by technology scaling due to exponential increase in leakage. Domino logic circuits with high fan-in are widely used due to their high performance. Scaling down the supply voltage is known to be the most effective way to reduce power consumption. For lower power supply voltage, the threshold voltage of transistors also needs to be scaled down to meet performance requirements. However, the lowering of the threshold voltage leads to an exponential growth of sub threshold leakage current.

Index terms — CMOSs & NMOS Domino Logic, Conditional Keeper Domino Logic Circuit.

1. INTRODUCTION

Wide fan-in domino logic has many applications in digital signal processors and high performance critical units of microprocessors. As technology is scaled down, power supply must be scaled to decrease power consumption. However, this leads to degradation of noise immunity because of lowering the switching threshold voltage. In the evaluation phase of the domino logic, the conventional problem is the inevitable leakage through the

pull down network (PDN), even when all the inputs are at the low logic level. This leakage is due to the BTBT (band-to-band-tunneling) current, gate tunneling current and the sub threshold current. In addition, voltages of dynamic nodes degrade to zero due to charges haring in the PDN yielding insufficient noise immunity. Use of NMOS transistors in the PDN with relatively high V_{th} has been proposed as a solution. However, increasing V_{th} increases the delay of discharging the dynamic node. Another proposed solutions to use a PMOS keeper. However, there is a speed degradation and power loss due to the contention between the pull down network and the strong keeper. Thus, performance of wide dynamic gates is affected by both sub threshold leakage and noise sources.

2 LITERATURE REVIEW

Several domino circuits have been proposed in the literature such as HS domino, Split Domino, CKCCD Domino, CKD Domino etc. The main goal of these circuit design techniques is improved noise immunity and circuit performance, especially in wide fan-in circuit.

2.1 CMOS & NMOS DOMINO LOGIC

Fig 2.1.1 & Fig 2.1.2 shows the implementation of an AND gate in both static CMOS and NMOS domino logic in which a full keeper is added to improve the robustness of the dynamic nodes. The keeper ratio K is defined as

$$K = \frac{\mu_p (W/L)_{\text{keeper}} - \text{transistor } \mu_n}{(W/L)_{\text{evaluation network}}}$$

where W and L denote the transistor size, and m_n and m_p are the electron and hole mobilities, respectively. Keeper transistor upsizing is a conventional method to improve the robustness of domino circuits. However, as the keeper transistor is up sized the contention between the keeper transistor and the evaluation network increases in the

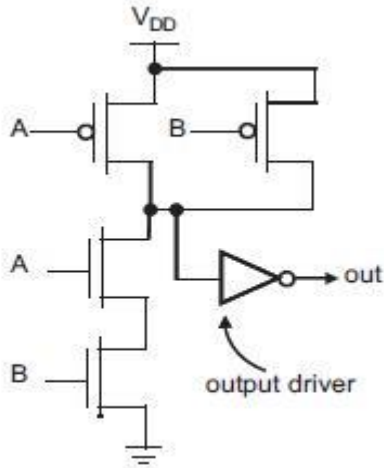


Fig 2.1.1 Implementation of an AND gate in CMOS

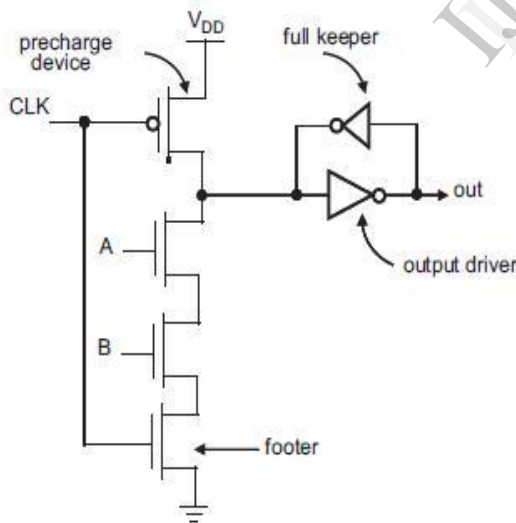


Fig 2.1.2 Implementation of an AND gate in NMOS domino logic

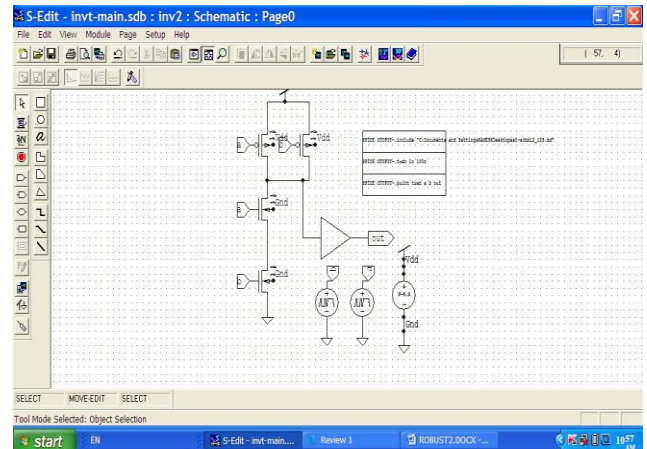
evaluation phase. This causes an increase in the evaluation delay of the circuit, increase in power consumption and degradation of performance. Therefore, to improve noise and leakage immunity, keeper upsizing is used as a compromise between delay and power. Several circuit techniques have been proposed in the literature to deal with this issue as described in Section 2. A new circuit design with controlled keeper by current-comparison domino (CKCCD) is proposed in this study. The main goal is to make the domino circuits more robust and with low leakage without significant performance degradation or increased power consumption.

The power consumption of a logic gate is given by,

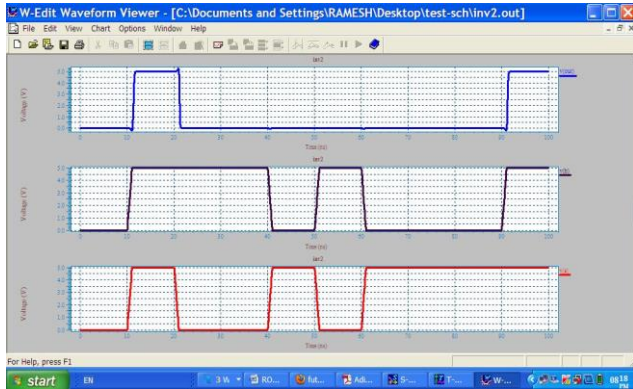
$$P_{avg/gate} = P_{switching} + P_{short-circuit} + P_{Leakage}$$

where $P_{switching}$ is the power consumed due to charging and discharging of the circuit capacitances, $P_{shortcircuit}$ is the power consumed due to the short circuit between V_{DD} and ground during output transitions and $P_{leakage}$ is the power consumed due to leakage current. The last term i.e. $P_{leakage}$ is dramatically increased with technology down scaling and increase in temperature, resulting in a reduction of leakage immunity and robustness. Therefore, it is very vital to reduce the leakage power of dynamic logic gates. In the proposed technique, conductance of the keeper transistor is controlled by comparison between the reference current and the evaluation network to improve the performance. The proposed technique improves leakage immunity using a footer transistor in diode-configuration.

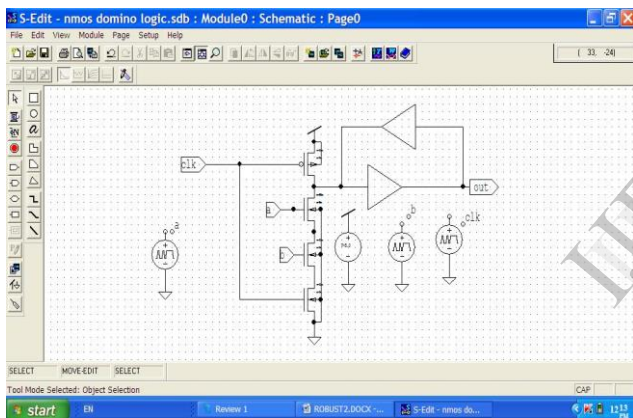
2.1.1 SIMULATION RESULT FOR CMOS



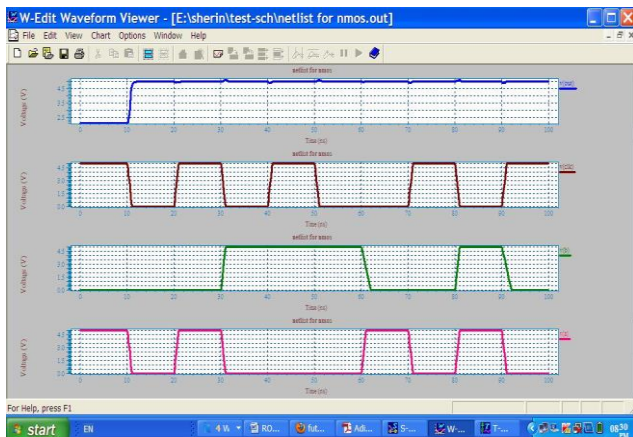
2.1.2 OUTPUT WAVEFORM FOR CMOS



2.2.1 SIMULATION RESULT FOR NMOS



2.2.2 OUTPUT WAVEFORM FOR NMOS



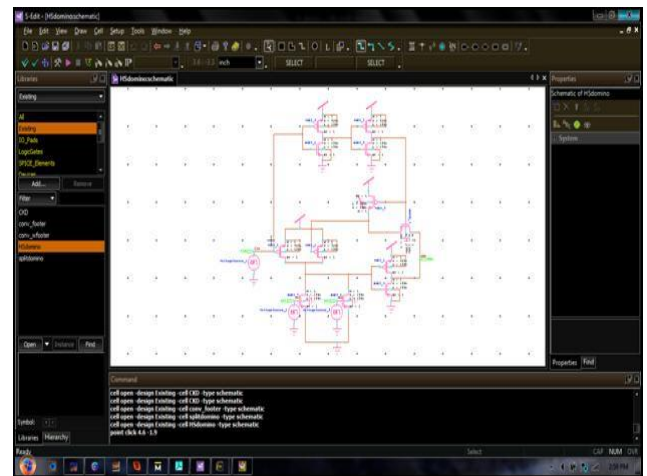
3. EXCISTING TECHNIQUES

3.1 HIGH SPEED DOMINO LOGIC CIRCUIT

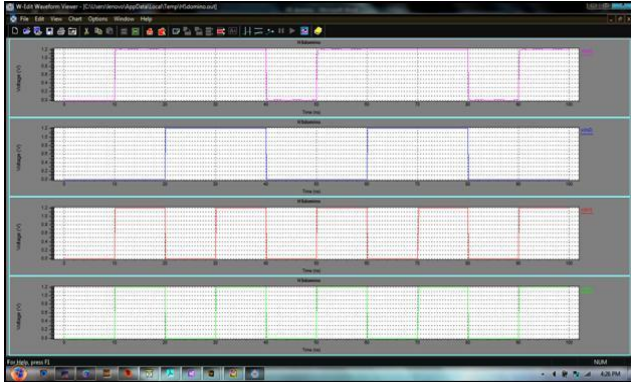
HS-Domino operates as follows: When the clock is LOW during precharge, the domino node is precharged to Vdd. Transistor Mn1 is OFF, P1 is ON charging the gate of the of the keeper transistor Q2 to Vdd, thus turning Q2 OFF. Q2 is therefore the beginning of ere OFF at the beginning of the evaluation phase. Contention is thus eliminated between the keeper and the pull-down devices during evaluation. Therefore, the domino gate evaluates faster and no contention current exists.

When the delayed clock becomes “1”, if the Domino node evaluates to “0” the gate output is “1”, and N1 is ON thus keeping Q2 OFF. If all the pull-down devices are OFF, the at Domino node stays “1”, Causing the gate output to be “0”, Which in turn discharges the keeper’s gate t, through N1. Therefore the keeper turns ON to maintain the voltage of the Domino node at Vdd and to compensate for any leakage currents. HS-Domino solves the contention problem by turning the keeper OFF at the start of the evaluation cycle. The keeper width can be sized up as Vth scales down to maintain a controlled NMOS without worrying about increasing the contention, and speed degradation.

3.1.1 SIMULATION RESULTS FOR HS DOMINO LOGIC



3.1.2 OUTPUT WAVEFORM FOR HS DOMINO LOGIC



3.2 SPLIT DOMINO CIRCUIT

The split domino gate achieves higher performance of operation through splitting the pull down devices into two networks. A logical 2-input NAND operation is utilized to generate the output. In this method the keeper device is split equally between the two networks. The main advantage of splitting the pull down network into two sections,

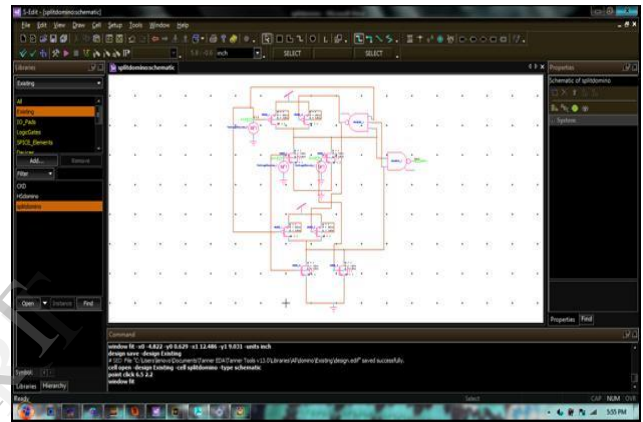
1. It is the reduction of the dynamic node capacitance and consequently faster evaluation.
2. The large keeper transistor in the conventional case is replaced by two devices each of which is nearly half the original keeper size leading to less contention.

The operation of the Split Domino circuit is:

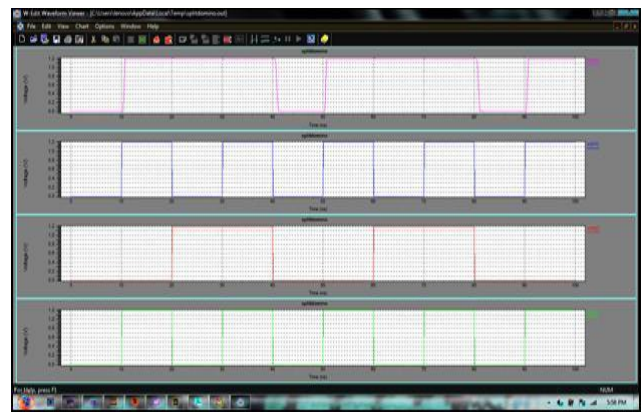
During precharge, CLK is LOW, the keeper devices are OFF and the output is LOW. At the onset of evaluation, the keeper devices remain OFF resulting in minimum contention. There are two different cases that need to be considered during the devices evaluation phase. When all inputs remain LOW and leakage current is at its maximum, the keeper devices controlled by the 3-input NAND gate are quickly activated to prevent the dynamic node from drooping and to keep output noise within the required limit

The 3-input NAND gate is skewed to allow for a very fast discharge of the keeper control signal in case all inputs remain LOW. The second case is any input goes HIGH, the corresponding dynamic node discharges very quickly due to decreased dynamic node capacitance and nearly keeps the keeper devices in the OFF state and contention is therefore minimized.

3.2.1 SIMULATION RESULTS FOR SPLIT DOMINO



3.2.2 OUTPUT WAVEFORM FOR SPLIT DOMINO



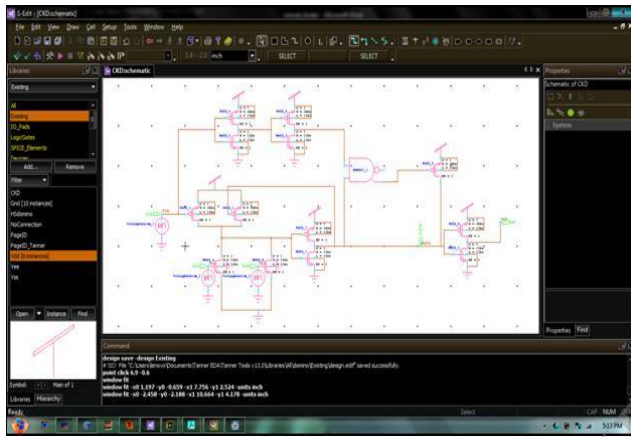
3.3 CONDITIONAL KEEPER DOMINO LOGIC CIRCUIT

The conditional keeper circuit works as follows:

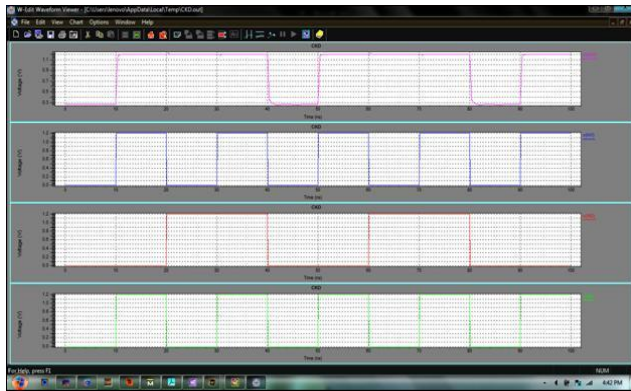
At the beginning of the evaluation phase, the smaller keeper (K1) is ON for keeping the state of the dynamic node. After delay of the inverters, if the dynamic

node is still high, the output of the NAND gate goes low to turn on K2. This keeper transistor is sized larger than K1 to maintain the state of the dynamic node for the rest of the evaluation period. The Conditional keeper remains off if the dynamic node is discharged to the ground. CKL logic has some problems like limitations on decreasing delays of the inverters and the NAND gate to improve noise immunity. Noise immunity can be improved by upsizing delay inverters, but this significantly increases power dissipation.

3.3.1 SIMULATION RESULTS FOR CKD



3.3.2 OUTPUT WAVEFORM FOR CKD

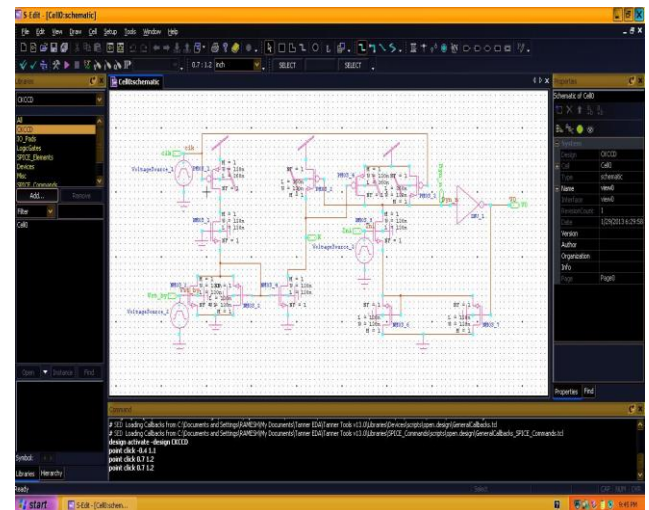


3.4 CONTROLLED KEEPER BY CURRENT-COMPARISON DOMINO (CKCCD)

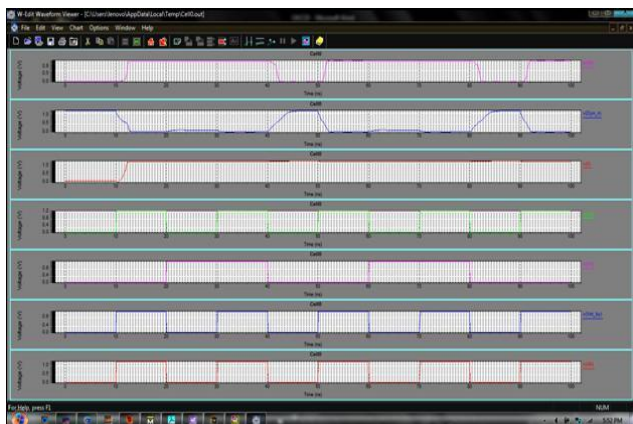
In Domino logic, the PMOS keeper must be upsized to increase the noise margin in the system. If the noise margin is 10% of V_{DD} then the PMOS keeper width can be sized to 10% of the worst case pull down width. But upsizing of keeper transistor leads to power consumption and the contention between the keeper transistor and the pull down network increases. These problems will be solved if the keeper transistor is OFF when the gate wants to pull down the dynamic node. But the voltage of the dynamic node is mainly decreased to zero in two different states: Either a conduction path to the ground is formed by the input vector or the leakage current of the pull down network with OFF transistors is increased that discharges the dynamic node due to the increased temperature or the existence of several parallel paths from the dynamic node to the ground. The keeper transistor should not turn off in the latter state. The current in the former state is more than the other. Therefore, the only way to distinguish between the two states is use of a reference current, which corresponds to the pull down network leakage and the temperature of the chip.

In the proposed circuit, the reference current is compared with the pull down network current. If there is no conducting path from the dynamic node to the ground and the only current in the pull down network is the leakage current, the keeper transistor will not turn off because the reference current is greater than the leakage current.

3.4.1 SIMULATION RESULTS FOR CKCCD



3.4.2 OUTPUT WAVEFORM FOR CKCCD



There is a race between the pull down network and the reference current. The current, which is greater than the other wins the race and turns off its keeper PMOS transistor. Transistor M_{pre2} is removed to discharge node K and thus turning on the keeper transistor in the precharge phase. This results in improved noise immunity.

3.5 PROPOSED CONTROLLED KEEPER BY CURRENT COMPARISON DOMINO

In Domino logic, the PMOS keeper must be upsized to increase the noise margin in the system. If the noise margin is 10% of V_{DD} then the PMOS keeper width can be sized to 10% of the worst case pull down width. But upsizing of keeper transistor leads to power consumption and the contention between the keeper transistor and the pull down network increases. These problems will be solved if the keeper transistor is off when the gate wants to pull down the dynamic node. But the voltage of the dynamic node is mainly decreased to zero in two different states: either a conduction path to the ground is formed by the input vector or the leakage current of the pull down network with OFF transistors is increased that discharges the dynamic node due to the increased temperature or the existence of several parallel (leakage) paths from the dynamic node to the ground. The keeper transistor should not turn off in the latter state. However, the current in the former state is more than the other. Therefore, the only way to distinguish between the two states issue of a reference current, which corresponds to the pull down network leakage and the temperature of the chip. In the proposed circuit, the reference current is

compared with the pull down network current. If there is no conducting path from the dynamic node to the ground and the only current in the PDN is the leakage current, the keeper transistor will not turn off because the reference current is greater than the leakage current. This idea is conceptually illustrate din Fig. 3.5.1

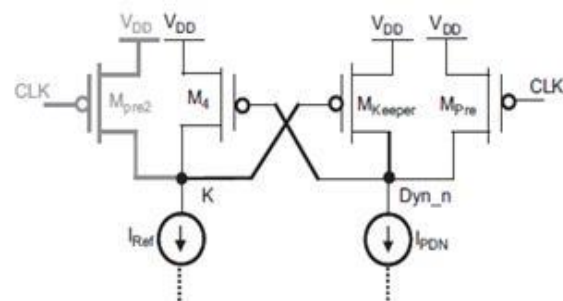
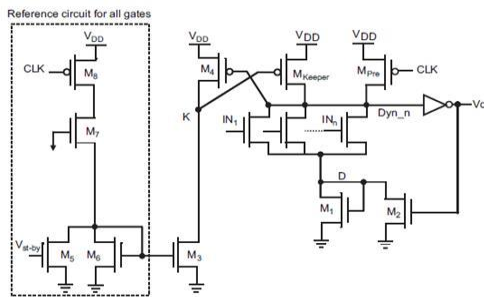


Fig 3.5.1 Concept of the proposed domino circuit

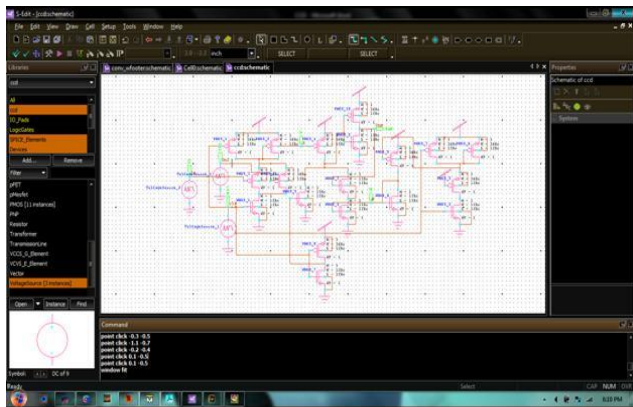
In fact there is a race between the pull down network and the reference current. The current, which is greater than the other wins the race and turns off its keeper PMOS transistor. Transistor M_{pre2} is removed to discharge node K and thus turning on the keeper transistor in the precharge phase. This results in improved noise immunity. Therefore, unlike circuit designs such as HS domino in which the keeper transistor is off at the beginning of the evaluation phase, the keeper transistor is on in this design. The proposed domino circuit is shown in Fig. 4.1.2 In this circuit M_1 is added in series with the evaluation network such as the wide OR gate, as illustrated in this schematic. Moreover, M_1 is added in a diode configuration to provide more leakage current reduction when all in puts in the OR gate area the low level or the circuit is set in the standby mode. Addition of M_1 results in a reduction of the sub threshold leakage of the evaluation network due to the stacking effect. The voltage drop across M_1 due to the leakage current decreases the sub threshold leakage in the following ways. First, it makes the gate to source voltage of the evaluation transistors negative. Second, it increases the body effect and the threshold voltage of the evaluation transistors. Third, it decreases the drain to source voltage and DIBL of the evaluation transistors. Therefore, the leakage power of the proposed circuit is decreased especially in standby mode. Since the leakage current of the pull down network is considerably low, a minimum keeper size is sufficient. However, increasing the keeper size increases the noise immunity especially

In wide OR gates with fan-in of more than 32inputs. Moreover, increasing the ratio of W3/W6 increases the reference current resulting in increased noise immunity. However, decreasing the ratio of W keeper/W4 increases the speed. The circuit of the reference leakage current consists of transistors M5, M6, M7 and M8. ThetransistorM5 is off in active mode and will be on in standby mode to reduce standby power. The size of themirrortransistorM3 is chosen based on the leakage of the pull down transistors. The mirror current must be greater than the pull down leakage and smaller than the minimum PDN discharge current with at least one input at the high logic level to ensure correct operation. Since the reference circuit is a replica circuit of the PDN, the reference current varies with temperature just like the PDN leakage current. Thus, the design is almost insensitive to temperature variations. The two phases of the proposed circuit in active mode are explained as follows:

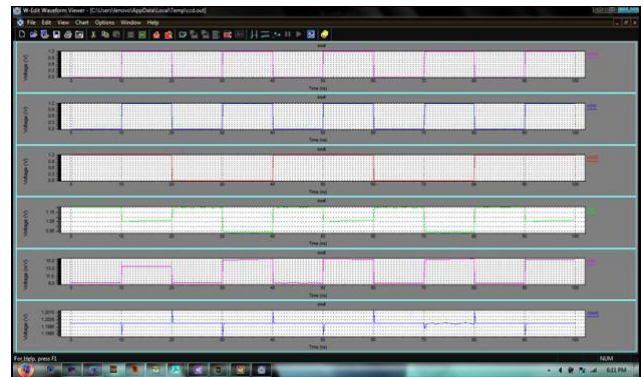


4.1.2 Proposed domino circuit

3.5.1SIMULATION RESULTS FOR CCD



3.5.2 OUTPUTFORM FOR CCD



3.6 PRECHARGE PHASE

In the precharge phase, clock voltage is in lowlevel (CLK¼'0' in Fig. 10). Hence, transistors Mpre, M keeper and M8 are onandM1 and M2 are off. Therefore, the voltage of the dynamic node (Dyn_n) is raised to the high level by transistor Mpre. In this phase, the leakage current is decreased due to the stacking effect since the minimum voltage of a MOS transistor in diode configuration is equal to $V_{gs}¼V_{ds}¼V_{tn}$, where V_{tn} is the NMOS threshold voltage.

3.7 EVALUATION PHASE

In the evaluation phase, clock voltage is in the high level (CLK¼'1' in Fig. 10), so the transistors such as Mpre and M8 are turned off. Depending on inputs levels, the other transistors may be turned on. According to the discharging current of PDN and the mirror current, two states may occur. The gate voltage of the keeper transistor depends up on which current is greater than the other. Then due to the positive feedback consisting of M4 and Mkeeper, the voltage of node K is determined. First, if all inputs are in low level, the mirror current is greater than the PDN leakage current, the voltage of node K is discharged to zero. Therefore, the keeper transistor is turned on and maintains the dynamic node at a high level. Second, if atleast one in put is at a high level, the discharging current of PDN is higher than the mirror current, yielding the voltage of node K to remain high. This reduces the contention problem by turning off the keeper transistor with any great change in the current of the NMOS pull down network rather than the mirror current. M2 is a small auxiliary transistor to pull down the footer node (node D

in Fig. 10) and reduce the delay due to the stacking effect of the NMOS evaluation transistors and M1. Therefore, the main idea in this circuit is that the keeper transistor is controlled with current comparison so that when the dynamic node is truly discharged, the keeper transistor will be off to prevent the contention current between the keeper and the PDN. Thus, the dynamic power and the propagation delay are reduced. Also, the short circuit power of the output inverter due to the glitch current is reduced, which relaxes the sizing constraints on the output inverter. As result, when compared to some implementations smaller sized output inverters can be used (from which some technique suffer). Moreover, leakage power is decreased as a result of the stacking effect. It must be considered that the consumed silicon area is not increased significantly compared with other domino circuits since the size of the added transistor in this design is small. In addition, the size of the output inverter and the keeper transistor can be smaller than the other existing circuit techniques. The proposed circuit has a low leakage current when all inputs are at the low level and meets the high robustness requirements of wide gates. This is because of the existence of a DC voltage in the sources of the evaluation network transistors, due to the diode configuration of saturated transistor M1 whose gate-source voltage is equal to its drain-source voltage. Therefore, the threshold voltage of the evaluation network transistors is increased according to Eq.(5)

$$V_t = V_{t0} + \gamma (\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s})$$

where V_{sb} is the voltage of source to bulk, $\phi_s = \frac{1}{4} \frac{2nT}{In} NA = n_i$ is the surface potential at threshold and γ is the body effect.

3.8 PROPOSED CURRENT COMPARISON BASED DOMINO CIRCUIT (CCD)

Since in wide fan-in gates, the capacitance of the dynamic node is large, speed is decreased dramatically. In addition, noise immunity of the gate is reduced due to many parallel leaky paths in wide gates. Although upsizing the keeper transistor can improve noise robustness, power consumption and delay are increased due to large contention. These problems would be solved if the PDN implements logical function, is separated from the keeper transistor by using a comparison stage in which the current of the pull-up network (PUN) is compared with

the worst case leakage current. In Fig 3(a), which utilizes the PUN instead of the PDN. In fact, there is a race between the PUN and the reference current. Transistor MK is added in series with the reference current to reduce power consumption when the voltage of the output node has fallen to ground voltage.

An important issue in the generation of the reference voltage, which is the correct variation of the reference current according to the process variations to maintain the robustness of the proposed circuit. Process variations are due to random and systematic parameter fluctuations. In random variations, parameters of each device vary individually and independent of adjacent devices. However, systematic variations affect the parameters of neighborhood transistors in the same way, yielding a strong correlation between parameters of nearby devices. In this paper, systematic variations are considered. We have assumed that in a given circuit design the threshold voltage of all nMOS transistors varies together and that of pMOS transistors varies together. In the proposed circuit, effects of any threshold voltage variation on the voltage of nodes A and B [in Fig. 3(b)] is important because it directly affects the speed of the gate, and consequently power consumption and noise immunity. The worst scenario is that the threshold voltage of nMOS transistors is decreased and that of the pMOS transistors is increased, i.e., fast nMOS and slow pMOS due to process variations. In the former case, the subthreshold leakage of pMOS transistors of the PUN is decreased, thus the reference current must be reduced and vice versa for the latter case. Therefore, the reference current must be varied according to threshold voltage variations to maintain robustness in this design. To track process variations in dynamic logic circuits, several solutions are proposed in the literature by using a process variation sensor, such as one based on drain-induced barrier lowering (DIBL) effect, rate sensing keeper, and replica keeper current. In the proposed circuit, a replica circuit like that proposed by can be used as a leakage current sensor for proper operation and superior performance, in the worst case of fan-in, i.e., a64-input OR gate because of its maximum leakage current

among other gates.

The proposed circuit for generation of reference current for all gates is shown in Fig. 3(b). This circuit is similar to a replica leakage circuit proposed by [1], in which a series diode-connection transistor $M6$ similar to $M1$ is added. In fact, as shown in Fig. 3(b), this circuit was a replica of the worst case leakage current of the PUN to correctly track leakage current variations due to process variations. Therefore, the gate of transistor $M7$ is connected to VDD, and its size is derived from the sizes of pMOS transistors of the PUN in the worst case, i.e., a 64-input OR gate, and hence its width is set equal to the sum of the widths of 64 pMOS transistors of the PUN. In the proposed CCD circuit, as shown in Fig. 3(b), current of the PUN is mirrored by transistor $M2$ and compared with the reference current, which replicates the leakage current of the PUN. The topology of the keeper transistors and the reference circuit, which is shared for all gates, is similar to that proposed in [1] which successfully tracked the process, voltage and temperature variations. The proposed circuit employs pMOS transistors to implement logical function, as shown in Fig. 3(b). Using the N-well process, source and body terminals of the pMOS transistors can be connected together such that the body effect is eliminated. By this means, the threshold voltage of transistors is only varied due to the process variation and not the body effect. Moreover, utilizing pMOS transistors instead of nMOS ones in the N-well process, it is possible to prevent increasing the threshold voltage due to the body effect in existence of a voltage drop due to the diode configuration of transistor $M1$, yielding decreasing the delay.

In other words, one can use nMOS transistors in the P-well process to achieve a higher speed due to their higher mobility. Although slower mobility of pMOS transistors decreases the speed, decreasing the capacitance of the dynamic node in the proposed circuit enables it to increase speed by proper choice of the mirror ratio M [see (2)]. As shown in Fig. 3(b), the proposed circuit has five additional transistors and a shared reference circuit compared to standard footless domino (SFLD). The proposed circuit can be considered as two stages.

The first stage preevaluation network includes the PUN and transistors M_{Pre} , M_{Eval} , and $M1$. The PUN, which implements the desired logic function is disconnected from dynamic node unlike traditional dynamic logic circuits, and indirectly changes the dynamic voltage. The second stage looks like a footless domino with one input [node A as input in Fig. 3(b)], without any charge sharing, one transistor $M2$ regardless of the implemented Boolean function in the PUN, and a controlled keeper consists of two transistors. Only one pull-up transistor is connected to the dynamic node instead of the n -transistor in the n -bit OR gate to reduce capacitance on the dynamic node, yielding a higher speed.

The input signal of the second stage is prepared by the first stage. In the evaluation phase, thus, the dynamic power consumption consists of two parts: one part for the first stage and the other for the second stage.

As we know the dynamic power consumption directly depends on the capacitance, voltage swing, and contention current on the switching node in the constant condition for frequency, power supply, and temperature. The first stage with n -input has a lower voltage swing VDD to V_{THP} and no contention. On the other hand, the second stage has rail-to-rail voltage swing with minimum contention. Although the proposed circuit has some area overhead, it has less dynamic power consumption compared to footless domino.

Transistor $M1$ is configured in diode connection, i.e., its gate and drain terminal are connected together. In the evaluation mode, the current of the PUN transistors establishes some voltage drop across $M1$. This voltage will be low, if all inputs are at the high level and only leakage current exists in the PUN and mirror transistor $M2$. Otherwise, if at least one conductive path exists between node A and ground, for example, level of one input becomes low in the OR gate, this voltage drop is raised up, turning on mirror transistor $M2$ and changing the output voltage.

The voltage drop across transistor $M1$ causes the gate-source voltage of the off transistors in the PUN to become positive, yielding an exponential reduction in sub threshold leakage due to the phenomenon called the stacking effect. It should be noted that if the body effect is not eliminated due to the unequal voltage of the source and body terminals, the leakage current will be decreased further at the expense of higher deviation due to process variations.

The voltage across the diode footer in other domino circuits that use diode-footed techniques such as [1] must be decreased to zero in order to lower the dynamic node voltage to zero. But in the proposed circuit, it is not necessary for this voltage to reach 0 V since the current of the diode

footer is needed instead of the voltage across it. Therefore, the size of the diode-footer transistor $M1$ in the proposed circuit is smaller than other DFD circuits. Consequently, a lower leakage current must be compensated by the keeper transistors instead of the larger one in the other circuit due to the larger size of the footer and mirror transistors. This results in lower delay and power consumption and area overhead. On the other hand, in the next precharge mode, the dynamic node is charged from nonzero voltage to power supply voltage, yielding reduction in the power consumption with respect to existence of the large capacitance on the dynamic node in wide fan-in gates, especially wide fan-in OR gates. In addition, since transistor $M1$ increases the switching threshold voltage of the pMOS transistors, the new switching threshold voltage of the gate is about twice the threshold voltage of the pMOS devices.

Since upsizing of transistor $M2$ increases the speed, the mirror ratio M is defined as the ratio of the size of transistor $M2$ to the size of transistor $M1$

$$M = (W/L)M2 / (W/L)M1$$

With reference to the circuit schematic shown in Fig. 3(b), two phases of the proposed circuit are explained in detail as follows.

A. Precharge Phase

Input signals and clock voltage are in high and low levels, respectively, [CLK = "0", CLK = "1" in Fig. 3(b)] in this phase. Therefore, the voltages of the dynamic node (Dyn) and node A have fallen to the low level by transistor $MDis$ and raised to the high level by transistor $Mpre$, respectively. Hence, transistors $Mpre$, $MDis$, $Mk1$, and $Mk2$ are on and transistors $M1$, $M2$, and $MEval$ are off. Also, the output voltage is raised to the high level by the output inverter.

B. Evaluation Phase

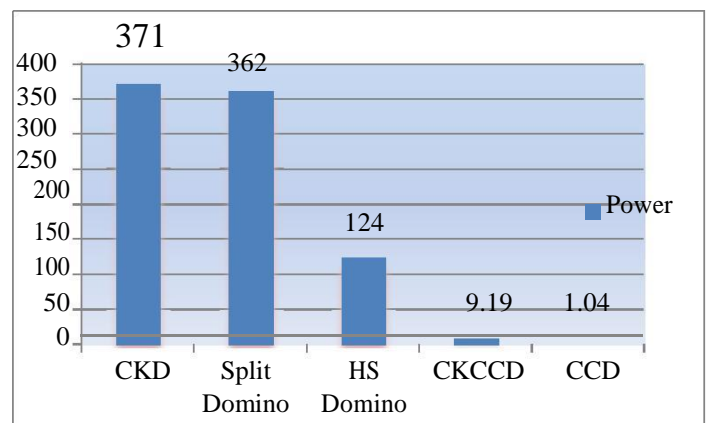
In this phase, clock voltage is in the high level [CLK = "1", CLK = "0" in Fig. 3(b)] and input signals can be in the low level. Hence, transistors $Mpre$ and $MDis$ are off, transistor $M1$, $M2$, $Mk2$, and $MEval$ are on, and transistor $Mk1$ can become on or off depending on input voltages. Thus, two states may occur. First, all of the input signals remain high. Second, at least one input falls to the low level. In the first state, a small amount of voltage is established across transistor $M1$ due to the leakage current. Although this leakage current is mirrored

by transistor $M2$, the keeper transistors of the second stage ($Mk1$ and $Mk2$) compensate this mirrored leakage current. It is clear that upsizing the transistor $M1$ and increasing the mirror ratio (M) increase the speed due to higher mirrored current at the expense of noise-immunity degradation. In the second state, when at least one conduction path exists, the pull-up current flow is raised and the voltage of node A is decreased to nonzero voltage, which is equal to gate-source voltage of the saturated transistor $M1$. This voltage is also equal to drain-source voltage of $M1$ and depends on size of $M1$ and its current. Increasing the pull-up current increases the mirrored current in transistor $M2$, thus voltage of the dynamic node Dyn is charged to VDD, yielding discharging the voltage of the output node and turning off the main keeper transistor $Mk1$. By this technique the contention current between the keeper transistor and the mirror transistor is mitigated.

3.9 COMPARISON TABLE

S.No.	Domino Circuit	Power	Delay
1	Split Domino	362 - Micro Watt	540 PS
2	CKD	371 - Micro Watt	14.4 PS
3	HS Domino	124 - Micro Watt	86.61 PS
4	CKCCD	9.19 Micro Watt	7.71 NS
5	CCD	1.04 Micro Watt	10.02 NS

3.10 GRAPH



4. CONCLUSION

A new leakage and noise tolerant domino logic circuit called Controlled Keeper by Current-Comparison Domino (CKCCD) is proposed. The main idea in this technique is that the keeper is controlled to decrease contention and yield a high performance using current comparison between the leakage current due to the low level inputs and the current due to at least one input at high level.

Several existing circuit designs and the proposed design were simulated with HSPICE in the 16-nm high performance V2.1 technology of PTM model at a power supply of 0.8 V and wide fan-in 8 to 64-bit OR gate circuit is used as a benchmark.

Results of simulations show that the proposed circuit technique exhibits from 29% to 39% less power consumption and from 1.86 to 2.57 times improvement in noise immunity for 8 to 64-bit OR gates at the cost of from 36% to 74% more die area consumption compared to the standard footless domino design, respectively.

Moreover, a normalized figure of merit (FOM) that includes die area, power, delay and UNG is defined. The proposed circuit demonstrated FOM's of 1.36, 1.85, 2.46 and 2.87 times their counterparts in footless domino OR gates for 8, 16, 32 and 64-bit OR gates, respectively. Therefore, the proposed circuit is superior to existing designs that were studied in detail in this paper, especially for wide fan-in gates.

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