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Reliability Enhancement of Low Power TSPC Flip Flop

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***Abstract*— In a True single-phase clocking flip-flop (TSPC FF), a logic structure reduction scheme is employed to reduce the number of transistors for achieving reduced power and delay. Despite its circuit simplicity, no internal nodes are left floating during the operation to avoid leakage power consumption. A pulsed latch has an advantage of reduced clock power and leakage power. They provide an alternative sequential element with high performance and low area and power consumption, taking advantage of both latch and flip-flop features. An integration of both Logic structure reduction flip flop (LRFF) and a pulsed circuit is proposed. In circuit implementation, transistor sizes are optimized with respect to the power delay product (PDP). Flip flops such as Adaptive coupled flip flop (ACFF) and Topologically compressed flip flop (TCFF) are also integrated with pulsed circuit, then a comparison analysis is done with integrated LRFF. PVT analysis has been done for all the three pulse integrated flip flops and also parameters analysis such as setup time, hold time, power, delay, Area and PDP was analyzed, from that integrated pulse LRFF was found better.**

Keywords—Complementary pass-transistor logic; flip- flop (FF); low power; true single-phase clocking (TSPC) ; pulsed flip-flops.

I. INTRODUCTION

Flip flops consumes more power due to the presence of clock system, so measures were taken to reduce the load on clock system. Reduced clock swing flip flop was one method implemented earlier to decrease the clock power with respect to other flip flops. By using this method clock systems voltage swing was reduced [7]. Reduced swing technique was used in differential conditional capture flip flop to reduce the clock load, but in this flip flop both low swing and full swing clock signals are given as enable signal [6]. Since power was not reduced as expected, therefore many flip flops such as differential discharge flip flop, differential pre-charge flip flop, pulse triggered flip flops and so on were introduced by reducing the circuit complexity. To decrease the switching activity of the flip flops conditional capture and pre charge techniques were used. In paper [8] it discusses about many parameters such as setup time, hold time, D-Q delay and C-Q delay. Many logic structures such as HLFF, SDFF, SSTC, DSTC, Power PC 603 and so on were compared using different parameters such as PDP, internal power, Transistor count, and all timing parameters. Now-a-days the applications based on battery are increasing which leads to increase in performance and decrease in power. Sequential circuits are built up of latches and flip flops. Similarly, by using master and slave latches flip flops was built. Data might be lost when we are using flip flops, so to detect the delay fault probability of a flip flop an enhanced scan flip flop was implemented. Enhanced scan flip flop (PESFF) is an enhancement of PFF. A comparison analysis of PESFF and PFF was done, from the analysis it was noticed that there was great decrease in power and also less affected by process variations [3]. Clock skew and clock jitter are the two timing parameters of clock distribution network. Different clock distribution networks were introduced in [11] and a comparison analysis is made among them. Issues of low power designs and power consumption also have been discussed. Transmission gates were used for the implementation of the flip flops, thus it not only reduces the stray capacitances.(acf) Earlier in the case of Transmission gate flip flops (TGFF) as shown in the Fig 1 there was an increase in work load, so to overcome this disadvantage an True single phase clocking scheme(TSPC) was introduced.

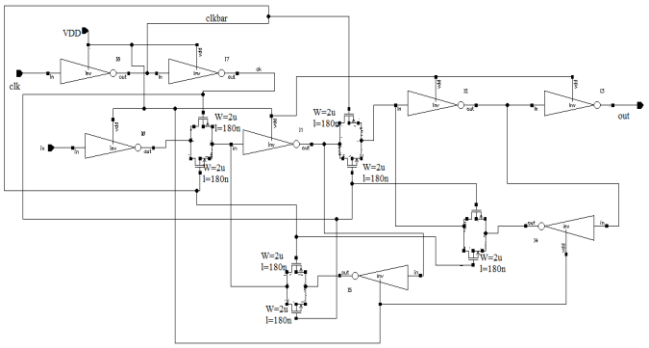

Fig 1 Transmission gate flip flop

TSPC consists of Adaptive coupled flip flop, Topologically compressed flip flop (TCFF), and Logic structure reduction flip flop. Transistor count of TSPC FF'S was reduced when compared to TGFF. In the case of ACFF as shown in Fig 2, instead of Transmission gates PMOS and NMOS are used, hence power consumption was decreased to a great extent.

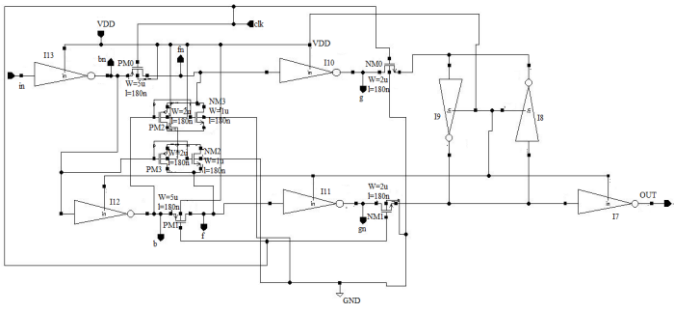

Fig 2 Adaptive coupled flip flop

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The structure of ACFF is similar to differential latch structure, due to the presence of weak PMOS transistors in the master latch it is very difficult for the transition to take place when there is a change in input. ACFF consists of two adaptive coupled elements (ACE), each adaptive coupled elements consists of one NMOS and PMOS transistors in parallel. These adaptive coupled elements make the transition easier, but its power consumption is high when data switching activity increases and also large setup time due to the presence of adaptive coupled elements [9]. When process variations analysis is done, Transmission gates in ACFF are affected and also it has clock skew issues when same clock is given at a time to all the transmission gates. Another TSPC FF implemented was TCFF as shown in Fig 3, TCFF is more prone to process variations when compared to ACFF. Earlier TCFF consists of 28 transistors, later on the transistor count was reduced to 21 by merging of both PMOS and NMOS transistor as shown in Fig 4 .

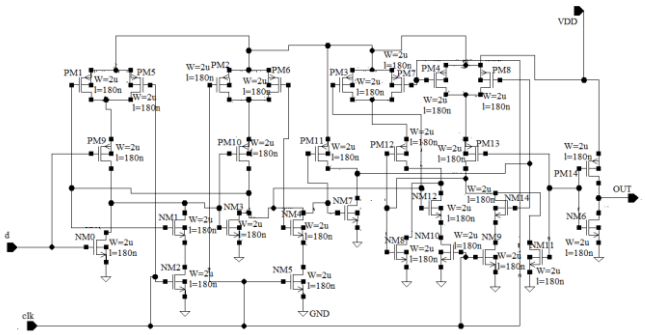

Fig 3 Topologically compressed flip flop (28 transistors)

Even though many PMOS and NMOS transistors were shared, performance of the circuit was not affected. Clock load and power dissipation of TCFF circuit was also reduced, but it has a disadvantage of large setup time [10].To overcome the disadvantage of TCFF Logic structure reduction flip flop (LRFF) was introduced which will be discussed later. A pulsed latch circuit was integrated with LRFF, thus performance of the circuit is less effected depending upon the pulse width obtained from the pulsed latch circuit. A MUX based pulsed latch circuit was implemented, thus the pulse produced from the circuit will help to obtain the correct operation under different process voltage temperature variations (PVT).

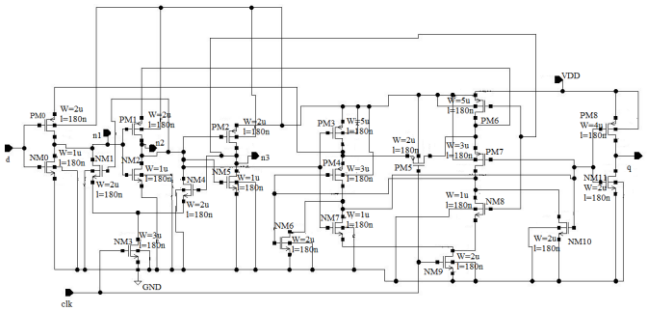

Fig 4 TCFF (21 Transistors)

II. PREVIOUS WORKS ON PULSED LATCHES

Pulsed latches were introduced to reduce the clock skew, jitter and power consumption in the circuit. It also enhances the performance of the circuit. Earlier, PVT analysis was made to ensure the performance of the circuit, from that pulse width of the circuit was so designed that it should not be too large or narrow. Depending on the pulse width of the circuit appropriate outputs are obtained. Several failure cases of the pulsed latch circuits were discussed depending on latch write time and pulse width [4]. A pulse is obtained by using delayed clock and inverted clock signal as shown in Fig 5. By appropriately changing the w/l ratios of the inverters we can control the pulse width of the circuit. For different voltages, temperature and process corners, pulsed latches circuit were designed properly to ensure the performance with less power and area. Hold time issues was one of the major disadvantages of pulsed-latches. To overcome this hold time issues, delay buffers were inserted in the circuit.

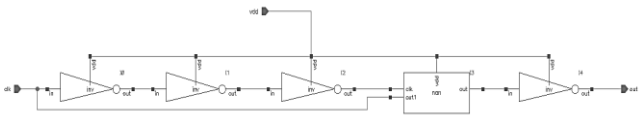

Fig 5 Simple pulse generator

A pulse generator was implemented with minimum 0.42 V. When input crosses a critical value of input NAND gate, then a pulse is generated. This level-detecting feature provides a wider operating window over a NIC across all of the PVT corners. We have called this circuit a DYSKL pulse generator [12]. A pulse latched circuit was introduced instead of flip flop for an ASIC design to reduce the timing problem, and also many advantages was discussed in [15].

A. Mux based pulsed latch

Pulses with non-identical widths was produced using a Mux based pulsed latch circuit as shown in Fig 6. Delay units are so selected depending upon the variations in supply voltage. For different delay units different transparency windows was produced. Case of failure condition was avoided by using small transparency window, so careful design of inverters was done such that proper pulse width was obtained without any failure. The size of the inverters at both the input and output of the NAND gate are so chosen to ensure the reliability of the circuit when the supply voltage is scaled down and at nominal supply voltage. Ctrl signal is used as select line for a 2:1 Mux; it chooses the appropriate pulse width for the circuit [1].

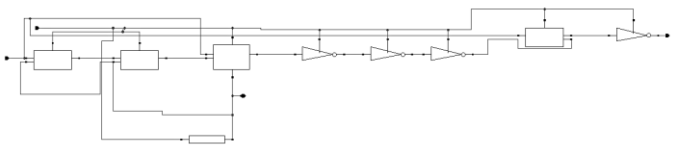

Fig 6 Mux based pulsed latch

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III. LOGIC STRUCTURE REDUCTION FLIP FLOP

LRFF is an enhancement of TCFF. It overcomes the disadvantage of TCFF by decreasing logic structure, floating case condition and power consumption of the circuit. In the case of LRFF as shown in Fig 7, it uses Complementary pass transistor logic (CPL) thus reduces the transistor count by two. Clock controlled PMOS (PM4) was connected between two nodes e and f to ensure that whether the supply voltage is reaching these two nodes, thus acting as an pseudo VDD nodes. These pseudo VDD nodes are controlled by the signals X2 and X3 which is given as input to PMOS transistors (PM2 & PM5). After hold time, if there is any change in input then data stored in master latch does not enter the slave latch, since both PM1 & NM3 are turned off thus floating case problem was avoided. When clk=0 PMOS transistors connected to clock turns on, then both nodes e & f are connected to VDD and the master latch is in data input mode. Initially when data= 0 or 1 and clk=0, then data is stored in master latch and slave latch holds the previous value, since clk controlled NMOS transistors are turned off. Later, when clk=1 all the NMOS transistors connected to clk turns on and the data is send from master latch to slave latch, thus the corresponding output is produced depending upon the change in data and clock signal [2].

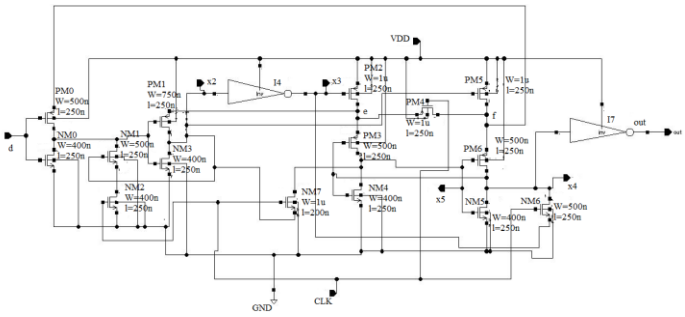

Fig 7 LRFF

A. *Integrated Mux Based Pulsed Latch LRFF*

Both MUX based pulsed latch and LRFF are integrated together as shown in Fig 8 so that reliability of the circuit is enhanced for different process voltage temperature variations. A comparison analysis is made with both Integrated TCFF and ACFF and was found that LRFF is best among them. Area occupied by integrated pulsed latch LRFF is less when compared with other two flip flops.

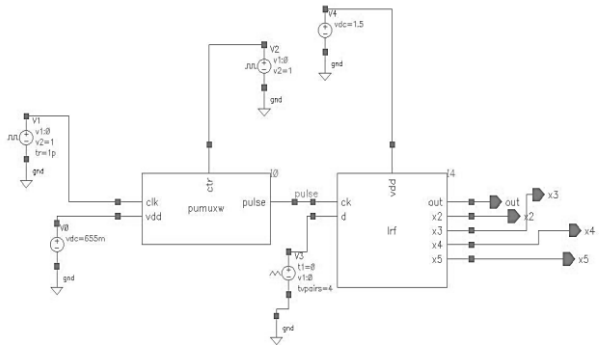

Fig 8 Integrated mux based pulsed latch LRFF

IV. PROCESS VOLTAGE TEMPERATURE VARIATIONS

The effect of operation of TSPC FF's was performed at different process, voltage and temperature variations depending upon the pulse width which is given as clock to the flip flops. Reliability of the circuit was ensured by performing PVT analysis at different corners. The main purpose to do PVT analysis was to find out which circuit is functioning better among TSPCFF.

A. *Process corner variations*

Now-a-days since the size of the devices are reduced to a large extend, any change during manufacturing process may lead to variations in parameter and the circuit operation fails [5]. It also helps to find the problem in operation of the circuit due to variation in many parameters, thus appropriate solutions was given to the circuit to ensure the correct operation for many parameter variations in the circuit. Process variations depends on some parameters such as Random dopant fluctuation, effective length variation and so on, leads to transistors change in threshold voltage and thus effects power of the circuit [14]. Process variation is done to ensure that the pulse width obtained by the pulsed latch is not too narrow or large, such that data is transmitted properly without any distortion. At different process corners such as Fast NMOS Fast PMOS (FF), Slow NMOS Slow PMOS (SS), Slow NMOS Fast PMOS (SF) and Fast NMOS Slow PMOS (FS) analysis of flip flops was done to identify at which corners the circuit is having a failure case problem.

B. *Voltage variations on TSPCFF*

Voltage variations were done to understand that up to which voltage a circuit works properly without any distortion. Scaling of voltage leads to decrease in power but delay might increase, so a proper trade of must be made between power and delay. Voltage variations are performed by considering three cases such as low voltage, nominal voltage and high voltage and other parameters such as power, delay, PDP was calculated to analyse how the variations affected the circuit. Earlier in the case of pulsed latch circuits the reliability of the circuit was little affected at lower supply voltage, so to overcome this problem a Mux based pulse latch circuit was designed so that the circuit would operate at different voltages without any degradation in performance. The timing overhead and hold time issues were reduced by using Mux based pulsed latches when compared other pulsed latches.

C. *Temperature variations*

Earlier a tool named a Temperature- and Reliability- Aware Memory Design (TRAM) approach to understand the effects of supply voltage, frequency, power dissipation and temperature. A mathematical model was also introduced to analyse the effects of temperature and supply voltage on performance of memory, since as frequency increases both error probability and dynamic power increases [13]. Temperature variations are performed carefully since each circuit works only at its specific environmental condition; we have to identify the range at which each circuit works properly by using parametric analysis. Temperature might affect performance, power and some data might get lost while varying the range of temperature. By varying the temperature it might affect the pulse width of Mux based pulse latch. Generally all the circuits are simulated at nominal temperature, to analyse the variations in output at different temperatures such as high and low temperature

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cases, thus worst case performance of a circuit can also be analysed. All the three integrated flip flops was analysed at different temperature and was found that integrated LRFF was found better.

V. PVT AND PARAMETER ANALYSIS

Process voltage temperature analysis was performed on Integrated LRFF, Integrated TCFF, and Integrated ACFF and the PVT analysis table is shown below. From the Table I & II shown below all the three flip flops are varied at different voltage, process and temperatures. Power and delay of three flip flops for each voltage variations was calculated by using cadence tool and also PDP was analysed. From the Table I we can say that PDP of Integrated LRFF is less and thus Integrated LRFF is better than other two flip flops. Process variations at different corners such as FF, SS, FS, SF were performed and thus were found that Integrated LRFF was better than other two flip flops. From the Table II Integrated LRFF works at FF, SS, and FS but were as in the case of other two flip flops they are not much reliable. Temperature variation analysis Table II demonstrates that for large temperature variations was not affecting the reliability of Integrated LRFF when compared to both Integrated TCFF and ACFF. Thus by looking at the analysis Tables I & II, we can say at which conditions or corners the circuit is not working.

TABLE I: Voltage variations

	Voltage variations	Vdd= 0.9	1	1.4	1.5	1.6
Integrated LRFF	Power (uw)	37.32	39.02	49.90	53.20	57.84
	Delay (ns)	48.67	15.87	7.24	0.0886	0.0533
	PDP (pws)	1.82	0.619	0.361	0.0047	0.0031
Integrated TCFF	Power (uw)	Distorted	13.61	27.24	33.17	40.33
	Delay (ns)	Distorted	58.05	59.06	59.98	105.64
	PDP (pws)	Distorted	0.79	1.61	1.99	4.26
Integrated ACFF	Only for V_{dd} =0.6 , Power=31.97uw, Delay=26.97ns					

TABLE II: Temperature & Process variations

	Temperature	Process variations				
Integrated LRFF	Working at (-70 to 70)	Nominal	FF	SS	FS	SF
		Yes	Yes	Yes	Yes	No
Integrated TCFF	Working at (-35 to 40)	Yes	Yes	No	Yes	No
Integrated ACFF	Working at (-25 to 30)	Yes	Yes	No	No	No

The parameter such as setup time, hold time and Area was analysed using parameter analysis in cadence tool. For setup time and hold time analysis clk-to-Q delay and D-to-Q delay was analysed from the waveform and also Area was calculated from layout, thus parameter analysis was done. From the parameter analysis Table III, conclusion was made that integrated LRFF was better than other two flip flops.

TABLE III: Parameter analysis

	SETUP TIME(ns)	HOLD TIME(ns)	AREA
Integrated LRFF	2.81	3.03	159.41
Integrated TCFF	34.39	3.078	186.885
Integrated ACFF	13.21	3.057	224.12

VI. RESULT AND DISCUSSION

The Fig 9 and Fig 10 are the pre-layout and post-layout simulations of Integrated LRFF. Layout was obtained as shown in Fig 11 based on following rules such as DRC, LVS and QRC. Post-layout simulation was done and later on it was converted to GDSII file

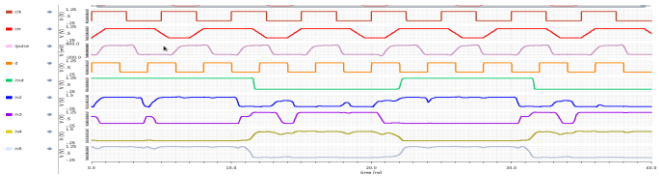

Fig 9: Pre-layout simulation

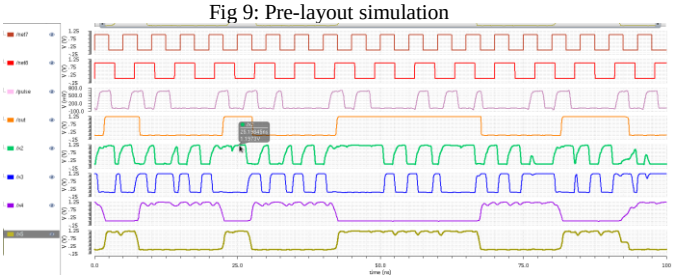

Fig 10: Post-layout simulation

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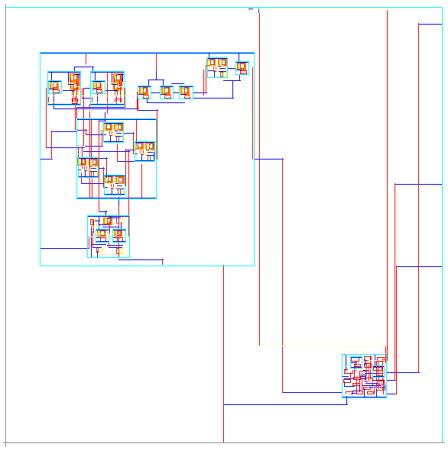

Fig 11: Layout of LRFF

VII. CONCLUSION

Complexity of the LRFF is reduced when compared with other two flip flops. Pulsed latch circuits have been introduced to generate pulses. By integrating this pulse latch circuit with LRFF we can improve the performance of the circuit. Parameters such as power, delay, PDP, setup time and area of all three flip flops were evaluated, from that Integrated LRFF was found better among all. PVT analysis was performed to ensure the reliability and robustness of the flip flops. Unnecessary timing overhead was also avoided.

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