Reduction of Partial Products for Vedic Multiplier

Mr. Sunil Patel
Dept. of Electronics And Communication
G.H.Patel college of Engineering And technology
Vallabh Vidhyanagar, India.

Prof. Deepak Parashar
Dept. of Electronics And Communication
G.H.Patel college of Engineering And technology
Vallabh Vidhyanagar, India.

Abstract— **Multiplier is one of the most important components of many high performance digital systems. And also it is one of the most power consuming and time consuming component of the digital systems. So optimization of multiplier is very important in process of making system fast and power efficient.**

This paper present multiplier based on Vedic method "Urdhava Tiryakbhyam" Method which is also known as "vertically and crosswise" method. This multiplier used 2x2multiplier blocks as basic building block. This paper suggest multiplier of 8x8 multiplier we should use 2x2 multiplier in place of 4x4 multiplier. As we have to many partial product with using 2x2 multiplier it look very complex and timely process of adding it. But adding the numbers in method describe in this paper make it simpler. QUARTUS tool is used for simulation and time analysis.

Keywords— *Vedic multiplier; Reduction of partial products; vertically and crosswise; Urdhava Tiryakbhyam Multiplier; 8x8 multiplier.*

General Terms— *Vedic multiplier= vertical and crosswise multiplier or Urdhava multiplier*
CSA= carry save adder

I. INTRODUCTION

Multiplication is one of the most used processes in digital systems and processors. Also it required plenty of adder and partial product generators. It can be said that multiplication is one of most time consuming and power consuming process. Due to this it is necessary to optimize the multiplier before finalizing any digital design.

Vedic multiplication techniques are simple formulae which can be used for solving number of different types of mathematical problems. This paper shows design of 8x8 multiplier "Urdhava Tiryakbhyam".

In this design 16 parallel 2x2 multiplier blocks are used as partial product generator. Then partial product is reduced to 7 using reduction. This remaining seven numbers are then added accordingly to find the product of the two numbers.

II. URDHAVA TIRYAKBHYAM

The Urdhava Tiryakbhyam is also known as vertically and crosswise. In this method partial product are simultaneous generated using partial product generators. And then they are added vertically and crosswise. This

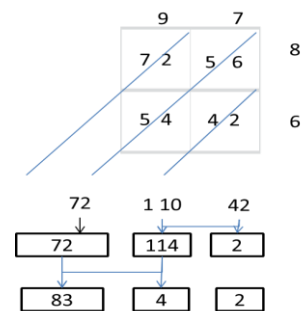method can be applied on every numbers to find their multiplication.

Fig. 1: *Urdhava Tiryakbhayam*

This figure shows multiplication of two decimal number using Urdhava Tiryakbhayam method. In this multiplication we four partial products and then added to find the product.
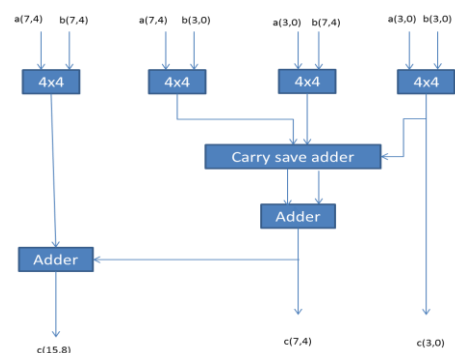
III. VEDIC MULTIPLIER

Fig. 2: *Vedic Multiplier*

This figure shows the use of Urdhava Tiryakbhyam method in binary multiplication. Various research papers are based on this architecture. Same method is used in design of 16x16 and 32x32 multiplier using n/2 multiplier as partial product generator. Cary save adder is used to make multiplier faster as it is faster way to covert 3 number

into 2 number than addition of two number can be carry out with any addition method.

Now in this paper, proposed architecture is based on use of "2x2 multiplier" as partial product generator.

IV.   PROPOSED ARCHITECTURE
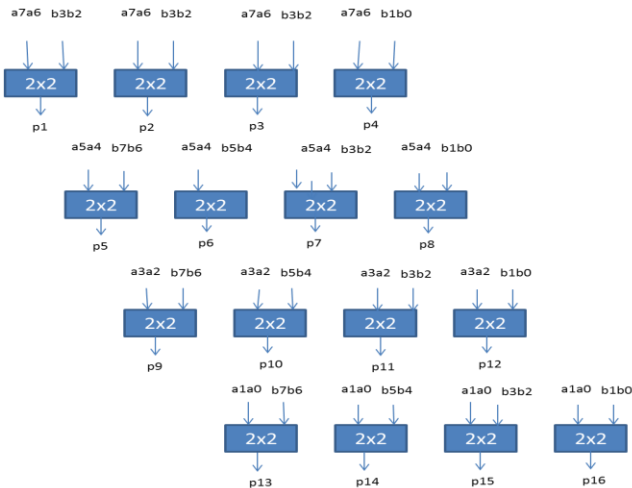
a.   Generation of partial products

Fig. 3: Partial profuct genration using 2x2 multiplier blocks

Here a(7,0)and b(7,0) are two 8 bit numbers that need to be multiply. 2x2 multiplier are used to generate 16 partial products. Every partial product is generate from multiplication of consecutive bits from both numbers. Like,

$$p1=a(7,6) \ x \ b(7,6)$$
$$p2=a(7,6) \ x \ b(5,4)$$

Other partial products are generate in same manner as shown in figure. Different partial product has different multiplying factor.

Now during addtion every partial product has different value. For example p1 multiplying factor of 2^{12} due to its inputs a7a6 is actually "a7a6 x 2^6" and b7b6 is actually "b7b6 x2^6". Like this multiplying factors of all partial products are varying from 2^{12} to 2^0. 2^0 is multiplying factor for p16 during addition because it is multiplication of both LSB.

b.   Reduction of partial products

Due to difference significance or different multiplying factors of partial products, some numbers doesn't even need to be added but just put them together according to their significance like following example,
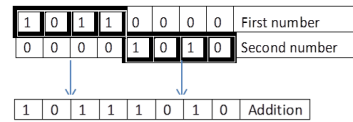
Here, first number has significant digit start after 4th digit and second number has not any significant number after 4th digit. In this case their addition is simply to write them together.

Multiplying factor of partial products are varying from 2^{12} to 2^0. All partial products have only four significant digits as they are outputs of 2x2multiplier. This method can be used on following combinations.

2^{12}(a1)	2^8(a3)	2^4(a8)	2^0(a16)	X1(16-bit number)
	2^{10}(a2)	2^6(a4)	2^2(a12)	X2(12-bit number)
	2^{10}(a5)	2^6(a7)	2^2(a15)	X3(12-bit number)
		2^8(a6)	2^4(a11)	X4(8-bit number)
		2^8(a9)	2^4(a14)	X5(8-bit number)
			2^6(a10)	X6(4-bit number)
			2^6(a13)	X7(4-bit number)

After applying this reduction 16 partial products are reduce into 7 numbers. These numbers can be added like following.

$$q1=x2+x3$$
$$q2=x4+x5$$
$$q3=x6+x7$$
$$Product= q1+q2+q3$$

V.   SIMULATION AND RESULTS

The 8x8 multiplier with the use of 2x2 blocks is designed in VHDL and function verification is done. Multiplier is simulatated with various inputs and results are checked.
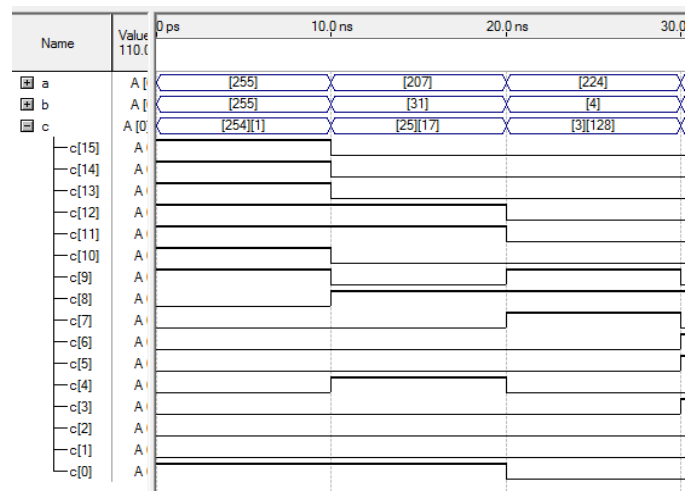

Fig 4 : fucntional simulation of proposed multiplier

Fig 4. RTL view of propsed architecture

8x8 multiplier comparisons

Multiplier	Time	No. of logic elements
Vedic multiplier[6]	27 ns	-
Further decomposed Vedic multiplier [5]	20 ns	-
Vedic multiplier using 4x4 multiplier and CSA	22 ns	150
Vedic multiplier using 4x4	23 ns	144
Vedic multiplier using 2x2 and reduced partial products(this architecture	16.948 ns	124

VI. CONCLUSION AND FUTURE WORK

In this paper we used 2x2multiplier as partial product generator. Due their significance difference in partial products in this method, partial products are easily reduced using above mentioned technique. Reduction of partial product 16 to 7 greatly reduce the adding effort that normally as now only 7 number need to be added. Of course numbers have different digits but still it is helpful in reduction of component and time delay effectively. Due to this, proposed architecture is improvement over overly used Vedic Multiplier Architecture.

This method can be used for higher bit multiplications and addition also can be optimized. Even after reduction of partial products still 7 numbers with different multiplying factor and different digits is available. Different optimizing method can be used to simplify the addition.

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ABOUT AUTHORS:

Mr. Sunil Patel:

He is the PG scholar at G.H.Patel college of engineering and Technology. He is pursuing his master in field of Embedded system. He has completed is bachelor degree in the field of electronics and communication engineering from the Sardar vallabhbhai National Institute of Technology (SVNIT), Surat, India. His area of interest is digital design on FPGA.

Prof. Deepak Parashar:

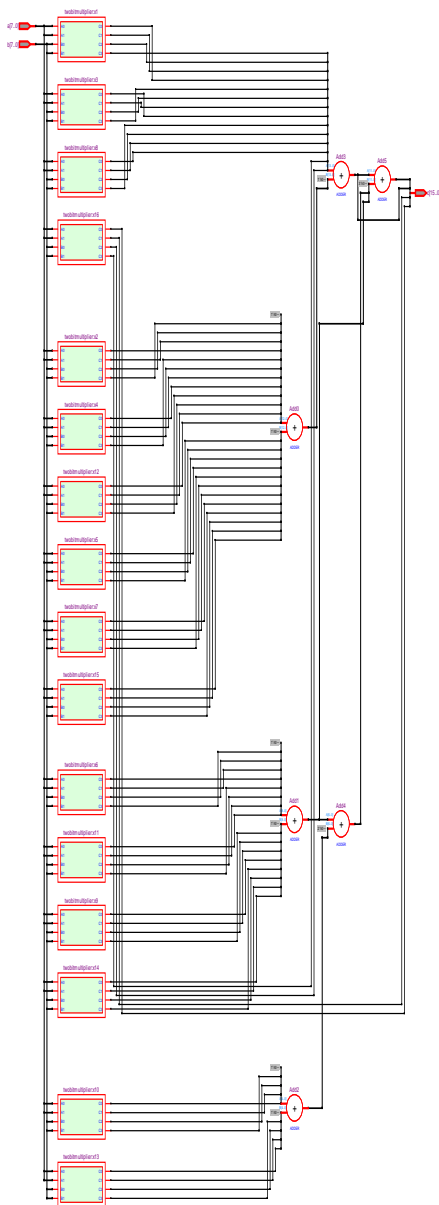Currently he is working as assistant professor at G.H.Patel college of Engineering and Technology. He area of interest is VLSI design.