Reduce Power and Area of Standard Cell Asics by using Threshold Logic Flip Flop and Fir Filter

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Absract:- A new approach is based on the reduce area, active power of the finite impulse response(FIR) without disturbing the performance by using threshold logic flip flop. The approach is based on design of threshold logic gates (TLGs) and their faultless integration with conventional standard-cell design flow. The threshold logic gate behaves as a several input , single output, edge triggered flip flop, which computes a threshold function of the input on the clock edge. Threshold gate is determine by how signals are mapped to its inputs. TLG is variance of diode transistor logic used , it means it contains diode and transistor. Diode performed by logical function and transistor performed by amplification function.

I INTRODUCTION

power is a feature of some electrical appliances, especially copiers, computer, GPUs and computer peripherals such as monitors and printer, that turns off the power or switches the system to a low-power state when inactive. some of the ways to reduce dynamic power include logic synthesis and restructuring to reduce switching activity, gate sizing, technology mapping, retiming, voltage scaling, and so on. Similarly, the uses of dual supply and device threshold voltages, adaptive body biasing, clock and power gating, transistor stacking, and so on are some of the well-known ways to reduce the power due to leakage.

Switching activity is used to measurement of changes of signal value. voltage is the power measurement technique, voltage is used in component increase or decrease depends on circumstance. Mapping an operation that associates each element of a given set (the domain) with one or more elements of a second set (the range). This are the way is used to reduce the system power.

LetY=(y1,y2,……..yn),y£{0,1},W={w1,w2,w3,……wn},w £ R ,and T £ R. A Boolean function f(y) is called a threshold function .

f(y)={1 if w ' y≥T
{0 otherwise

The exist weights w and threshold T can be assumed to be positive integer for during without loss condition.

Threshold value is set first in the system and system voltage is compared with the threshold value. If the value is less than the threshold value , it is consider as 0.system will be off. If the value is greater than the threshold value , it is consider as 1.system will be on. It is used to save the power consumption.

VLSI circuit design for low power:

The growing market of portable (e.g., cellular phones, gaming consoles, etc.), battery-powered electronic systems demands microelectronic circuits design with ultra low power dissipation. As the integration, size, and complexity of the chips continue to increase, the difficulty in providing adequate cooling might either add significant cost or limit the functionality of the computing systems which make use of those integrated circuits. As the technology node scales down to 65nm there is not much increase in dynamic power dissipation. However the static or leakage power is same as or exceeds the dynamic power beyond 65nm technology node.

II THRESHOLD LOGIC

Networks of functions

We deal in this chapter with the simplest kind of computing units used to build artificial neural networks. These computing elements are a generalization of the common logic gates used in conventional computing and, since they operate by comparing their total input with a threshold, this field of research is known as threshold logic.

Feed-forward and recurrent networks

Our review in the previous chapter of the characteristics and structure of biological neural networks provides us with the initial motivation for a deeper inquiry into the properties of networks of

abstract neurons. From the viewpoint of the engineer, it is important to define how a network should behave, without having to specify completely all of its parameters, which are to be found in a learning process. Artificial neural networks are used in many cases as a black box : a certain input should produce a desired output, but how the network achieves this result is left to a self-organizing process. x1 x2 xn y1 y2 ym F ... ... Fig1. A neural network as a black box.

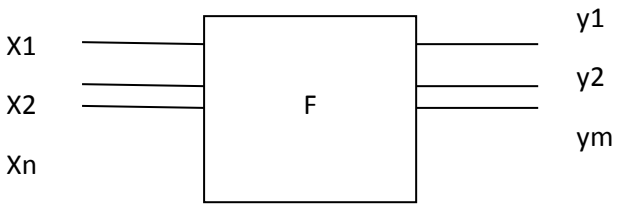

Fig 1. A neural network as a block box

In general we are interested in mapping an n-dimensional real input (x1, x2, . . . , xn) to an m-dimensional real output (y1, y2, . . . , ym). A neural network thus behaves as a "mapping machine", capable of modeling a function F : IRn → IRm. If we look at the structure of the network being used, some aspects of its dynamics must be defined more precisely. When the function is evaluated with a network of primitive functions, information flows through the directed edges of the network. Some nodes compute values which are then transmitted as arguments for new computations. If there are no cycles in the network, the result of the whole computation is well-defined and we do not have to deal with the task of synchronizing the computing units. We just assume that the computations take place without delay.

III. NEW ARCHITECTURE FOR A THRESHOLD GATE

In this section , the architecture for a threshold gate that employs differential logic , referred as a PNAND cell, is described .a PNAND cell is clocked , and behavior can be abstracted to be that of a multi-input edge trigged flip-flop (ETFF). Conventional D-type ETFF (D-FF) computes the function f(y)=y on a clock edge.DFF and PNAND cell can be made scannable and have other features , such as asynchronous preset and clear. A flip-flop is abatable multivibrator . Here reduce power and area by using D flip flop circuit.

D Flip flop

The D flip-flop is widely used. It is also known as a "data" or "delay" flip-flop.

The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line.

Clock	D	Qnext
Rising edge	0	0
Rising edge	1	1
Non-risingedge	X	Q

Fig.2. Truth table of DFF

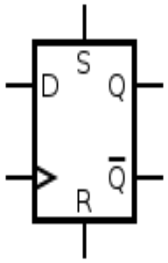

Fig.3.symbol of DFF

IV CELL OPERATION

The PNAND cell consists of three main components : 1) two group of parallel pFFT transistor referred to as the left input network(LIN) and the right input network (RIN). 2)sense amplifier (SA). 3)set-reset latch. The cell operated in two phase such as reset (CLK) and evaluation (CLK).

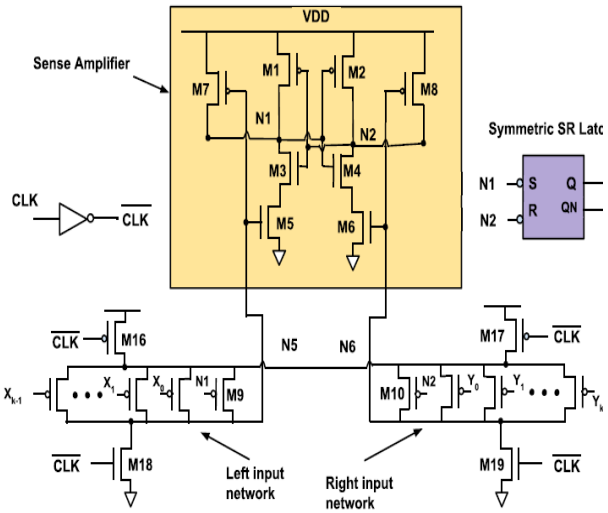

Fig.4. Architecture of the PNAND cell

1) Reset phase : with CLK = 0, the two discharge devices *M*18 and *M*19 pull nodes *N*5 and *N*6 low, which turn OFF *M*5 and *M*6, disconnecting all paths from *N*1 and *N*2 to ground. In addition, *M*7 and *M*8 are active, which results in *N*1 and *N*2 being pulled high. The nFETs *M*3 and *M*4 are ON. With *N*1 and *N*2 being high, the state of the SR latch does not change.
2) Evaluation phase : This corresponds to when CLK=1. As the discharge devices

*M*18 and *M*19 are turned OFF, both *N*5 and *N*6 will rise to 1. Due to the higher conductivity of the LIN, node *N*5 will start to rise first, which turns ON *M*5. With *M*3 = 1, *N*1 will start to discharge through *M*3 and *M*5. The delay in the start time for charging *N*6 due to the lower conductance of the RIN allows for *N*1 to turn ON *M*2 and turn OFF *M*4. Thus, even if *N*2 starts to discharge, its further discharge is impeded as *M*2 turns ON, resulting in *N*2 getting
pulled back to 1.

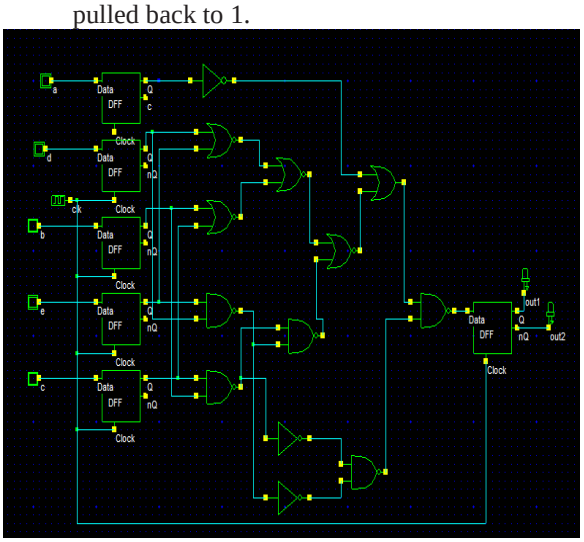

Fig.6. comparison of PNAND with functionally equivalent network of standard cells

Comparing a pNAND with a D-FF does not demonstrate its full advantages, because a pNAND embeds a multi-input logic function, which might require several levels of logic when synthesized with conventional logic cells. The cone of logic feeding the output D-FF is the threshold function f(a,b,c,d,e). Both inputs are one means output will be one that is system will be on. Any one of the input zero means output will be zero. It can be clearly explain in fig. 7. Micro wind software can be used for this implementation

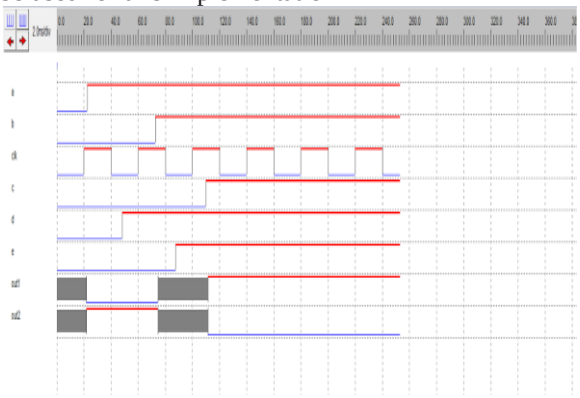

Fig .7. output diagram for fig 6

To reduce the number of gate and flip- flop by replacing single PNAND cell. This can be implanted by three method such as 1)replacing backward cones of logic 2) replacing forward cones of logic. 3) replacing backward and forward cones of logic.

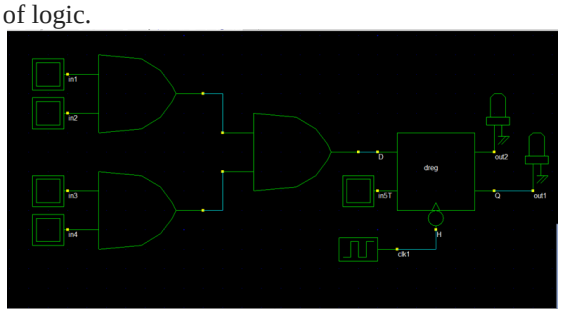

Fig 8(a).replacing Backward cones of logic

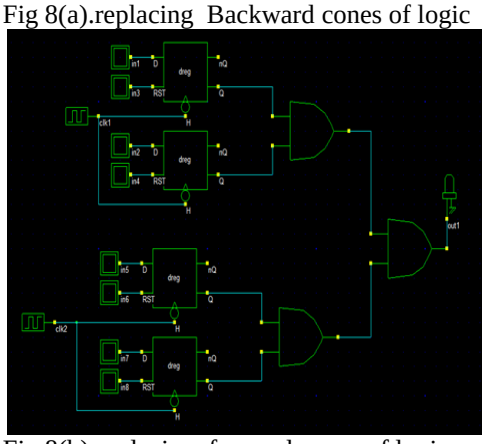

Fig 8(b).replacing forward cones of logic

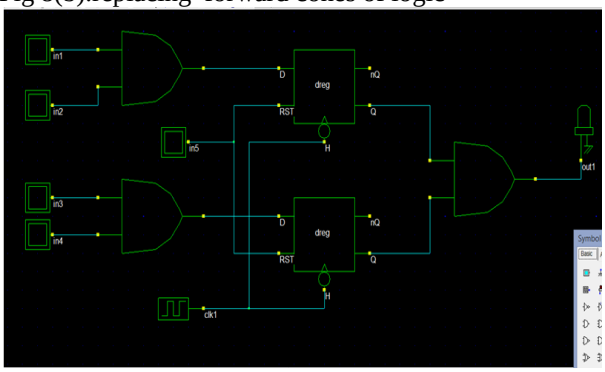

Fig 8(C) . Replacing forward and backward cones of logic

A pNAND cell can replace a single output subcircuit whose function is one of the threshold functions in the library, and whose output has a clock cycle latency of one. Fig. 8shows three different circuits that can be replaced by a single pNAND cell. Note that replacing circuits shown in Fig. 8(b) and (c) with a single pNAND will reduce the total number of flip-flops in the resulting hybrid circuit, which may result in hybrid circuit, which may result in additional reduction in power. Such a replacement would make it difficult to perform a simple functional equivalence check between the original circuit and its hybrid version, because the one-to-one
correspondence between the D-FFs and pNANDs would be lost. For this reason, the hybridization is restricted to maintain
the correspondence. Hence, only the replacement of the type shown in Fig. 8(a), i.e., the replacement

of a single flipflop along with some or all of its fan-in cone by a pNAND, is allowed.

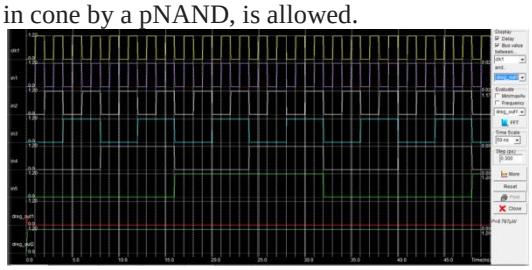

Fig9(a). Backward output

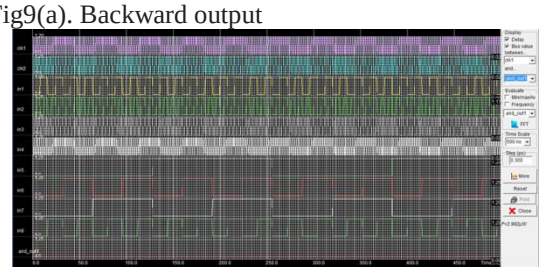

Fig 9(b).forward output

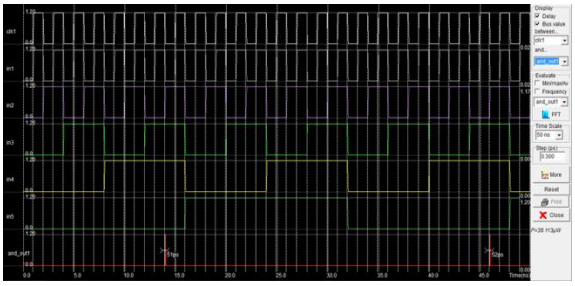

Fig 9(c).forward and backward output

V FIR FILTER IMPLEMENTATION

Adaptive filtering is a widely research topic in communication. When the received signal is corrupted by noise signal. Where both the received signal and noise change continuously then its arises the need of adaptive filtering. Adaptive filters use different algorithms for noise reduction. It passes the corrupted signal through a filter that tends to suppress the noise while leaving the signal unchanged.

e(n)=d(n)-y(n)

Here, x (n) is the input signal, and d (n) is the reference signal or the desired output signal (some noise component are present in it). While y (n) is the output signal.

VI CONCLUSION

Thus the low power leakage is reduced by FIR filter

Dynamic power usage is reduced by replacing DFF by PNAND3.To implement the threshold function output of voltage vs time. An FIR filter is converting the signal by continuous manner to discrete manner.The power is reduced by less than 4**µs**.It is used to estimate the time varying signal.

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