Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 11 Issue 05, May-2022

Recovering Timing Error based on Adaptive Clock Holding Logic for Varying Combinational Path Delay

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***Abstract*—Electronic circuits are the base of electronic devices that we are using in our daily life. It can be sequential circuits or combinational circuits. The proper working or designing of electronic circuit is essential for the proper electronic system or devices. So, the designing should do accordingly. There are different types of errors in electronic circuits. Timing error is one of the main errors in such circuits. Timing error can be caused by many factors. One of such cause is delay. In this paper I am are going to discuss about how timing error can recovered by using a logic called Adaptive Hold Logic (AHL).**

Keywords—Adaptive Hold Logic, Time Borrowing, Razor Flipflop.

I. INTRODUCTION

The electronic circuits may vary in sequential circuits and combinational circuits. They are the main base of electronic devices. Here I am using combinational circuit for the discussion. The demand of electronic devices will only increase if there is a well-equipped system. For that the designing of electronic circuit should be done properly. Minute variation in designing can lead to huge errors in the circuits. The error can cause due to temperature variations, pressure variations, vibrations, incorrect selection of components for the circuit etc. The errors are varied accordingly. Timing errors are an important error that can be caused in circuits.

The combinational circuits may cause timing errors due to many factors. One of such factors is delay. Delay can alter the whole operation of the electronic devices. It can lead to decreasing the demand of that device from customer side. So, there should be a proper method for recovering such timing error circuit. Many of them put large effort in this field. But due to certain limitation we must move into any another method. Here I am going to discuss about how the combinational circuit will affect due to presence of delay and how can be recovered from it. There are many techniques available for recover this problem. Somewhat how they couldn't achieve the goal due to certain limitations. So, I am using a logic called Adaptive Hold Logic (AHL) to recover the timing error circuit. It can not only used to detect the error, but also to recover from the error. The detailed explanation is given in following sections.

Previously there were many techniques used to detect or avoid timing error. Some of the existing systems are time borrowing, in which the present clock cycle will borrow some time from successive stages to reduce the timing error in a circuit. But the circuit implemented was very complex and it was hard to implement. Later, another technique has arrived where the timing error tolerant circuit is detected by using a controlling clock. In that paper the discussion was based on only considering 2 stages of input transmission. And it is also, only mentioning about single delay. Justifying by simply considering a single delay is difficult because different circuit will have different delay error. The technique was done by using the transparency of clock. If the input arrived at correct time the clock for output flipflop become and it gets input in correct time. If the input comes out from the combinational circuit after some delay, then the clock become nontransparent for output flipflop for some time for giving enough time for current clock to complete the operation. Then only the second flipflop become on by giving clock to it and it get input. In this way it is tolerating the timing error. But this is only a technique used to detect the error. We can't correct the error by using this technique. So, I am adopting another logic into it for proper functioning. The logic is called Adaptive hold logic. By using AHL circuit we can recover the timing error circuit. It is the process of holding the clock pulse for certain amount of time when the timing violation affects the operation of successive stage.

The AHL circuit contains a simple counter, which indicates whether the circuit has suffered significant performance degradation. The counter counts the number of errors from transition detector over a certain period. If the timing violations exceed a predefined threshold, it means the circuit has suffered significant timing degradation due to the combinational logic. Then AHL will output 0 to disable the clock signal of the flip-flops. Otherwise, the AHL will output 1 for normal operations.

II. REVIEW OF TIMING ERROR TOLERANT CIRCUIT BY CONTROLLING CLOCK

The timing error tolerant circuit by using a controlling clock is an existing technique developed for acting against the timing error that can be raised in a circuit. It is explained using 2 flipflops and a combinational circuit. In first case, the flipflop1 will send an input to the combinational circuit. In combinational circuit there will be some operation. This system also consists of a transition detector and master clock generator as shown in Fig 1a. The transition detector detects the changes in input transition of a flip-flop, and it produces an error signal. Based on the output of the transition detector, the master clock generator produces a pulse. That pulse is for a certain period only when the clock is high. While a pulse is 1(high) the flip-flop allows the input to the output since the pulse forms a transparent window by controlling a clock of master in the flip-

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
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flop. Thus, the irregular data that are stored in the flip-flop can be returned with delayed regular data.

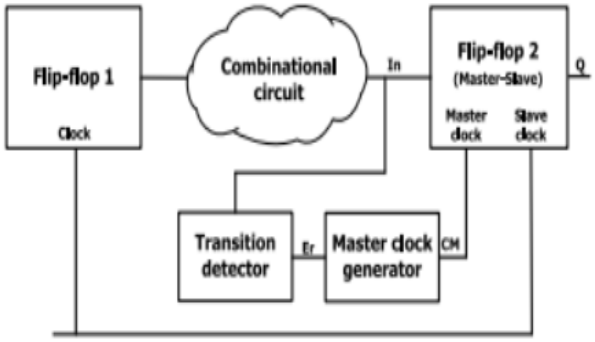


Fig 1a. Concept of Existing System

The timing circuit for the above working is shown in Fig 1b. When a timing error happens on the input data of the flip-flop 2, the flip-flop 2 stores irregular data to the output Q due to the delayed input. After the delayed regular data have arrived at the input of flipflop 2, the transition detector generates an error signal. The transition detector detects both a rising edge and a falling edge of the data by using an inverter and the AND gate.

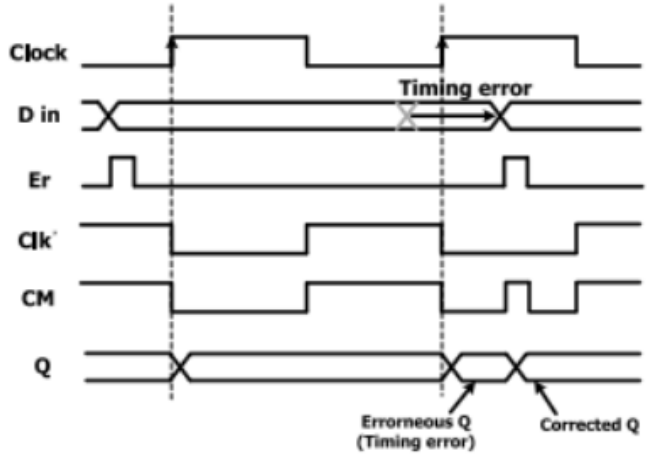


Fig 1b. Timing diagram for Existing System

The transition detector generates a period of a pulse according to designer, which maintains the transparent window for enough time. The master clock generator creates a clock of the master (CM) based on the error signal and clock. Due to the OR gate and inverter in the master clock generator, a CM signal is high for a certain period of time when a timing error occurs. While the CM is high, the FF 2 becomes transparent, and the delayed regular input is stored through FF 2. Thus, the wrong output Q is corrected with the regular input. But it only discusses about single delay error and only consider the issue in 2 stages. But in practical it is not applicable. Due to this limitation I have to move into new technique.

III. PROPOSED TIMING ERROR CORRECTION BY ADAPTIVE HOLD LOGIC

The proposed system considers varying delays occurs in stage of large system with so many stages. I am modifying the existing system that can be applicable practically. The block diagram for proposed recovering timing error circuit by using Adaptive hold logic is shown in Fig 2. So, when an input data delivers from FF1 to combinational circuit. If there is any delay in output of combinational circuit the transition detector will detects the error and produce an error signal. It is given to the AHL logic. AHL logic mainly consists of counter and comparator. The error occurrence in transition will count by the counter in the AHL logic. If the value of counter exceeds the threshold value that I set into comparator. Whenever the counter value is lesser than the threshold value, the gating signal will be one. Whenever the counter value exceeds the threshold value, gating signal will become zero. This zero enter as an input of AND gate and the output of AND gate become zero. That means no clock is applied to wherever the clock is applied. For that clock pulse no operation will take place. It means there is no new data receiving or functioning will take place. So, this mechanism will create time for combinational logic value because they are not stopping any operations in the combinational logic circuit. During the next clock pulse all this delay will be cancelled. Then everything will get new data without delay from like beginning. So here by allowing one clock pulse to hold means providing time to rest of delayed blocks to complete its operation. To adjust the delayed time in the following stages another block is used called time borrowing circuit. In this architecture there another block called Razor flipflop. The transition detector only detects the transition, whenever there is an output from combination circuit the transition detector will detects it as a change and error signal will count. But it doesn't provide the information of whether the transition is taking place in correct time or wrong time. Razor flipflop is used for identifying whether the transition is taking place at correct or wrong time.

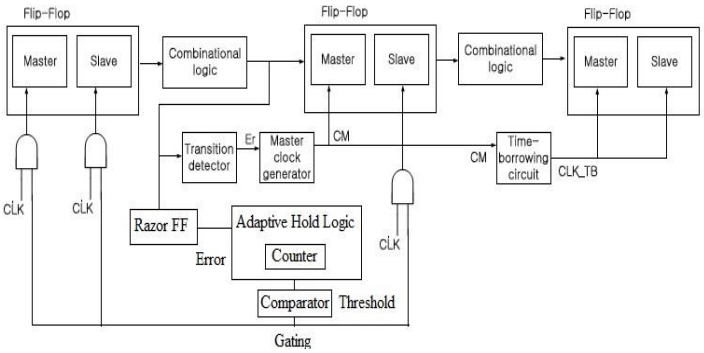


Fig 2. Proposed System Architecture

Razor flipflop is combination of a flipflop and a latch as shown in the Fig 3. Now the output of the combinational logic is given to both flipflop and latch. Flipflop will be active at rising edge and latch become active at delayed clock signal. If the output of combinational logic is '1' and the data comes in the correct time. At rising edge flipflop will receive the '1' and during the falling edge the same '1' will received at latch. By using the comparator at the end of flipflop and latch the output of comparator become '0', so there is no error. If the combinational logic gives output with a delay, the previous value of combinational logic is '0' then flipflop will hold that '0' because during rising edge of transition this '1' has not come. The latch will be enabled at falling edge and it receive new data '1'. Now the output of comparator will be '1'. It

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 11 Issue 05, May-2022

means error is present. Then only the counter in the adaptive hold logic will count. It will avoid the wrong interpretation.

The proposed Adaptive Hold Logic will help us to detect and recover the timing errors through the above-mentioned procedures with the help of Adaptive Hold Logic block and Razor Flipflop block. So, this technique will become an efficient method that to be applicable in those timing based circuits. The architecture for AHL is shown below in the Fig 2 and Razor Flipflop in Fig 3.

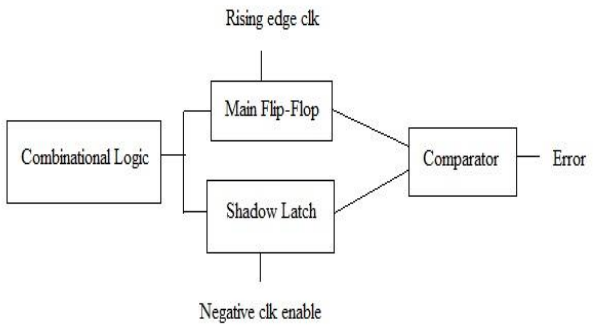


Fig 3. Razor Flipflop

IV. SIMULATIONS AND RESULTS

In this section the proposed technique has been simulated in ModelSim SE 6.3f software. The simulated result is shown in the Fig 4. This result shows how the proposed system varied from existing system. The performance of proposed system is analyzed by changing the values of selection lines, input, reset and set data.

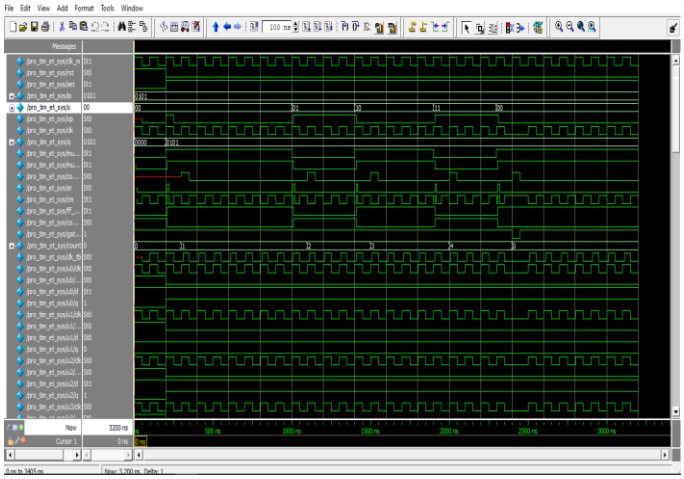
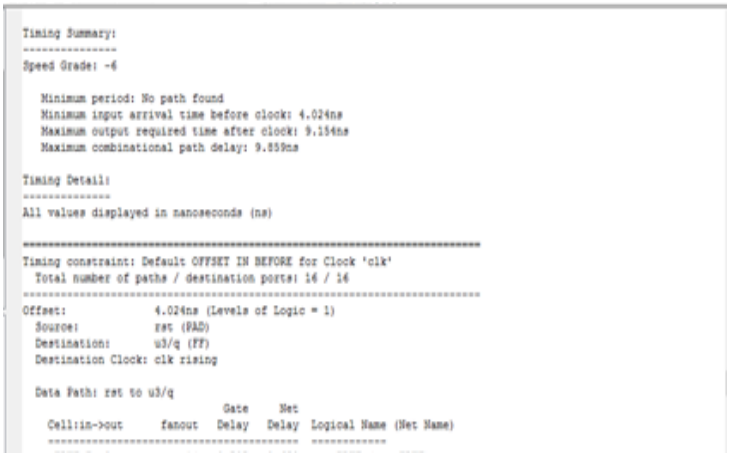


Fig 4. The Simulation result of AHL

V. PERFORMANCE COMPARISON

a. Existing System

In this section the performance comparison of Existing system and Proposed system are depicted. Timing summary of Existing system is shown in the Fig 5. Device Utilization Summary of Existing system in Fig 6. The Current (mA) and Power (mW) Summary of the Existing System in Fig 7.



```
Timing Summary:
---------------
Speed Grade: -6

   Minimum period: No path found
   Minimum input arrival time before clock: 4.024ns
   Maximum output required time after clock: 9.154ns
   Maximum combinational path delay: 9.859ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 16 / 16
-------------------------------------------------------------------------
Offset:              4.024ns (Levels of Logic = 1)
  Source:            rst (PAD)
  Destination:       u3/q (FF)
  Destination Clock: clk rising

  Data Path: rst to u3/q
                                Gate     Net
    Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
```

Fig 5. Timing Summary of Existing System

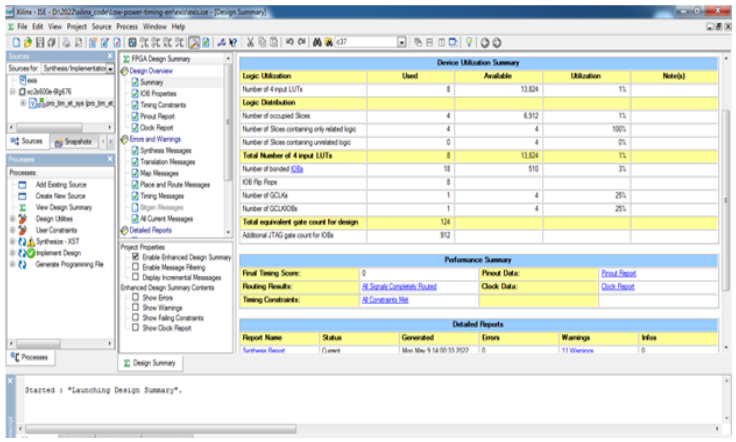
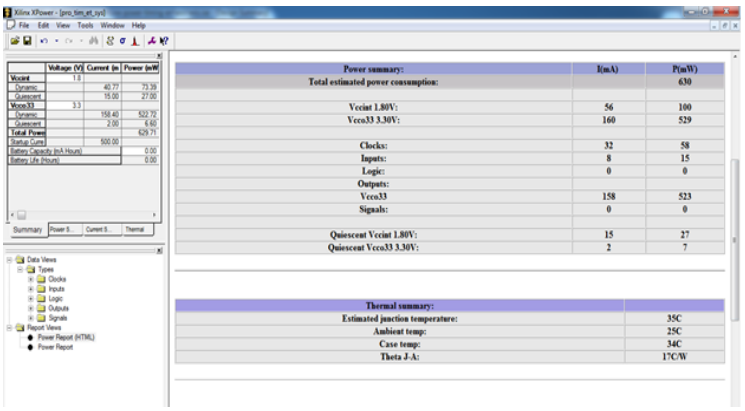


Fig 6. Device Utilization Summary of Existing System



Power summary:	I(mA)	P(mW)
Total estimated power consumption:		630
Vccint 1.80V:	56	100
Vcco33 3.30V:	160	529
Clocks:	32	58
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	158	523
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Thermal summary:	
Estimated junction temperature:	35C
Ambient temp:	25C
Case temp:	34C
Theta J-A:	17C/W

Fig 7. The Current (mA) and Power (mA) summary of Existing System

b. Proposed System

Timing summary of Proposed system is shown in the Fig 8. Device Utilization Summary of Proposed system in Fig 9. The Current (mA) and Power (mW) Summary of the Proposed System in Fig 10.

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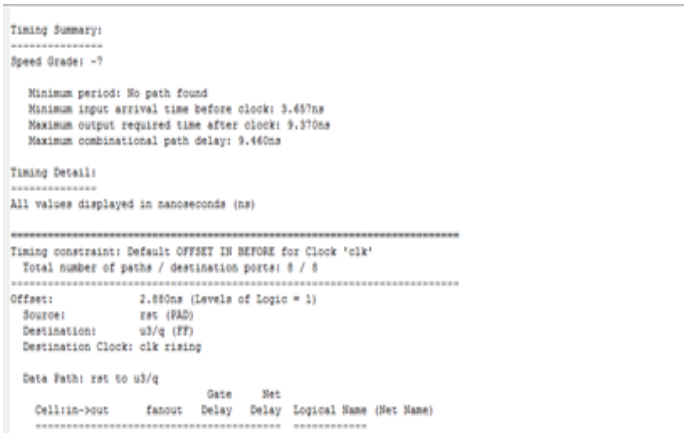


```
Timing Summary:
---------------
Speed Grade: -7

   Minimum period: No path found
   Minimum input arrival time before clock: 3.657ns
   Maximum output required time after clock: 9.370ns
   Maximum combinational path delay: 9.460ns

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 8 / 8
-------------------------------------------------------------------------
Offset:              2.880ns (Levels of Logic = 1)
  Source:            rst (PAD)
  Destination:       u3/q (FF)
  Destination Clock: clk rising

  Data Path: rst to u3/q
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
```

Fig 8. Timing Summary of Proposed System

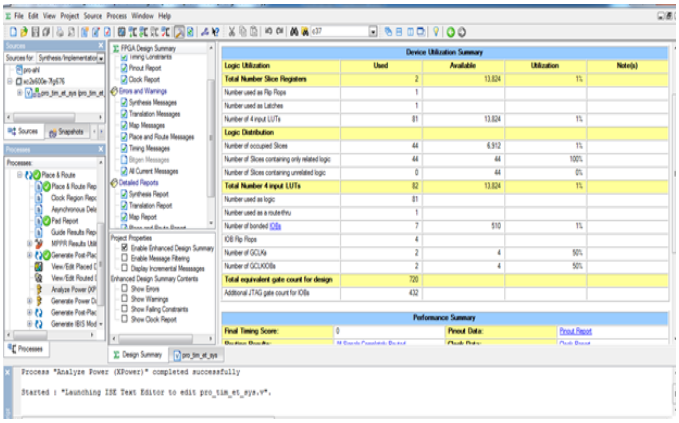
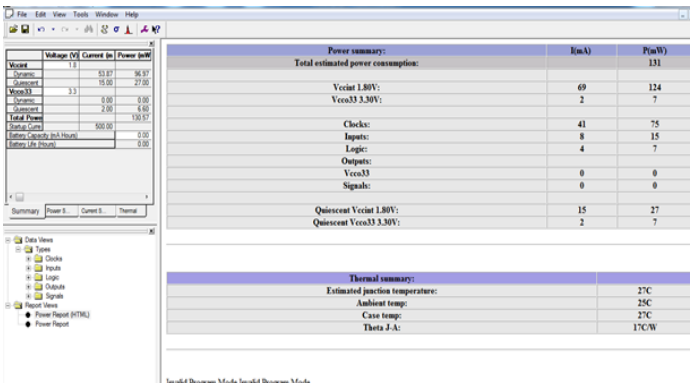


Fig 9. Device Utilization Summary of Proposed System



Power summary:	I(mA)	P(mW)
Total estimated power consumption:		131
Vccint 1.80V:	69	124
Vcco33 3.30V:	2	7
Clocks:	41	75
Inputs:	8	15
Logic:	4	7
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Thermal summary:	
Estimated junction temperature:	27C
Ambient temp:	25C
Case temp:	27C
Theta J-A:	17C/W

Fig 10. The Current (mA) and Power (mA) summary of Proposed System

VI. CONCLUSION

The proposed Adaptive Hold Logic technique is presented in this paper. Comparison between Existing and Proposed systems are described in detail. The proposed system are better in performances like power consumption, time consumption, delay etc. The entire proposed system is coded in Verilog HDL and simulated in ModelSim SE 6.3f software. The proposed system is very much better than existing system and it is an efficient method that can be adopted into timing-based circuits.

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