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Quasi Z-Source Extended Boost Inverter with Active Z-Network Switch

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***Abstract*—A novel configuration for a quasi-Z-source extended-boost inverter with an active Z-network switch is discussed in this paper. The suggested topology of the inverter, in comparison with Enhanced-Boost Quasi-Z-Source Inverters (EB-QZSI) which have two switched impedance networks, achieves the same boost factor with one extra switching device along with a reduction of two LC pairs and one diode. Besides, the current stress around switches is halved, which results in a larger reduction in switch conduction loss. Due to a reduction in losses, the efficiency of the proposed inverter is improved. Also, the proposed inverter maintains a common ground between the inverter bridge and the source. Besides, the input current is continuous for the proposed inverter. The operation principles of the suggested topology are described below. Some points of differences and similarities in the EB-QZSI and the suggested inverter topology are also described in the paper. The simulation results of the suggested topology are achieved. all the results are checked using theoretical analysis.**

Index Terms— impedance network, quasi-Z-source inverter, active switched

I. INTRODUCTION

In fuel cell and solar systems which are renewable energy systems, the Z-source inverter (ZSI) seems to be a very successful topology as discussed in [1]. ZSI contains unique qualities, which are not obtainable from a conventional current source or voltage source converter. To reduce the conceptual and theoretical problems which are present in conventional current source (CSI) and voltage source converter (VSI) [2], a Z-source converter is used. The Z-source converter eliminates the logical and technical obstacles and drawbacks of the conventional current source converter and voltage source converter. For any power conversion, the Z-source can be applied. Turning on of the switches in the same leg simultaneously is possible in the Z-source inverter that too without dead time. This is not allowed in conventional VSI and CSI. ZSI also has the buck-boost capability with improved reliability of the converter.

Given the above benefits, the ZSI also suffers from certain disadvantages such as a discontinuous input current due to the input diode in between input power supply and dc connection, failure to share a common ground in between them. To solve these issues, [3] a class of quasi-Z-source inverter (QZSI) is invented for joint earthing and continuous current characteristics with reduced ratings of components and source tension, but no improvement in boost factor is achieved when compared to the original ZSIs. To achieve a high boost factor, extended boost topologies have emerged. The proposed inverter in [4] is able to improve voltage boost ability with switched inductor (SL) cells used in place of two inductors in the impedance network. However, the drawbacks are input current is discontinuous and still, there is no common ground between dc link and power supply.

To reduce the passive elements of the impedance network a switched boost inverter (SBI) is invented. SBI adding only one extra active switch to reduce the passive components. The boost factor of the SBI is the same as ZSI. By reducing the passive components significant reduction in volume, weight, and converter cost is achieved in [5] and [6]. To improve boost inversion ability, high voltage-gain switched Z-source inverter (HVG-SZSI) in [7] is invented. this topology brings together SBI and QZSI. But the problem with sharing common ground persists.

By using cascaded networks, voltage gain can be improved. Extended-boost ZSIs in [8] have four families. With the addition of LC pairs and diodes to the QZSI, other families can be realized to improve boost ability. Besides, voltage stress across the capacitors is reduced in comparison to the conventional ZSI. The boost factor of enhanced-boost Z-source inverter with switched Z-impedance (EB-ZSI) in [9] is very high and its expression is given in (1).

$$B = \frac{1}{1 - 4D + 2D^2} \tag{1}$$

where B stands for boost factor and the shoot-through duty cycle is represented by D. The proposed topology also suffers from certain drawbacks such as different ground points between dc supply and inverter bridge and the input current is discontinuous. To overcome these drawbacks a new topology enhanced-boost quasi-Z-source inverter (EB-QZSI) is proposed in [10]. The proposed inverter provides continuous input current by using two switched impedance network. The proposed inverter escapes the above-mentioned disadvantages in [9] and maintains a high boost factor. Fig. 1 shows EB-QZSI with continuous input current configuration. To get a high boost factor, both [9] and [10] use four inductors and four capacitors due to which it becomes bulkier and heavier leading to an increase in converter cost.

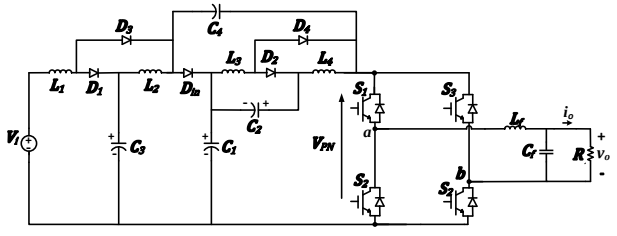

Fig. 1.Enhanced-boost quasi-Z-source inverter for continuous input current configuration using two switched impedance networks [10].

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A new quasi Z-source extended boost inverter with an active Z-network switch is introduced in this paper. Proposed topology overcomes the above-mentioned disadvantages of a traditional ZSI. The proposed inverter reduces two inductors, two capacitors, and one diode and adding only one extra switch as compared with EB-QZSI. The boost factor of both the topologies is the same. The proposed topology has all the advantages that are present in EB-QZSI such as, the input current is continuous, double-ground features, etc. Also, the current stress around switches is halved, resulting in a large reduction in switch conductive loss and an improvement in overall inverter efficiency. The principles of operation are evaluated in section II. The EB-QZSI and suggested topology are compared with each other in section III. The theoretical testing of the proposed inverter is performed in section IV with simulation results.

II. PROPOSED TOPOLOGY

Fig. 2 displays the suggested topology structure consists of two inductors (L_1, L_2), two capacitors (C_1, C_2), four diodes (D_1, D_2, D_3, D_4), and one active switch(S), couples the V_i source voltage to the dc link. A low pass LC filter (L_f, C_f) connects the dc link to the load R. Remember that in this paper evaluation is done using a single-phase H-bridge inverter but the suggested topology can also be extended to three-phase circuits

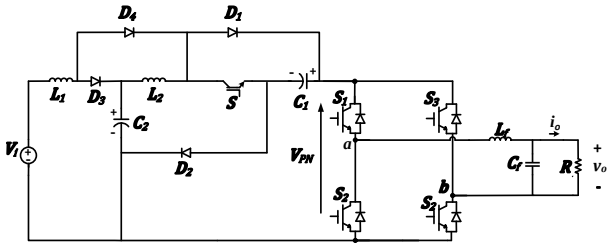


Fig. 2. Quasi Z-source extended boost inverter with Active Z-network switch

A. Operation Principles

For study purpose, there are two operative conditions of the proposed inverter that is shoot-through state and non-shoot through state. operation principles of traditional ZSI and proposed inverter are similar. Fig. 3 (a) and (b) displays the proposed inverter's corresponding circuits for the duration of the shoot-through and non-shoot-through conditions, accordingly,

1) Shoot-Through state

When all the switches in any leg are switched ON simultaneously, the inverter bridge is short-circuited as shown in fig.3 (a). this condition is called as a shoot-through state. The diode D_4 and switch S is switched ON and the diodes D_1, D_2, and D_3 are biased in reverse. Via capacitors, inductors are charged in the shoot-through state. The two inductor voltages (V_{L1}, V_{L2}) and two capacitor currents (i_{C1}, i_{C2})are derived in this state. Power is not transferred to the load R, because the inverter bridge is a short circuit in this state.

$$V_{L1} = L_1 \frac{di_{L1}}{dt} = V_i + V_{C1} \quad (2)$$

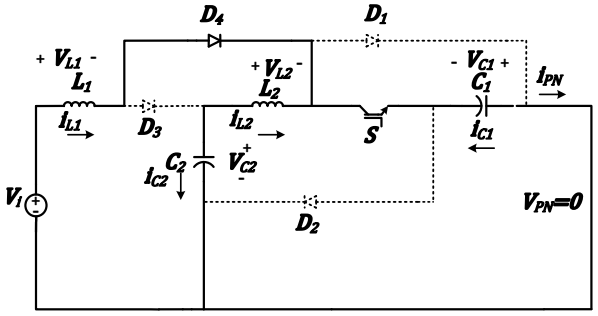
$$V_{L2} = L_2 \frac{di_{L2}}{dt} = V_{C1} + V_{C2} \quad (3)$$

$$i_{C1} = C_1 \frac{dV_{C1}}{dt} = -i_{L1} - i_{L2} \quad (4)$$

$$i_{C2} = C_2 \frac{dV_{C2}}{dt} = -i_{L2} \quad (5)$$

When all switches in one leg are turned OFF, peak dc-link voltage ($\hat{V}_{PN}$) is zero.

$$\hat{V}_{PN} = 0 \quad (6)$$



(a)

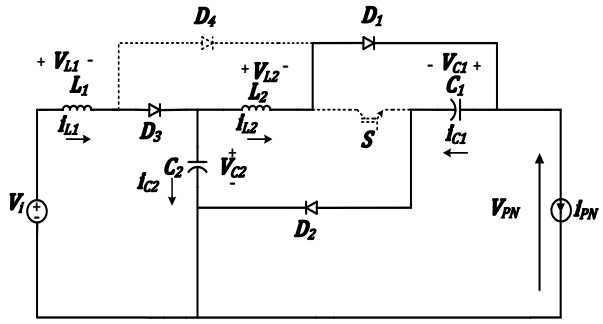


Fig. 3. Corresponding circuits of the proposed topology. (a) Shoot-through state and (b) non- shoot-through state

2) Non-shoot-Through State

Non-shoot-through state conditions are shown in Fig. 3 (b). In this state the switch S and diode D_4 are turned OFF and diodes D_1, D_2, and D_3 are switched ON. The source charges the capacitors via inductors. During this state, power is transferred to the load R which is stored in the inductors, inverter bridge is open-circuited. In this state, the voltage and current relationship can be written as

$$V_{L1} = L_1 \frac{di_{L1}}{dt} = V_i - V_{C2} \quad (7)$$

$$V_{L2} = L_2 \frac{di_{L2}}{dt} = V_{C1} + V_{C2} \quad (8)$$

$$i_{C1} = C_1 \frac{dV_{C1}}{dt} = i_{L1} - I_{PN\_non} \quad (9)$$

$$i_{C2} = C_2 \frac{dV_{C2}}{dt} = i_{L1} - i_{L2} \quad (10)$$

Where I_{PN_non} stands for average dc-link current in the non- shoot-through condition.

The maximum dc-link voltage is equivalent to the capacitor voltage C_1 .

$$\hat{V}_{PN} = V_{C1} \quad (11)$$

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B. Boost Factor Derivation

Once the voltage balance principle is applied for the inductor L_1 from (2), we obtain

$$V_i = (1 - \mathrm{D})V_{C2} - DV_{C1} \tag{12}$$

From (3), applying the volt-sec balance law to the inductor L_2, we have

$$V_{C2} = (1 - 2\mathrm{D})V_{C1} \tag{13}$$

The voltage across the capacitor C_1 is obtained by putting (13) into (12), we have

$$V_{C1} = \frac{1}{1 - 4D + 2D^2} V_i \tag{14}$$

Substituting (13) into (14), yields

$$V_{C2} = \frac{1 - 2D}{1 - 4D + 2D^2} V_i \tag{15}$$

In non-shoot-through condition, the peak dc-link voltage across the converter bridge can be derived from (11) and (14), we have

$$\hat{V}_{PN} = \frac{1 - 2D}{1 - 4D + 2D^2} V_i \tag{16}$$

Thus, the boost factor B of the suggested inverter can be expressed as

$$B = \frac{\hat{V}_{PN}}{V_i} = \frac{1 - 2D}{1 - 4D + 2D^2} \tag{17}$$

where D is the duty ratio. The value of D is between 0 to 0.29

C. Control Strategy for the proposed topology

In this paper, switches are controlled using control signals generated using the PWM control technique. Voltage gain G of the Single-phase dc–ac converter is obtained by

$$G = M \cdot B = \frac{\hat{v}_0}{V_i} \tag{18}$$

Where M stands for the modulation index, B is the boost factor and the peak output voltage is represented by $\hat{v}_0$. Boost factor B is dependent upon the PWM control technique. From (18), when the boost factor is high, automatically voltage gain G is high. Simple boost control (SBC) in [6] is used in the proposed inverter. as shown in fig.4, in one switching cycle two shoot-through states occur. By using the SBC, current stress around the switches is halved as compared with the control method in [5]. In a shoot-through state, a two-phase leg is switched ON simultaneously under the SBC although the only one-phase leg is switched ON in control technique [5]. By controlling the modulation index, we can control the duty ratio in SBC as follows:

$$D \leq 1 - M$$

Fig. 4 shows the PWM control technique for the proposed inverter [6]. Two modulating waveforms, i.e., $v_{control}$ and $-v_{control}$, are related with a high-frequency triangular waveform, i.e., v_{tri}, to produce pulses. This pulse is used to operate the switches S_1, S_2, S_3, and S_4. Compared to another triangle waveform (dashed line) with a double frequency and half of the amplitude of that of v_{tri}, a constant voltage $-V_{SH}$ is produced for the S_0 switch. The S_0 a control signal is then passed through the OR logic gate to produce the shoot-through states in the inverter bridge into the control signals of switches S_1 to S_4.

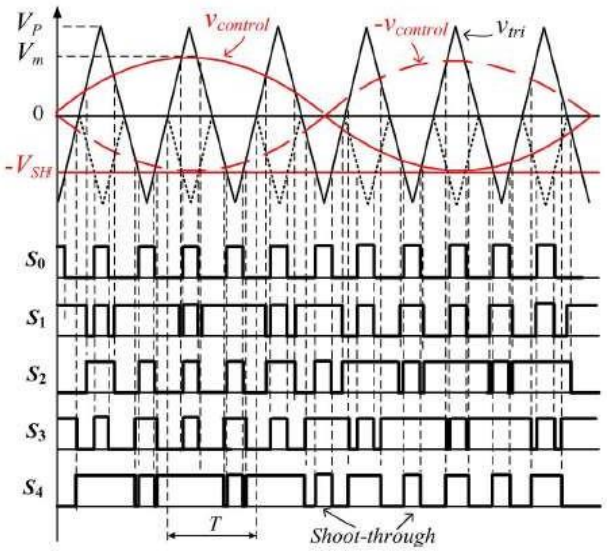

Fig. 4. PWM control for the proposed inverter.

D. Inductors and Capacitors Design

During shot-through state the inductor currents rise linearly according to the above activity concepts. Therefore, the current ripple of inductors can be obtained in terms of (2), (14), and (15) as follows:

$$\Delta i_{L1} = \frac{2D(1-D)^2}{(1 - 4D + 2D^2)} \frac{V_i}{L_1 k_{sh} f_s} \tag{19}$$

$$\Delta i_{L2} = \frac{2D(1-D)}{(1 - 4D + 2D^2)} \frac{V_i}{L_2 k_{sh} f_s} \tag{20}$$

where k_{sh} represents the number of shoot-through states within one switching cycle. Under the suggested topology SBC approach, ksh= 2. Thus, the inductors L_1 and L_2 can be obtained by

$$L_1 = \frac{2D(1-D)^2}{(1 - 4D + 2D^2)} \frac{V_i}{\Delta i_{L1} k_{sh} f_s} \tag{21}$$

$$L_2 = \frac{2D(1-D)}{(1 - 4D + 2D^2)} \frac{V_i}{\Delta i_{l2} k_{sh} f_s} \tag{22}$$

The average current of the input supply can be achieved under lossless conditions as (23)

$$I_i = \frac{P_o}{V_i} \frac{2D(1-D)^2}{(1 - 4D + 2D^2)} \frac{V_i}{\Delta i_{L1} k_{sh} f_s} \tag{23}$$

The average input source current is equal to the average inductor $L1$ current, applying the capacitor charge balance

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theory from (4), (5), (9), (10), and (23), the average inductor currents can be extracted as follows:

$$I_{l1} = \frac{M^2}{(1-4D+2D^2)^2}\frac{V_i}{2R} \quad (24)$$

$$I_{l2} = \frac{(1-D)M^2}{(1-4D+2D^2)^2}\frac{V_i}{2R} \quad (25)$$

In addition, The average non-shoot-through dc-link current may be written as

$$I_{PN\_non} = \frac{M^2}{(1-D)(1-4D+2D^2)}\frac{V_i}{2R} \quad (26)$$

According to (4), (5), and (24), (25), voltage ripple of the capacitors can be produced as follows:

$$\Delta v_{C1} = \frac{D(2-D)M^2}{(1-4D+2D^2)^2}\frac{V_i}{2RC_1k_{sh}f_s} \quad (27)$$

$$\Delta v_{C2} = \frac{D(1-D)M^2}{(1-4D+2D^2)^2}\frac{V_i}{2RC_1k_{sh}f_s} \quad (28)$$

Therefore, the capacitors can be designed by

$$C_1 = \frac{D(2-D)M^2}{(1-4D+2D^2)^2}\frac{V_i}{2R\Delta v_{C1}k_{sh}f_s} \quad (29)$$

$$C_2 = \frac{D(1-D)M^2}{(1-4D+2D^2)^2}\frac{V_i}{2R\Delta v_{C2}k_{sh}f_s} \quad (30)$$

III. COMPARISON OF PROPOSED TOPOLOGY WITH EB-QZSI

The proposed topology is compared with the enhanced-boost quasi-Z-source inverter for continuous input current configuration (EB-QZSI) which have two switched impedance networks [10]. Detailed comparison of the topology characteristics as shown in table I.

A. *Topology characteristics*

TABLE I. COMPARISON OF TOPOLOGY CHARACTERISTICS

Topology Characteristics	EB-QZSI	Proposed
No. of Inductors	4	2
No. of Capacitors	4	2
No. of Diodes	5	4
No. of Switches	0	1
Common Ground	Yes	Yes
Starting inrush current	No	No
Continuous input current	Yes	Yes
Input current ripple	Approximate zero	Approximate zero
Boost factor	$\frac{1}{1-4D+2D^2}$	$\frac{1}{1-4D+2D^2}$

Detailed comparison of the topology characteristics as shown in table I. when comparing the topology characteristics, LC output filter, and switches of the inverter bridge are not taken into account. It can be found from the table I that the boost factor of the proposed topology and EB-QZSI is the same. However, the proposed inverter reduces two inductors, two capacitors, and one diode as compare to EB-QZSI. To reduce these passive components, proposed topology adding just one switch into the circuit. Input current ripple in both the topologies is approximate zero. Advantages of the EB-QZSI is no start-up inrush current, common ground between source and inverter bridge, input current ripple is approximate zero, and input current is continuous. These are all advantages also present in the proposed inverter by using less passive components.

B. *Voltage and Current Stresses*

By using the same boost factor and input voltage, the proposed inverter compares voltage stresses across diodes, capacitor voltages, and switch stresses with EB-QZSI as shown in table II. In proposed topology, The voltage stresses across the capacitors C_1 and C_2 is higher than the EB-QZSI. But the entire voltage stress across the capacitors in both the topologies are identical. Because the proposed inverter uses only two capacitors and the EB-QZSI used four capacitors. As shown in table II the voltage stress around the switches is the same in both the topologies. The total voltage stress across the diodes is identical in both the topologies as shown in table II.

TABLE II. COMPARISON OF VOLTAGE STRESS IN THE SAME BOOST FACTOR AND INPUT VOLTAGE

Parameter		EB-QZSI	Proposed
B		$\frac{1}{1-4D+2D^2}$	$\frac{1}{1-4D+2D^2}$
Capacitor voltage	C_1	$(1-D)^2BV_i$	BV_i
	C_2	$D(1-D)BV_i$	$(1-2D)BV_i$
	C_3	$(1-3D+D^2)BV_i$	–
	C_4	$D(2-D)BV_i$	–
$\sum V_C/V_i$		$2(1-D)B$	$2(1-D)B$
$V_{C,max}/V_i$		$(1-D)^2B$	B
Diode stresses	$D_{1,2}$	$(1-D)BV_i$	BV_i
	D_3	DBV_i	$2(1-D)BV_i$
	D_4	DBV_i	$2DBV_i$
	D_{in}	BV_i	–
$V_{D,max}/V_i$		B	B
Switch stresses	S	–	BV_i
	S_{1-4}	BV_i	BV_i
$V_{C,max}/V_i$		B	B

For comparison purposes, the same input voltage, voltage gain, and load are taken in proposed and EB-QZSI as shown in the table II. The control technique of both the inverters is different, because of this the stress across the switches is not

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the same. In the proposed topology SBC control method [6] is used and in EB-QZSI control method [5] is used. By using the SBC control method [6], the current stress around the switches is reduced by halved as compared to the control method [5] as shown in table III. Inductor currents of both the topologies are equal, under the same operating condition. It is envisaged that the current stress across the diodes is generally less than that of EB-QZSI.

TABLE III. COMPARISON OF CURRENT STRESS IN THE SAME VOLTAGE GAIN, INPUT VOLTAGE AND LOAD

Parameter		EB-QZSI	Proposed
G		$M \cdot B$	$M \cdot B$
I_i		$G^2V_i/(2R)$	$G^2V_i/(2R)$
I_{PN-non}		$MGV_i/[2(1-D)R]$	$MGV_i/[2(1-D)R]$
Inductor currents	$L_{1,3}$	I_i	I_i
	$L_{2,4}$	$(1-D)I_i$	$(1-D)I_i$
Diode stresses	D_1	I_{L1}	I_{L2}
	D_2	I_{L1}	$I_{L2}-I_{PN-non}$
	$D_{3,4}$	I_{L1}	I_{L1}
	D_{in}	$I_{L2}-I_{PN-non}$	$-$
$I_{D,max}R/V_i$		$(1-D)G^2-MG/[2(1-D)$	$G^2/2$
Switch stresses	S	$-$	$I_{L1}+I_{L2}$
S_{1-4}		$I_{L1}+I_{L2}$	$I_{L1}+I_{L2}/2$
$I_{S,max}\,R/V_i$		$(2-D)\,G^2/2$	$(2-D)\,G^2/2$

C. Inductance and Capacitance

From table II, the voltage stress across the inductors of the proposed inverter is double as compared to EB-QZSI. Current stress across the inductors is the same in both topologies, as shown in table III. In other words, with the same operating conditions, the inductance of the suggested topology is double than EB-QZSI and the capacitance of the proposed topology is the same as EB-QZSI as shown in table IV.

TABLE IV. COMPARISON OF INDUCTANCE AND CAPACITANCE

Parameter	EB-QZSI	Proposed
$L_{1,3}$	$D(1-D)^2BV_i/\Delta i_{L1}k_{sh}f_s$	$2D(1-D)^2BV_i/\Delta i_{L1}k_{sh}f_s$
$L_{2,4}$	$D(1-D)BV_i/\Delta i_{L2}k_{sh}f_s$	$2D(1-D)BV_i/\Delta i_{L2}k_{sh}f_s$
$C_{1,4}$	$D(2-D)M^2B^2V_i/(2R\Delta v_{C1}k_{sh}f_s)$	
$C_{2,3}$	$D(1-D)M^2B^2V_i/(2R\Delta v_{C2}k_{sh}f_s)$	

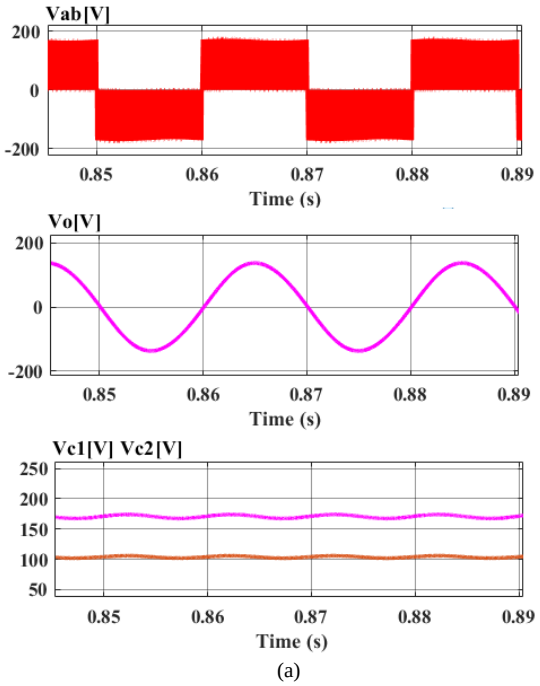
IV. Simulation Results of the Proposed Inverter

Simulation results are given to validate the process and efficiency of the proposed topology. table V displays the circuit parameters used to simulate the proposed topology.

TABLE V. PARAMETERS USED FOR SIMULATION

Parameters	Values
Input voltage (V_i)	50 V
Output voltage(V_o)	$100V_{RMS}$
Fundamental frequency (f_o)	$50H_Z$
Switching frequency (f_s)	10 kH_Z
Inductors $(L_1 = L_2)$	2 mH
Capacitors $(C_1 = C_2)$	470 μF
Output filter inductor (L_f)	4.6 mH
Output filter capacitor (C_f)	10 μF
Load resistance (R)	50 Ω

The simulation results for the proposed topology are shown in Fig. 5. The suggested topology has been simulated using MATLAB / Simulink on the open-loop configuration. The control method [6] is used to simulate the proposed topology. To boost the input voltage, D = 0.2 and M = 0.8 is taken. RMS output voltage across the load is roughly 101 V and dc-link voltage is approximately 178V as shown in fig.5 (a). To provide a pure AC supply to the load, the LC filter is connected as shown in fig.2. The value of output filter inductor (L_f) and capacitor (C_f) are 4.6 mH and 10 μF respectively as shown in table V. the voltage across capacitor Vc1 and Vc2 are approximately 180 and 108 V respectively, as shown in fig.5 (a). These results are matched with theoretical values (14) and (15) respectively. The values of both the Inductor currents L_1 and L_2 are increases in shoot-through state linearly. as shown in fig. 5 (b). In non-shoot-through condition, inductor current decreases linearly. Accordingly, the above operational criteria in section II are well confirmed over the analysis of the following simulation.



(a)

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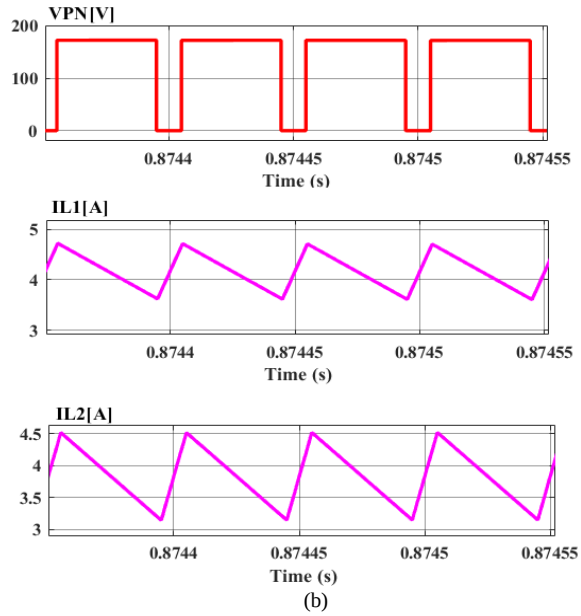

(b)

Fig. 5. Simulation results of the proposed topology with $V_i = 50$ V, $D = 0.2$ and $M = 0.8$. (a) From top to bottom: Output voltage of inverter bridge (V_{ab}), output voltage (V_o), and capacitor voltages (C_1, C_2), respectively. (b) From top to bottom: dc-link voltage (V_{PN}) and inductor currents (L_1, L_2), respectively.

V. CONCLUSION

In this paper, a new Quasi Z-source extended boost inverter with Active Z-network switch is presented. The proposed inverter is compared with EB-QZSI. There are some advantages of the proposed inverter over the EB-QZSI such as 1) current stress across the inverter bridge switches is less and it helps to improve the efficiency of the overall inverter. 2) reducing the weight, volume, and cost of the proposed topology by reducing the two inductors, two capacitors, and one diode but the boost factor is the same in both the topologies. 3) the power losses of the suggested topology are reduced, by reducing the passive components, that help to improve boost ability.

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