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Quantum Dot Cellular Automata based Arithmetic and Logical Unit Design

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***Abstract*—Quantum dot cellular automata(QCA) is an upcoming nanotechnology and it is considered as a suitable technology which overcomes the limitations of the current CMOS technology. This paper proposes the design of an efficient single layer ALU in QCA without crossovers. The proposed architecture has significant reduction in cell count, area and complexity. The design is implemented with QCA Designer tool to analyse the efficiency of ALU.**

Keywords—Quantum dot cellular automata; QCA; CMOS; nanotechnology; ALU

I. INTRODUCTION

Due to the limitations of the conventional CMOS technology, researchers extremely felt the need to find an alternative technology for the coming future. As a result, quantum-dot cellular automata (QCA) was found to be a suitable replacement that would provide unique eminent features such as small feature size at an ultra low power consumption that can operate in room temperature at a frequency range of THz [1]. The International Technology Roadmap for Semiconductors (ITRS) report lists out several nano-electronics substitutes: Single Electron Tunneling(SET), Resonant Tunneling Diodes(RTD), Tunneling Phase Logic(TPL), Quantum Dot Cellular Automata(QCA). Accordingly, QCA is a promising technology which provides high device density at low power [2].

Further, VLSI circuits carries following limitations: power dissipation, interconnections and short channel effects. Increment in the device density within a stipulated area may result in chip damage due to the thermal effect developed over the chip. QCA is a good alternative to the silicon based technology. Advantages of QCA based systems are high speed, high device density at low power consumption. Also high parallel processing can be attained by using QCA [3].

This paper is composed of following sections. Section 1 includes the introduction. Section 2 gives details about related work carried out in the field of QCA. Section 3 includes the proposed ALU design. Section 4 comprises of simulation results and discussions. Finally, the conclusion is presented in Section 5.

II. RELATED WORK

A. QCA Cell

The basic building elements in QCA are cells. A cell has four quantum dots that are situated around the four vertices. There are two mobile electrons inside the cell which places themselves at opposite corners with respect to each other because of the columbic repulsion. Based on this arrangement of electrons, two possible polarization states are available such as P=+1 that is considered as binary value '1' and P=-1 which is treated as binary value '0' as shown in the fig.1. If the polarization state of one cell gradually changes from one state to the other, immediately the next consequent cell goes through a quasi-adiabatic switching phenomena which leads to a change of state of its polarization [4].

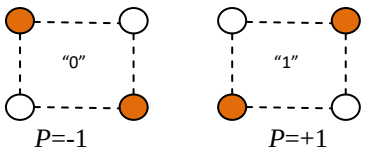

Fig. 1. QCA cell comprsing four quantum dots and two electrons with two stable polarization states

B. QCA wires

In this technology, transmission of information is achieved by using QCA binary wires which are formed by linear arrangement of quantum cells as arrays. Columbic interactions within adjacent cells causes the change in polarization states of each cell which indeed results in the flow of information [5]. As there is no flow of current but only information flow through a binary wire, there is a significant reduction in power dissipation associated with signal transmission. The propagation of signal through a 90° QCA wire is shown in fig.2. In the proposed ALU, along with 90° QCA wires, the 45° QCA wire are also used in order to avoid crosstalk problems.

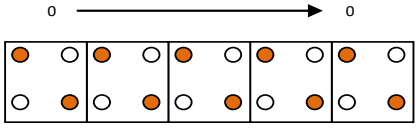

Fig. 2. QCA contact wire

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C. QCA Clocking

The clocked control of QCA cell arrays removes metastability issues, and facilitates pipelined computing architecture realization. There are 4 clock zones which is systematically applied to each QCA cell in QCA circuits.the clock zones are Clock 0, Clock 1, Clock 2 and Clock 3. The clock signal in each clock zone experiences 4 different phases-Switch, Hold, Release, and Relax [6]. There is a phase shift of 90 °between 4 adjacent phases of a clock zone. Fig. 3 illustrates four phase switching realized in each clocking phase for different clock zones. Information flows in a pipelined fashion from inputs to the outputs during each clock zones [7].

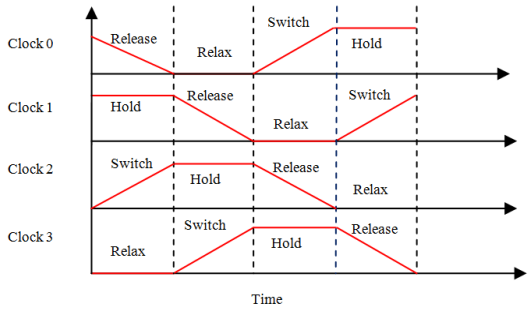

Fig. 3. Clock zones in QCA

D. Three Input Majrity Voter

The majority gate plays a significant role in the design and implementation of QCA circuits. The three input majority voter is the basic structure used in realization of logical expressions. 'AND' and 'OR' operations can be easily obtained with a slight change in the polarization of one of the QCA cell. The three input majority gate consists of five QCA cells. The three inputs are A, B and C. The cell at the center is called the 'device cell' which is initially at null state and it attains a polarization at once when all the input cells are at stable polarization state as shown in fig.4. The outermost cell is the output cell [8].

The expression for three input majority voter is given by (1).

$$M3(A,B,C) = AB + BC + AC \quad (1)$$

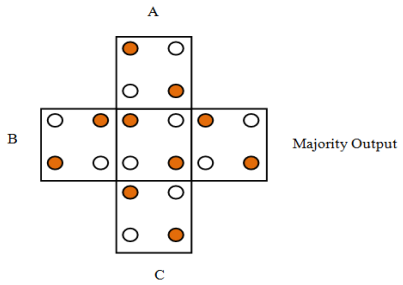

Fig. 4. Three input majority voter

E. Five Input Majrity Voter

Although QCA has many benefits; the design of complex architectures becomes tedious. The design task is difficult as all the architectures are drawn just by making use of three input majority voter,wire and inverter structure. In order to overcome the complexity in design, a new five input majority voter is introduced [9]. Fig.5 shows the five input majority voter. The expression for the five input majority voter is given by (2)

$$M5(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (2)$$

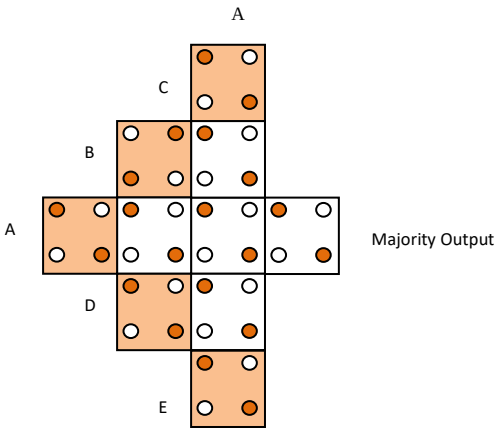

Fig. 5. Five input majority voter

III. Proposed ALU Design

The Arithmetic and logical unit (ALU) is a important part of Central Processing Unit . An ALU is a digital circuit that does arithmetic and logical operations. Arithmetic logic unit is a significant component of a microprocessor. An ALU performs operations such as addition, subtraction, increment, decrement, 'and', 'or', 'exor', 'not' [10]. The proposed ALU is simulated using the QCA Designer tool. In this paper, two layouts of 1 bit ALU are proposed and implemented.

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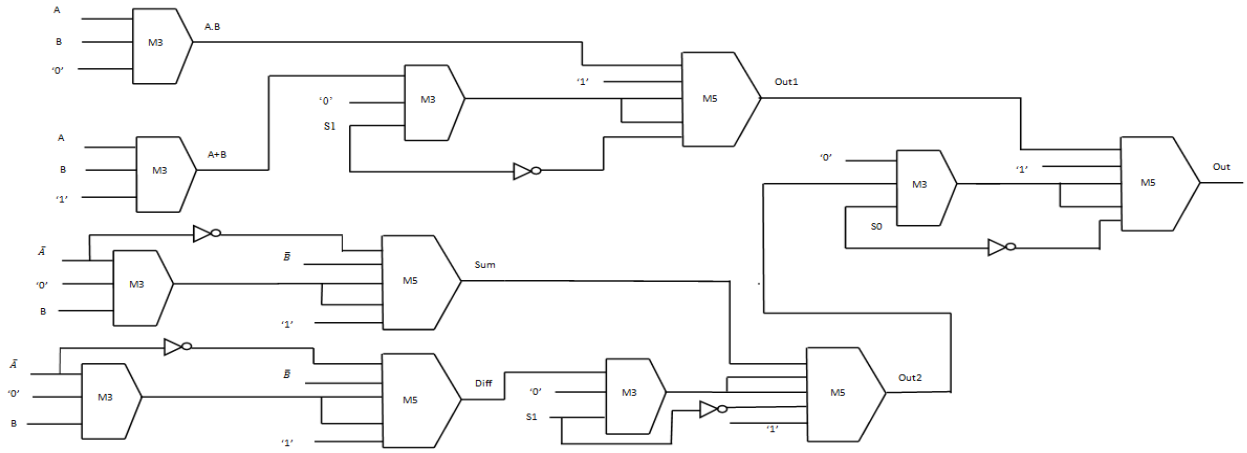

Fig. 6. Logic implementation diagram of proposed Type 1 ALU

The logic implementation of Type 1 structure is shown in fig.6. The first ALU performs the function of 'AND', 'OR', half adder 'Sum' and half subtractor 'difference'. The second architecture of ALU performs the functions of 'AND', 'OR', 'EXOR' and full adder 'Sum'. The 4:1 multiplexer is used in order to realize ALU functions.

The operands are the inputs given to the ALU and performs the operation based on code generated by control unit. Extremely efficient and complex ALUs are present inside the processors of CPU. More than one ALU might be required to compute all the operations [11].

By making use of majority voter, inverter and binary wire, any complex QCA structure can be developed. The basic logic gates such as AND, OR, NOT, EXOR etc can be realized in QCA. Two input 'AND' and 'OR' gate can be implemented by using three input majority voter gate; by setting one input as constant.

A. AND GATE

The boolean AND gives the output as '1' if both the inputs are '1', otherwise it gives a '0'. The majority voter can be used in the realization of the QCA based AND by setting one of its input to a fixed value '1' and the other two input are set as input driver cells [12]. The QCA design of two-input AND gate is as shown in fig.7(a).

The expression for three input majority voter based AND gate is given by (3)

$$M3(A,B,0) = A.B + B.0 + A.0 = A.B \quad (3)$$

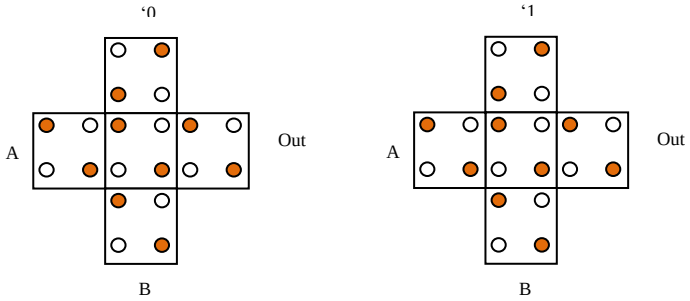

Fig. 7. (a)QCA based AND structure,(b) OR gate QCA structure

B. OR GATE

The OR gate can be realized using majority voter in the same way as AND gate. Instead of a fixed '0', a fixed '1' is given to one of QCA cell [13]. OR gate structure is shown in fig.7(b).

The expression for three input majority voter based OR gate is given by (4)

$$M3(A,B,1) = A.B + B.1 + A.1 = A + B \quad (4)$$

C. EXOR

The Exor is implemented by making use of three input majority voter and a five input majority voter. The Exclusive-Or is achieved by using the majority gate functions as shown in (5). The five input majority gate is used to implement the Exor function. Consequently, the Exclusive-or of A and B signals is produced in a different clocking zone. A high speed and single layer two-input XOR gate is introduced in a previous work. A five input majority gate along with two three-input majority gate and inverter is used to attain Exor functions as shown in (5).

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As illustrated in fig.8, Signal A, inverse of signal B, logic '1' are the inputs to the five input majority voter. The other two inputs are obtained from the output of the three input majority voter. Thus as a result, the Exclusive-or of A and B signals is obtained. The equation of two-input XOR gate as follows:

$$M5(A, M3(\bar{A}, 0, B), M3(\bar{A}, 0, B), \bar{B}, 1) \quad (5)$$
$$M5(A, \bar{A}B, \bar{A}B, \bar{B}, 1) = \bar{A}B + A\bar{B}$$

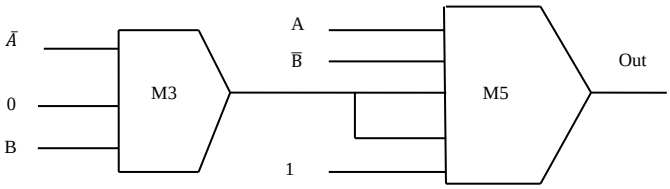

Fig. 8. QCA based EXOR gate logic diagram

D. HALF ADDER AND SUBTRACTOR

The half adder circuit is basically used to calculate the sum and carry of the two binary inputs fed to it. The equations of half adder sum and Carry is as given below:

$Sum = A \oplus B$
$Cout = A.B$

The most fundamental arithmetic logic circuits in digital systems are adder and subtractor circuits. Operation of adder and subtractor circuits is directly affected by the performance of digital systems [8]. In order to improve the performance of the arithmetic circuits several QCA based approaches are devised over the recent years. The half subtractors are implemented over a single layer. A half subtractor performs subtraction of two input A and B, and outputs the difference and borrow.

$Diff = A \oplus B$
$Borrow = \bar{A}.B$

E. FULL ADDER

The most significant mathematical operation is addition as other operations such as subtraction, multiplication, and division can be implemented by using the adders itself. Thus design of arithmetic circuits must be efficiently done [14]

$Sum = A \oplus B \oplus C_{in}$
$Cout = AB + BC + AC$

The QCA majority voter based equations for sum and carry is given by (6)

$$Sum = M5(A, B, M3(\mathrm{A}, B, C_{in}), M3(\mathrm{A}, B, C_{in}), C_{in})$$
$$Cout = M3(\mathrm{A}, B, C_{in}) \quad (6)$$

The fig.9 shows the logic diagram of the full adder circuit which is implemented using the five input majority voter,three input majority voters and inverters.

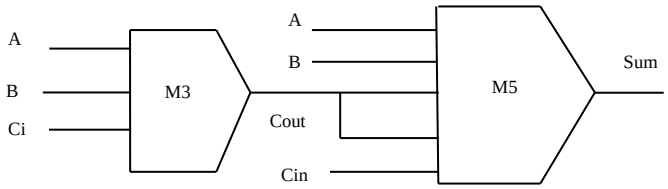

Fig. 9. QCA based full adder logic diagram

F. MULTIPLEXER

Multiplexers play a considerable role in applications where the desired input must flow onto the output. Implementation of multi-input multiplexer in a single layer is noteworthy. There are diverse structures that have been introduced in previous researches to realize multiplexers. These designs were implemented using combinations of three three-input majority gates, inverters in different ways. The cell count in each case where found to be different. An innovative methodology for designing 2-to-1 multiplexer is introduced in [1]. This design has a modular structure that consists of several elementary blocks as illustrated in fig.10.These designs have been implemented according to (7)

$M5(A, M3(B, 0, S), M3(B, 0, S), \bar{S}, 1)$
$M3(A, BS, BS, \bar{S}, 1) = A\bar{S} + BS \quad (7)$

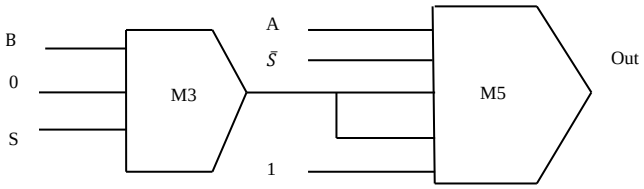

Fig. 10. QCA based 2:1 Multiplexer logic diagram

The 4:1 multiplexer is also implemented by using three 2:1 multiplexers that are based on five input majority voter. This design is less complex and efficient in terms of cell count and area. The fig.11 shows the logic diagram of the 4:1 Multiplexer which is implemented using the five input majority voter based three 2:1 multiplexers.

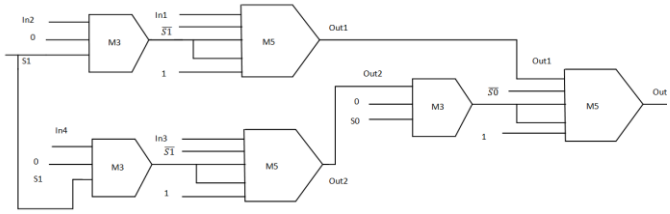

Fig. 11. QCA based 4:1 Multiplexer logic diagram

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IV. SIMULATION AND EXPERIMENTAL RESULT ANALYSIS

QCA Designer 2.0.3 open software tool is used for the simulation of the proposed work. The table 1 represents the default values of parameters under Coherence vector simulation engine in QCA Designer tool[15].

TABLE I. COHERENCE VECTOR PRAMETER MODEL

Parameter	Area
Temperature	1.000000K
Relaxation time	1.000000e − 15 s
Time step	1.000000e − 016 s
Total simulation time	7.000000e − 011 s
Clock low	9.800000e − 022 J
Clock high	3.800000e − 023 J
Layer separation	11.500000
Clock amplitude factor	2.000000
Radius of effect	80.000000 nm
Relative permittivity	12.900000

The basic gates implementation and verification of results is performed using QCA designer software. The fig.12 and fig.13 shows the simulation results of the basic AND gate and OR gate in QCA Designer using Coherence vector engine.

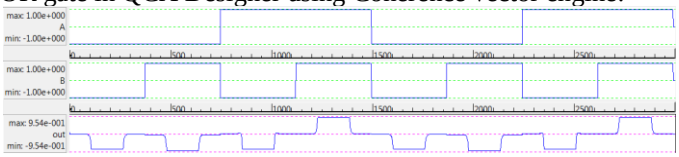

Fig. 12. Output waveform of QCA based AND gate

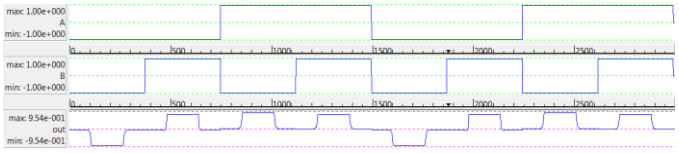

Fig. 13. Output waveform of QCA based OR gate

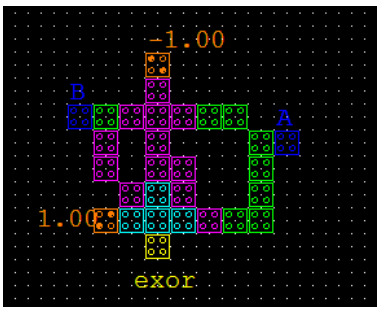

Fig. 14. QCA based EXOR gate implementation

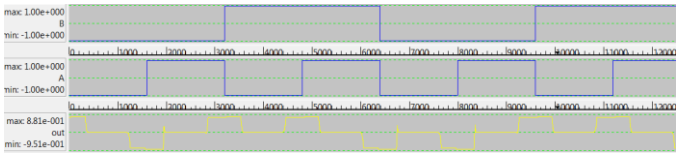

Fig. 15. Simulation result of QCA based EXOR gate

The fig.14 shows the implementation of the EXOR gate which is developed by using the five input majority voter and fig.15 shows simulation results of the five input majority voter based EXOR gate. The fig.16 shows the implementation of the 4:1 Multiplexer which is implemented using the five input majority voter based three 2:1 multiplexers and fig.17 shows simulation results of the five input majority voter based 4:1 Multiplexer. Cell count is 98 cells and the total area consumed for the implementation of 4:1 multiplexer is 0.21 um^2.

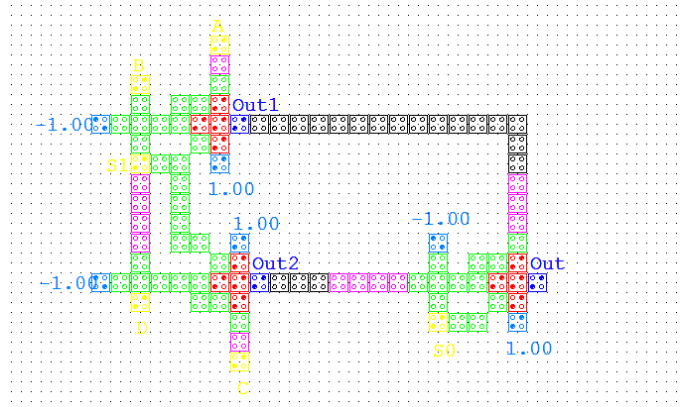

Fig. 16. QCA based 4:1 Multiplexer logic diagram

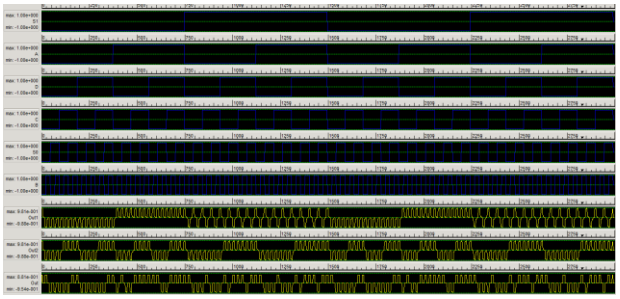

Fig. 17. Simulation results of QCA based 4:1 Multiplexer

Fig.18(a) shows the layout of Arithmetic and Logical Unit (Type 1) which performs four operations such as AND, OR, Sum and Difference. Fig.18(b) shows the layout of Arithmetic and Logical Unit (Type 2) which performs four operations such as AND, OR, EXOR and Full adder Sum.

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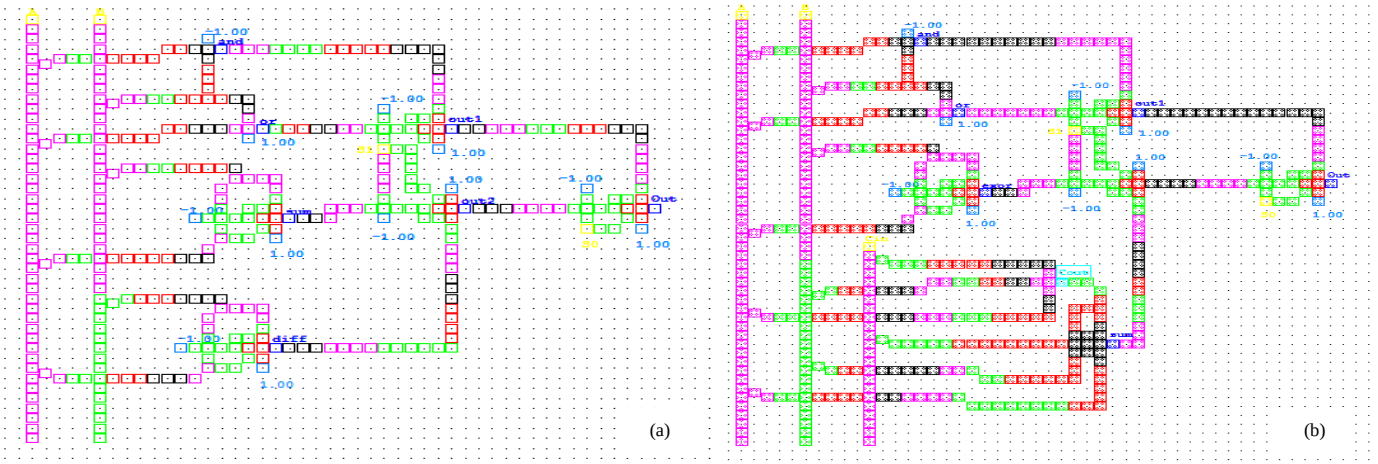

Fig. 18. (a)QCA based ALU layout(Type 1), (b)QCA based ALU layout(Type 2)

	Type 1	Type 2
Functions	AND,OR,SUM, DIFF	AND,OR,,EXOR, SUM
Cell Count	381	510
Cell area	0.86um2	0.98um2
Simulation time	230s	313s
No. of Clock Cycles	4	5

V. CONCLUSION

QCA Designer tool version 2.0.3 is used for the implementation and simulation of the proposed work. The proposed ALU layout is more efficient in area as the entire implementation involves the five input majority voter based design. This implementation of 1-bit ALU can be further expanded to created higher bit versions of ALU ranging from 2 bit to 64 bit. The proposed ALU structure has the advantage of being implemented in just a single layer. In future works, highly robust and more device density enhancement can be used in arithmetic and logic circuits that are much fault tolerant in digital systems.

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