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# Quad-Core Processors: New Way to Achieve High System Performance

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**Abstract:-** Multi-core processors significantly represent an evolutionary change in conventional computing as well setting the new trend for high performance computing (HPC). The move toward chip-level multiprocessing architectures with a large number of cores continues to offer dramatically increased performance and other characteristics. This move also presents significant challenges. This paper will show how far the industry has progressed and evaluates some of the challenges we are facing with multi-core processors and some of the solutions that have been developed.

## A. INTRODUCTION

Since the birth of microprocessors in 1971, the industry has successfully continued to innovate and improve performance. The architecture of a processor refers to the instruction set, registers, and data structures that are public to the programmer and are maintained and enhanced from one generation to the next. The micro-architecture of a processor is known as an implementation of processor's architecture in silicon, the micro-architecture is change from one processor generation to the next, while implementing the same public processor architecture. Process technology is known as a semiconductor circuit design process in silicon and the manufacturing methodologies used to create transistors which are increasingly smaller, faster and more power efficient. The output of this process is the production of a more sophisticated and integrated chip.

## B. PERFORMANCE AND PERFORMANCE-PER WATT CONSIDERATION

True performance is a proper combination of both clock frequency and IPC. On existing process technology 65 nm CMOS and micro architecture optimized for that frequency such as NetBurst we can easily achieve today 3.8 GHz maximally. If we analyze the NetBurst's based processors running today we can easily observe highest available speed 3.8 GHz and the thermal guideline 115 W. Unfortunately, leakage power limits frequency scaling.

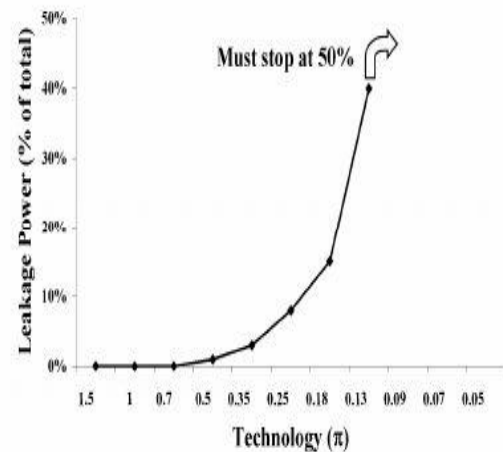


Figure 1. Leakage Power (% of total) vs. process technology

Intel first implemented a 64-bit integer

SIMD in 1996 has been the part of the Intel Pentium processor with MMX technology. The following implementation of SIMD was 128-bit SIMD single precision floating-point instructions (SSE), in the Pentium III processor which was introduced in 1999. Intel recently introduced new innovative techniques within their latest mobile microarchitecture, called micro fusion.

Micro fusion fuses many common micro-operations into a single micro-op, to reduce the total number of micro-ops necessary to execute a given task. Pure performance is important but we need to always consider the implications, when measuring the performance. Considering performance and power equations, CPU designers need to balance IPC efficiency from one side and voltage and frequency from the other to offer a compromise of performance and power efficiency of the processor.

New metrics of design success are no longer focused just pure performance, but also in delivering a new microarchitecture which delivers leadership in both raw performance and in performance per watt.

## C. MULTI-CORE: THE NEW INNOVATIVE

*design*

Dual and multi-core processor systems have changed the dynamics of the market and enable new innovative designs. Intel has more than 15 multi-core processor projects and is on the fast track to deliver multi-core processors in high volume across off of their platform families. In

addition to general-purpose cores, Intel multi-coreprocessors will eventually include specialized coresfor processing graphics, speech recognitionalgorithms, communication protocols, and much more.Many new innovations have been designed to optimize the power, performance, and scalability isimplemented into the new multi-core processors.Consider a dual-core processor from a system perspective and isrecognized as two separate CPUs.In such a configuration counting the number of theCPUs in the system becomes confusing from a software perspective so many vendors count numberm of sockets in the system instead of CPUs. Theclass of an implementation is primarily driven bymanufacturing cost efficiencies. TheMCP enables better overall yield and enable a'bin' as higher frequency dual core processors that can bepaired and frequency matched from anywhere on thewafer.The monolithic design usually has shared L2 cache whichincreases the efficiency of cache to processor coredata transfers, and also processor to processorcommunication.The difference between shared L2 cache dual-coreCPUs and independent caches for each corepopulating dual socket system illustrate Figure 2.

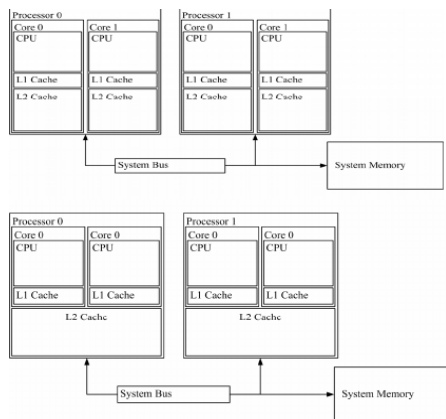


Figure 2. Dual socket system with different dual-core CPU L2 cache organization

The microarchitecture extends the energy-efficient philosophy, first delivered in Intel's mobile micro-architecture found in the Intel Pentium M processor family and optimized for the performance, and scalability of multi-core processors. The most important micro-architecture innovations are:

- Intel Wide Dynamic Execution
- Intel Intelligent Power Capability
- Intel Advanced Smart Cache
- Intel Smart Memory Access
- Intel Advanced Digital Media Boost

#### D. INTEL WIDE DYNAMIC EXECUTION

Intel Wide Dynamic Execution allows delivery of more instructions per clock cycle to improve execution time and energy efficiency. Every execution core is wider, which allows each core to fetch, dispatch, execute, and return up to four full instructions.

#### E. INTEL INTELLIGENT POWER CAPABILITY

Intel Intelligent Power Capability is a set of capabilities that are designed to reduce power consumption. It helps in managing the runtime power consumption of all the processor's execution cores. It includes an advanced power-gating capability that helps in an ultra fine-grained logic control that turns on individual processor logic subsystems when they are needed.

#### F. INTEL ADVANCED SMART CACHE

Intel Advanced Smart Cache is multi-core optimized cache that can improve performance and efficiency by increasing the probability that each execution core of a dual-core processor can access data from a higher-performance, more-efficient cache subsystem. By sharing L2 caches among each core, Intel Advanced Smart Cache can use up to 100% of L2 cache when needed. When one core has minimal cache requirements, other cores generate the ability to increase their percentage of L2 cache, reducing cache misses and increasing performance.

#### G. INTEL SMART MEMORY ACCESS

Intel Smart Memory Access includes an important new capability called memory disambiguation, which increases the efficiency of processing by providing the execution cores with an integrated intelligence to load data for instructions that are about to be executed before, are all previously stored instructions that are executed.

#### H. INTEL ADVANCED DIGITAL MEDIA BOOST

Intel Advanced Digital Media Boost is a feature which improves performance when executing SSE instructions. In the previous generation processors, instructions were executed of one complete instruction every two clock cycles. Intel Advanced Digital Media Boost enables 128-bit instructions to be executed during every clock cycle, effectively doubling the speed of execution for these instructions and raising the IPC ratio.

#### I. CONCLUSION

Platforms built around the dual-core processors are ideal for enthusiasts who crave computing power for audio, video, and gaming applications from one side and multitasking scenarios in business. Multi-core capabilities can enhance experiences in multitasking environments, such as, foreground applications run concurrently with a number of background applications such as virus protection and security, wireless, management, compression, encryption and synchronization.

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