# Quad–Core Processors: New Way to Achieve High System Performance

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***Abstract:-*** **Multi-core processors significantly represent an evolutionarychange in conventional computing as well setting thenew trend for high performance computing (HPC). The movetoward chip-level multiprocessing architectures witha large number of cores continues to offerdramatically increased performance and othercharacteristics. This move also presentssignificant challenges. This paper will show howfar the industry has progressed and evaluates some ofthe challenges we are facing with multi-coreprocessors and some of the solutions that have beendeveloped.**

## A. INTRODUCTION

Since the birth of microprocessors in 1971, theindustry has successfully continued to innovate andimproved performance. The architecture ofa processor refers to the instruction set, registers, anddata structures that are public to the programmer andare maintained and enhanced from one generation tothe next.The micro-architecture of a processor is known as animplementation of processor's architecture in silicon,the micro-architecture is change from oneprocessor generation to the next, while implementingthe same public processor architecture.Process technology is known as a semiconductorcircuit design process in silicon and themanufacturing methodologies used to createtransistors which are increasingly smaller, faster andmore power efficient. The output of this process is theproduction of a more sophisticated and integratedchip.

## B. PERFORMANCE AND PERFORMANCE-PER WATT CONSIDERATION

True performance is a proper combination of both clockfrequency and IPC. On existingprocess technology 65 nm CMOS and micro architecture optimized for that frequencysuch as NetBurst we can easily achievetoday 3.8 GHz maximally. Ifwe analyze the NetBurst's based processors runningtoday we can easily observe highest available speed 3.8 GHzand the thermal guideline 115 W. Unfortunately, leakage power limits frequency scaling.

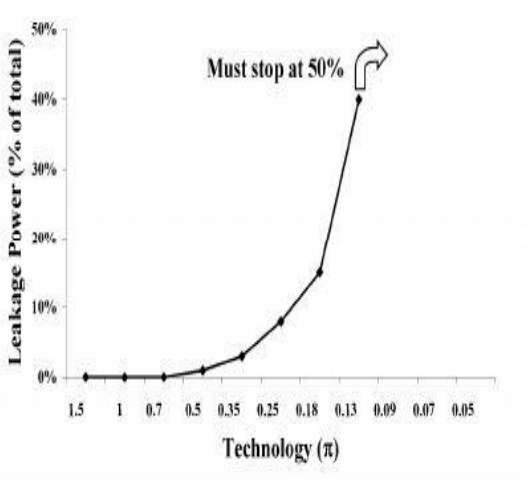


Figure 1. Leakage Power (% of total) vs. process technology

Intel first implemented a 64-bit integer

SIMD in 1996 has been the part of the Intel Pentium processorwith MMX technology. The followingimplementation of SIMD was 128-bit SIMD singleprecisionfloating-point instructions (SSE), in thePentium III processor which was introduced in 1999.Intelrecently introduced new innovativetechniques within their latest mobile microarchitecture, calledmicro fusion.

Micro fusion fusesmany common micro-operations into a single microop, to reduce the total number of micro-ops necessaryto execute a given task.Pure performance is important but we need toalways consider the implications, when measuring the performance.Considering performance and power equations, CPU designers need to balance IPCefficiency from one side and voltage and frequencyfrom the other to offer a compromise of performanceand power efficiency of the processor.

New metrics of design success are no longer focused just pureperformance, but also in delivering a new microarchitecturewhich delivers leadership in both rawperformance and in performance per watt.

## C. MULTI-CORE: THE NEW INNOVATIVE

*design*

Dual and multi-core processorsystems have changed the dynamics of themarket and enable new innovative designs.Intel has more than 15 multi-coreprocessor projects and is on the fast trackto deliver multi-core processors in high volumeacross off of there platform families. In

addition to general-purpose cores, Intel multi-coreprocessors will eventually include specialized coresfor processing graphics, speech recognitionalgorithms, communication protocols, and much more.Many new innovations have been designed tooptimize the power, performance, and scalability isimplemented into the new multi-core processors.Consider a dual-core processor from a system perspective and isrecognized as two separate CPUs.In such a configuration counting the number of theCPUs in the system becomes confusing from asoftware perspective so many vendors count numberm of sockets in the system instead of CPUs. Theclass of an implementation is primarily driven bymanufacturing cost efficiencies. TheMCP enables better overall yield and enable a‘bin’ as higher frequency dual core processors that can bepaired and frequency matched from anywhere on thewafer.Themonolithic design usually has shared L2 cache whichincreases the efficiency of cache to processor coredata transfers, and also processor to processorcommunication.The difference between shared L2 cache dual-coreCPUs and independent caches for each corepopulating dual socket system illustrate Figure 2.

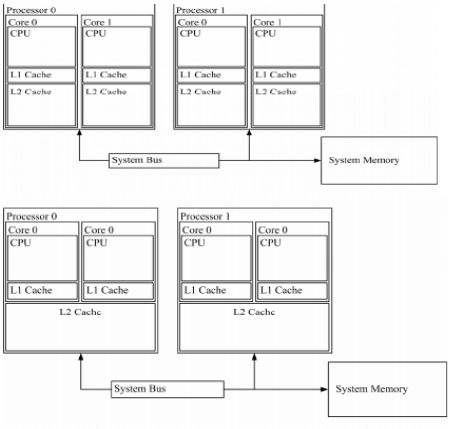


Figure 2. Dual socket system with differentdual-core CPU L2 cache organization

The microarchitectureextends the energy-efficient philosophy,first delivered in Intel’s mobile micro-architecturefound in the Intel Pentium M processor family andoptimized for the performance, and scalability ofmulti-core processors.The most important micro-architecture innovations are:

- Intel Wide Dynamic Execution
- Intel Intelligent Power Capability
- Intel Advanced Smart Cache
- Intel Smart Memory Access
- Intel Advanced Digital Media Boost

## D. INTEL WIDE DYNAMIC EXECUTION

Intel Wide Dynamic Execution allows delivery ofmore instructions per clock cycle to improveexecution time and energy efficiency. Everyexecution core is wider, which allows each core to fetch,dispatch, execute, and return up to four full instructions.

## E. INTEL INTELLIGENT POWER CAPABILITY

Intel Intelligent Power Capability is a set ofcapabilities that are designed to reduce power consumption.It helps in managing the runtime power consumptionof all the processor’s execution cores. It includes anadvanced power-gating capability that helpsin anultra fine-grained logic control that turns onindividual processor logic subsystemswhen they are needed.

## F. INTEL ADVANCED SMART CACHE

Intel Advanced Smart Cache is multi-coreoptimized cache that can improve performance andefficiency by increasing the probability that each execution core of a dual-core processor can accessdata from a higher-performance,more-efficient cachesubsystem. By sharing L2 caches among each core, IntelAdvanced Smart Cache can use up to 100 % ofL2 cache when needed. When one corehas minimal cache requirements, other cores generate the ability toincrease their percentage of L2 cache, reducing cachemisses and increasing performance.

## G. INTEL SMART MEMORY ACCESS

Intel Smart Memory Access includes an importantnew capability called memory disambiguation, which increases the efficiency of processing byproviding the execution cores with an integratedintelligence to load data for instructionsthat are about to be executed before, are all previouslystored instructions that are executed.

## H. INTEL ADVANCED DIGITAL MEDIA BOOST

Intel Advanced Digital Media Boost is a featurewhich improves performance whenexecuting SSE instructions. In the previous generation processors, instructions were executed of one completeinstruction every two clock cycles. Intel AdvancedDigital Media Boost enables 128-bit instructions to be bexecuted during every clock cycle, effectivel doubling the speed of execution for these instructionsand raising the IPC ratio.

## I. CONCLUSION

Platforms builtaround the dual-core processors are ideal forenthusiasts who crave computing power for audio,video, and gaming applications from one side and multitasking scenarios in business. Multi-core capabilities can enhanceexperiences in multitasking environments, such as,foreground applications runconcurrently with a number of backgroundapplications such as virus protection and security,wireless,management, compression, encryption andsynchronization.

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