International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 2 Issue 11, November - 2013

PWM For Single Phase Five level Transistor Clamped Strategies H Bridge Inverter With Voltage Boosting Capacity

K.Rachel, U.Ramesh

PG scholar,pandian saraswathi yadav engineering college,sivaganga

Assistant Professor of EEE,pandian saraswathi yadav engineering college,sivaganga

Abstract

This project presents a new technique for getting a multilevel output and also uses PWM control techniques. This new type of converter is suitable for high voltage and high power applications.This paper presents a new topology of the multilevel inverter with feature like output voltage boosting capability along with capacitor voltage balancing .The proposed multilevel inverter uses transistor clamped H-bridge (TCHB) with an bidirectional switch and four auxillary switches producing a boost output voltage. The proposed topology results in reduction of the number of switches,losses,installation area,and converter cost It provides a high equalization efficiency. The analysis of the output voltage harmonics is carried out and compared with conventional cascaded H-bridge inverter topology. From the results,the,compared with proposed and conventionl topology was simulated by using MATLAB_SIMULINK

Keywords— multilevel inverter; cascaded H-bridge; multicarrier pulse width modulation; transistor clamped inverter, cascaded neutral –point clamped inverter .

1.INTRODUCTION

Multilevel voltage source inverter is recognized as an important alternative to the normal two level voltage source inverter especially in high voltage application.[1] There are various application varying from medium voltage to high voltage high power application which requires DC to AC conversion using multilevel inverters.[2] The research on multilevel inverter is ongoing further to reduce the number of switching devices count to reduce the manufacturing cost, capacitor voltage balancing. The inverters with number of voltage levels equal to three or above than that are known as the multilevel inverters.[3] Using multilevel technique, the amplitude of the voltage is increased, stress in the switching devices is reduced and the overall harmonics profile is improved. Among the familiar topologies, the most popular one is cascaded multilevel inverter. The cascaded multilevel inverter switching signals are derived from the proposed triangular-sampling current controller that results in a good dynamic performance under both steady state and transient operations.[5] The novel universal multi-carrier PWM control scheme is used .This paper mainly focuses mainly on the cascaded H-bridge inverter topology. Transistor clamped topology is popular now a days as it provides provision to increase the output levels by taking different voltage levels from the series stacked capacitors [6], [7]. In this paper the new configuration of the (symmetrical H-bridge) single phase 5-level inverter is proposed which produces a five-level output voltage instead of three-level as in case of conventional H-bridge.[8] Also this new proposed topology produces the boost output voltage in comparison to conventional H-bridge topology which requires two H-bridge cells producing the five-level output voltage but the output voltage equal to the input DC voltage.[9] However, in the proposed approach only calculation of real power (p) losses are conducted.[10],[11] This method is simple and different from conventional methods;it provides effective compensation for harmonics.

II.PROPOSED SYSTEM

In this proposed system series-connected five-level TCHB cells to reduce the switch count and THD minimization [1]. The main of the proposed system is inverter provides higher output quality with relatively lower power loss as compared to the other conventional inverters with the same output quality.The general block diagram for the proposed inverter is shown in fig and the general configuration of the proposed inverter topology is shown in , which also represents a single cell which produces the five-level output with boost output voltage. It consist of total of four main controlled switches and five auxillary switches including an additional bidirectional switch consisting of S11 and S11' in a single cell which is connected between the first leg of the H-bridge and the capacitor midpoint, enabling five output voltage

levels (+2Vdc, +Vdc, 0, -Vdc, -2Vdc) based on the switching combination . [3]The switches S21, S31, S41, S51 forms the H-bridge and the remaining switches Sa1, Sa2, Sa3, Sa4 are auxillary switches connected in the same leg which plays a role in boosting the voltage and the input DC voltage is connected with positive terminal between the switches Sa1 and Sa2 and the negative terminal between the switches Sa3 and Sa4. The capacitor voltage divider is formed by C1 and C2. [5]

BLOCK DIAGRAM

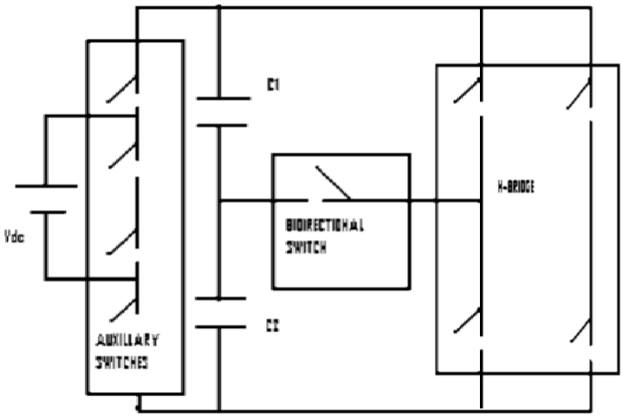

Table 1:Switiching pattern for proposed

Voltage level	+2vdc	+vdc	0	-vdc	-2vdc
Sa1	0	0	0	1	0
Sa2	0	1	0	0	0
Sa3	0	0	0	1	0
Sa4	0	1	0	0	0
S11	0	1	0	1	0
S21	1	0	1	0	0
S31	0	0	0	0	1
S41	0	0	1	1	1
S51	1	1	0	0	0

III.MODULATION TECHNIQUES FOR CONTROL SCHEME

There are many modulation techniques for multi-level inverters. Multilevel inverter has to synthesize a staircase waveform by using the modulation technique to have the controlled output voltage [1].Carrier based modulation (SPWM) technique is easy and efficient. The level-shifted PWM (LS-PWM) and phase-shifted PWM (PS-PWM) techniques have been the natural extensions of carrier-based sinusoidal PWM (SPWM) and for multicell converters (CHB and FC), respectively. The LSPWM, which is also known as phase-disposition PWM (PDPWM), and other carrier disposition variants.[2],[3] For any given number of levels in the output voltage the number of carrier to be used is given as N-1 Where N is the number of levels in the output voltage.represents the triangular shape carrier waveform and the sinusoidal reference signal showing the pulse width modulation technique used for the control.[6] This method has the advantage of having very few commutations per cycle and is therefore the one that achieves better efficiency and enables air cooling.

1V. simulation results

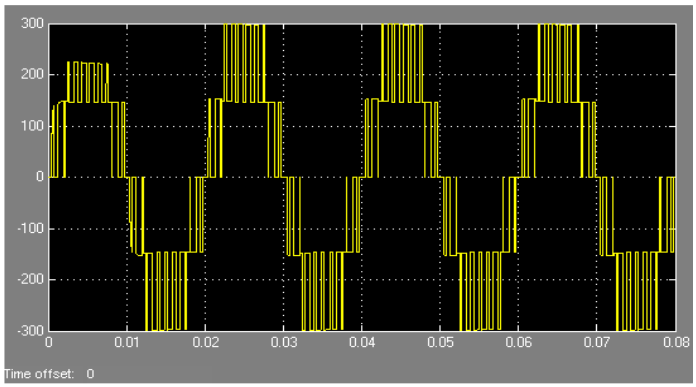

Fig1.Output voltage waveform of the proposed Single-phase 5-level inverter using PWM

The fig 1 shows that output voltage.This will boost the voltage upto 300.

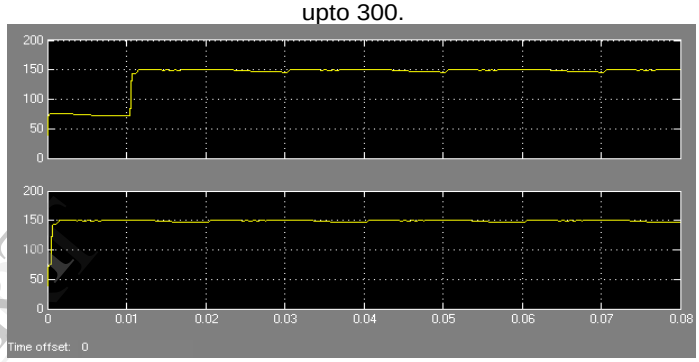

Fig.2.Waveform of the voltage across the capacitors C1 & C2

The fig 2 shows the voltage raise in the capacitor.

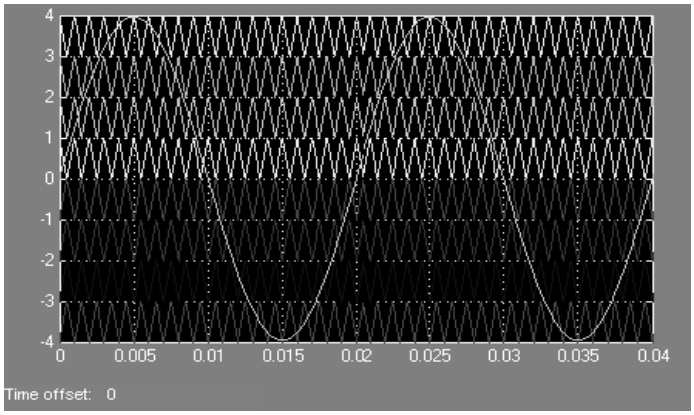

fig3.Multicarrier based PWM control scheme

the fig 3 shows the modulation index as 1.this will tell the THD rating.

V. ANALYSIS AND COMPARISON OF PROPOSED WITH CONVENTIONAL MLI

In the proposed 5-level multilevel inverter topology the number of switches is only one more then the 5-level single phase cascaded H-bridge inverter. To produce the same output voltage the cascaded H-bridge has to use the two cells where as only one cell is required with the proposed topology. The total harmonic distortion produced by the proposed inverter is 38.11% only, Fig.6 shows the THD in % for single phase 5-level proposed multilevel inverter which is very low as compared to the single unit of conventional H-bridge inverter having THD of 70.99%. In order to produce the nine levels in the output voltage the conventional H-bridge requires three cells where as the proposed topology requires only two cells.

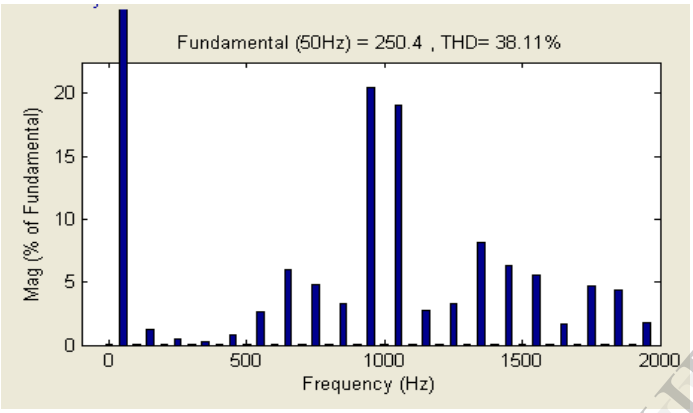

TABLE 2:ANALYSIS OF THD RATING

Ma	Ff	Cf	Thd
1	1.110	1.414	5.43
0.95	1.110	1.414	5.99
0.9	1.110	1.414	6.13
0.85	1.109	1.414	6.21
0.8	1.11	1.414	6.88

V1.CONCLUSION

A new topology of multilevel inverter with feature like output boosting capability along with capacitor voltage balancing uses transistor clamped h-bridge(TCHB) with biderictional switch and four auxillary switches produced a boost output voltage was analysed and simulated by using MATLAB_SIMULINK

REFERENCES

[1] Nasrudin Abd. Rahim, Mohamad Fathi Mohamad Elias, Wooi Ping Hew, "Transistor-Clamped H-Bridge Based Cascaded Multilevel Inverter with New Method of Capacitor Voltage Balancing" August 2,2011; revised November 22, 2011 and February 27, 2012. Accepted for publication April 8,2012.

[2] Rashid, M.H, 2004. "Power Electronics: Circuits, devices an applications. Third Edition, Prentice Hall.

[3] S.Mukherjee and G. Poddar, "A Series-Connected Three-Level Inverter Topology for Medium-Voltage Squirrel-Cage Motor Drive

[4] P. Lezana and G. Ortiz, "Extended Operation of Cascade Multicell Converters Under Fault Condition," Industrial Electronics, *IEEE*

[5] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey topologies, controls, and applications," IEEE Transaction on Industrial electronics, vol. 49, no. 4, pp. 724–738, Aug. 2002

[6] Ebrahim Babaei, 2008, "A Cascade Multilevel Converter Topology With Reduced number of switches"IEEE transaction on power electronics, Vol. 23, No.6I

[7] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo,B.Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters,"*IEEE TransInd.Electron.*, vol. 57, pp. 2553-2580, 2010. Nasrudin Abd. Rahim, Mohamad Fathi Mohamad Elias, Wooi Ping

[8] Gerardo Ceglia, Víctor Guzmán, Carlos Sánchez, Fernando Ibáñez, JulioWalter, and María I. Giménez "A New Simplified Multilevel Inverter Topology for DC–AC Conversion" IEEE Transactions on Power Electronics,Vol. 21, No. 5, September 2006.

[9] Gupta, Krishna Kumar; Jain, Shailendra; , "A novel universal control scheme for multilevel inverters," Power Electronics, Machines and Drives(PEMD 2012), 6th IET International Conference on , vol., no., pp.1-6, 27-29 March 2012

[10] L. M. Tolbert, F. Z. Peng, T. G. Habetler, "Multilevel PWM methods at low modulation indices," IEEE Transactions on power electronics, vol. 15, no. 4, July 2000, pp. 719-725

[11] S.Khomfoi and L. M. Tolbert, "Fault Diagnosis and Reconfiguration For Multilevel Inverter Drive Using AI-Based Techniques," *IEE E Trans.Ind.Electron.*, vol. 54, pp. 2954-2968, 2007.