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# PV System based Cascaded Multilevel Inverter: A Critical Review

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***Abstract*— This paper presents a single-stage circuit topology consisting of the association of a full-bridge isolated dc–dc converter and two input inductors and two input diodes connected to the mains network, in order to obtain an isolated ac/dc switch mode power supply, with sinusoidal input current. The topology does not use an input bridge rectifier, common in similar applications. The current in the two input inductors can therefore, flow in both directions. Consequently, the different topology equally distributes the current by the four-bridge transistors that provide four input parallel boost power factor correctors (PFCs). The use of the four bridges permitting the accurate simultaneous regulation of output voltage and input current is hereby described.**

***Keywords*— Full-bridge converters, Input current shaping, low-distortion input current, single-stage power factor correctors (PFCs)***

## I. INTRODUCTION

In modern technology, power electronics and processor plays a vital role in the field of motor control, light control, heat control, power supplies, vehicle system, HVDC, FACTS and renewable applications. The philosophy focuses on preserving the energy and meeting the power demand accurately and the power modulator pertaining to inverter / converter technology fulfills the requirements and this attracts the researchers to explore in the inverter field. The above-mentioned applications work in the range of medium power, high power at a higher voltage. With the help of semiconductor device technology, power converters are to be designed with higher operating voltage. As a single device fails to support such high voltages, a number of devices need to connect in series to meet the voltage rating. Another challenge in the industrial sector is the requirement and maintenance of the sinusoidal power supply with variable voltage and frequency. The above demerits are overcome by the introduction of Inverters. The series connected switches in the inverters and through control mechanism, the voltage stress with respect to high voltage rating is shared among the series switches and also the losses are minimized. Due to advantage of minimum losses, inverters is also used for medium voltage applications. The classical square wave inverter operating at higher voltage introduces the dominant harmonics, thereby the performance on the load side and on the front end of the inverter has a large impact and the performance is affected. Though the solution is sought through the passive filters, the loss are increased and occupies more space. The alternative path is provided by Multilevel Inverters (MLI). MLI generates sinusoidal voltage waveform in the form voltage steps through switching sequence. The other advantages of MLI are reduced electromagnetic interference, reduced current distortion, good quality voltage waveform, good current waveform. The basic types of MLI are neutral point clamped MLI, flying capacitor MLI and cascaded H- bridge MLI. To synthesize nearly sinusoidal voltage, higher number of levels needs to be generated with the help of more number of switches, more number of sources and more number of gate drivers. Due to this, the efficiency decreases as more number of switches are utilized in the conduction path.

## II. LIITERATURE REVIEW

The topology suggested in (Abderezak Lashab et al. [1]) comprises of a combination of three-level (3L) active neutral-point-clamped inverter and floating capacitor connected parallel to the legs of H-bridge. Two switches operated at fundamental frequency are connected across the DC link structure and enhances the topology performance by a two-fold increase in RMS value. Through logical mapping, the switches are turned on /off by deriving the pulses through voltage balancing scheme and the scheme balances the floating capacitor voltage regardless of load angle.

Cascading five-level diode clamped MLI with seven level or 9 level conventional Cascaded H Bridge (CHB) Multilevel Inverters (MLI) results in hybrid topology (A. Lashab et al., [2]) for generating 11-level / 13-level respectively. The conventional MLI has a case to case merits and demerits. In the presented topology, the demerits of the conventional topology are minimized by cascading two different conventional topologies. The MLI switches at the fundamental frequency and the operation is shown for a particular modulation index and variable load angle. Capacitor balancing is attained between the charging cycle and the recharging cycle.

A new symmetric structure for cascade multilevel converter is developed in (Q. Huang et al., [3]) which is composed of several series-connected switched capacitor diode units and an H-Bridge inverter for polarity reversal. A fewer number of device count is required for configuring the topology. Besides, optimal structures derived from the topology projects the merits by maximizing the number of levels with different objectives such as a minimum number of switch count and sources. The simulation and experimental results added to show the performance of the implemented method and the results are compared with other structures.

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MLI structure using a cascade connection of sub multilevel inverter by (M. Abarzadeh et al., [4]). The sub-MLI consists of a switched-capacitor converter circuit with inherent boosting and capacitor self-balancing through a series-parallel connection operated in asymmetric mode. The main advantage of the topology is low voltage stress, because the H bridge is not used and the other merit is providing a conduction path for the inductive load reverse current. The topology is validated by simulation and by experiment.

A. Lashabet et al. [5], in this work, the near-state pulse width modulation (NSPWM), adjusted to be utilized as a part of dual-voltage source inverter (VSI) fed open-end load, is acquainted essentially pointing with obviously limit the voltage add up to harmonic distortion (THD). Inside the framework of the strategy, the active time of pulses at the second inverter is moderately balanced inside switching interim (contrasted with the principal VSI). The phase voltage harmonics are detailed for dual-inverter regulated by NSPWM; at that point, ideal change is distinguished by means of a three-dimensional bend of phase voltage THD versus modulation file (MI) and phase edge displacement (PAD). Because of the restriction of MI in NSPWM, the coveted yield voltage is orchestrated with altering MI as well as PAD between references of two VSIs. Moreover, NSPWM naturally exploits better productivity contrasted with traditional space vector modulation because of switching just two phases inside an interim (by clipping one phase to positive/negative dc-rail). The dual-VSI provided by two isolated dc sources is amassed in the lab to tentatively assess the THD diminishment highlight of the implemented technique; additionally, the simulation comes about acquired by methods for a MATLAB/Simulink condition indicate close concurrence with exploratory information.

From a single DC source, step-up voltage with twice the value is obtained in the Switched Capacitor Cell (SCC) developed by (C. Wang et al., [6]) with the help of capacitor self-balance by activating the corresponding switches in the charging mode and discharging mode. The SCC has six switches, two diodes and one DC source and two capacitors. When compared with CHBMLI, the total component count is reduced. The essential cells are cascaded to get asymmetric MLI and from the 25 level prototype, the analysis is validated.

Y. P. Siwakoti et al. [7], in this investigation, the near-state pulsewidth modulation (NSPWM), adjusted to be actualized in dual-voltage-source inverter (VSI) fed open-end engine, is implemented with the point of relieving low-arrange harmonics (which prompt current aggregate harmonic distortion (THD) minimization). The accompanying two developed techniques are examined in detail: 1) settling phase edge displacement (PAD) between two VSIs to 120° while altering the modulation record (MI); and 2) settling MI to the foreordained esteem (wherein low-arrange harmonics are profoundly relieved) while modifying PAD.

A. K. Yadav et al. [8], besides, the approaches improve effectiveness by restricting the quantity of replacements inside the switching interim. The examination likewise displays the numerical approaches to accurately decide low-arrange harmonic segments and switching losses for dual-VSI structure. The exploratory setup, including dual-VSI and open-end induction engine, is collected in the lab to assess execution of the implemented technique. At long last, the simulation comes about, completed in the MATLAB/Simulink condition, are observed to be in close concurrence with exploratory information.

Inherent capacitor charge balancing MLI using basic cell by (W. Li et al., [9]) works in symmetric and asymmetric mode. The basic cell consists of two DC source, two capacitors, six unidirectional switches and one bidirectional switch. The six unidirectional switches are arranged in each leg of a square with two switches in the vertical leg and one switch in the horizontal leg. The bidirectional switch connects the left side capacitor to the central point of the vertical leg.

D. Cui et al. [10], extend the procedure to connect the other capacitor on the other side. One DC source is connected parallel to the vertical leg on the left side. The remaining DC source is connected on the right side of the vertical leg with polarity reversed. Similar basic cells are cascaded to form the MLI structure and four types of magnitude algorithms are investigated to obtain the number of levels. Multi Carrier (MC) Pulse Width Modulation (PWM)is adopted and the steady-state and dynamic results are projected.

The topology shown in (W. Sheng et al., [11]) generates five-level using a single DC source and reduced components compared to five-level CHBMLI under symmetric mode. Using split capacitors and by self-charge balance, the peak value of voltage across the capacitor equals the DC source voltage. From a single DC source, two more sources are derived, hence the topology is called a step up MLI. The pulses derived by the modified Phase Shifted (PS) PWM scheme has only one carrier wave for testing the model.

A new reduced component topology overcoming the drawback of Cascaded Transformer Multilevel Inverter (CTMI) has been presented in (H. Tian et al., [12]). This topology requires 50% of switching devices and gate drivers in par with conventional CTMI for generating the desired voltage levels using a single DC source. Reliability based on the Markov evaluation approach and the Mean Time to Failure of the converters has been investigated to prove the enhancement of the topology.

Using transformer and semiconductor devices with a single DC source and two split capacitors, Cascaded Multilevel Inverter (CMLI) is constructed by (Y. P. Siwakoti et al., [13]). The semiconductor device such as unidirectional and bidirectional devices are used. The turns ratio of the transformer depends upon the symmetric and asymmetric mode. In symmetric mode, the turns ratio is equal whereas for asymmetric it is unequal. Through proper switching sequence, the stepped voltage is obtained across the series

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connected transformer. As the configuration is constructed without the utilization of H bridge, the blocking voltage of the switches is reduced reasonably and the results prove the effectiveness of the topology.

N. D. Dao et al. [14], three-phase MLI based on three-phase transformer connection through H bridge by (F. Rong et al. [15]) under equal voltage ratio for seven-level configuration is demonstrated by controlling the switches through three different schemes namely fundamental, Sine Pulse Width Modulation (SPWM) and Selective Harmonic Elimination (SHE)PWM. The pulses are derived using the FPGA processor. The results are investigated and compared with the conventional types.

H. Wang et al., [16], in this examination work, angular modulation list (AMI) actualized through an altered space vector modulation for the dual voltage source inverters (VSI) is implemented with the fundamentally meaning to lessen switching losses. The coveted voltage across the load is blended by applying suitable phase-point displacement between space vector references. The approach maintains a strategic distance from the utilization of a dc/dc boost converter (which forces loss and weight/value punishment to copy the dc-connect voltage) and results to be especially appropriate for electrical/mixture vehicle applications. In particular, the use of sparing energy to continue driving has been distinguished as real concern. Thus, this work centers around the system to improve proficiency.

G. Farivar et al. [17], the standards of the controlling strategy and switching loss, which is decreased at any rate by half, are hypothetically assessed. This work proposes a spearheading scientific approach to effectively decide add up to harmonic distortion (THD) estimation of the voltage/current for the dual-VSI structure. Moreover, simulation and exploratory outcomes demonstrate that the developed technique safeguards benefits as far as normal mode voltage, THD of the voltage, and switching loss decrease. The dual-VSI model providing 1.5-kW induction engine is gathered in the research center to tentatively assess execution of the developed technique. Likewise, the simulation comes about helped out through MATLAB/Simulink condition are given to affirm execution of this simple to-actualize and high-proficient technique.

Y. Yu et al. [18] a four-level five-phase open-end winding (OeW) drive topology is presented in this investigation. The drive involves a five-phase induction machine with open-end stator windings, provided utilizing two-level voltage-source inverters with isolated and unequal dc-interface voltages, in the proportion 2 : 1. The topology offers the benefits of a measured structure with less semiconductor segments and has a more noteworthy potential for fault tolerance, as contrasted and a comparable single-sided four-level drive. Because of the extensive number of switching states, advancement of a reasonable space vector pulsewidth-modulation (PWM) strategy can be testing. Subsequently, this work looks at the execution of two-level-moved transporter based PWM strategies.

J. I. Leon et al. [19], the impact of dead time on the drive execution is talked about, and it is demonstrated that synchronous PWM switching of the two inverters can prompt debased yield phase voltage waveforms. Nitty gritty investigation of this wonder is introduced, an answer is implemented, and the changed modulation systems are joined in a trial setup, at first in conjunction with $V/f$ control. Once the verification of idea has been given, full field-situated control is executed in this OeW drive topology out of the blue; definite exploratory testing is directed, and comes about are accounted for.

Y. Yu et al. [20], this work investigates the dual inverter driven open-end perpetual magnet synchronous engine (PMSM) system and proposes control technique which can produce most extreme yield power in general speed extend for incorporated starter/alternator. Dual inverter driven open-end machine system comprises of two inverters which are associated with the two closures of the machine winding. By separating one inverter from the power source, the dc-interface voltage of flying capacitor can be boosted through the machine. Since one inverter is associated with the main power source, yield power of the machine is managed by the source associated inverter.

H. Snani et al. [21], in this investigation, modulation strategy for expanding yield power of inverter and engine with decreased harmonic and loss is implemented. It is a cross breeds modulation joining six-advance and pulse width modulations. With strategy, proficiency and task territory are enhanced and cost of whole driving system is likewise diminished because of the expelling of dc-dc converter. Investigations, methodologies, control strategy, and simulation comes about are descripted. The trials with PMSM are accomplished to confirm the attainability of developed technique.

Bayhan et al. [22], a dual-inverter with an open-end winding motor setup is an attractive technique to supply a higher voltage to an engine for electric vehicle (EV) applications. A topology using two isolated dc sources is considered to procure the benefits of dependability and high voltage. In spite of the fact that this design may require two battery chargers, in this examination, the utilization of just a single charger to a fundamental battery was considered. The central issue is to charge the auxiliary battery from the principle battery by means of the engine, regardless of whether it is at a halt or running. The inverter voltage edge staying after engine torque generation decides the charging capacity. The solidarity power-factor task is appeared to be valuable to amplify the charging power. Simulations and trials are displayed that demonstrate the legitimacy of the plot.

R. J. Wai et al. [23], a near-state three-dimensional space-vector modulation (NS 3-D SVM) switching plan, which means to diminish the basic mode commotion in a three-phase four-leg voltage source inverter, is implemented. The impact of basic mode clamor, which is identified with electromagnetic impedance issues for a high-voltage level

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four-leg system, is explored first. Distinguishing proof of the segment in a 3-D space, choice of the near-state switching vectors, and arrangement of the chose switching vectors are then acquainted in ventures with depict the switching plan. The switching plan depends on traditional 3-D SVM, creating higher dc-interface use, less harmonic substance, and decreased switching loss contrasted with sinusoidal PWM. Hypothesis, simulation, and trial come about demonstrate that the near-state 3-D SVM can work under both adjusted and unequal load conditions.

L. S. Yang et al. [24], this work presents examinations on current swell in a dual 2-level inverter encouraging an open-end winding induction engine drive. Pulsewidth modulations (PWMs) for the freely controlled inverters are actualized utilizing a basic powerful time placement influenced by counterbalance time idea, accordingly, disposing of the utilization of segment distinguishing proof and query tables. Diagnostic articulations for swell substance in the engine phase current are produced and a present direction is hypothetically gotten straightforwardly from the switching conditions of the dual inverter in a stationary reference frame. Furthermore, this work likewise portrays a present swell direction in the engine by investigating the opportunity of autonomously working the individual inverters with various PWMs.

F. L. Luo et al. [25], in view of the investigation, intermittent PWMs are utilized for the individually inverters that not just offer the upside of diminishing the aggregate switching substitutions in the inverters yet in addition decreases the present swell. Explanatory articulation for the RMS swell current and variety in RMS swell current in one cycle of activity for various PWMs are likewise introduced for the whole speed scope of the dual-inverter drive. The execution of the dual-inverter drive with the PWM variations is first concentrated scientifically and afterward checked by performing reasonable investigations on a 1-kW open-end winding induction engine drive.

## III. MULTI LEVEL INVERTER

Figure 1 shows the multilevel converter modulation methods. The modulation control schemes for the multilevel inverter can be divided into two categories, fundamental switching frequency and high switching frequency PWM such as multilevel carrier-based PWM, selective harmonic elimination and multilevel space vector PWM Multilevel SPWM needs multiple carriers. Each DC source needs its own carrier. Several multi-carrier techniques have been developed to reduce the distortion in multilevel converters, based on the conventional SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals. By generalizing, for an ‘n’ level multilevel inverter, (n-1) carriers are needed. The implementation of the various carrier PWM techniques that is possible for multi-level inverters are [26-29]:

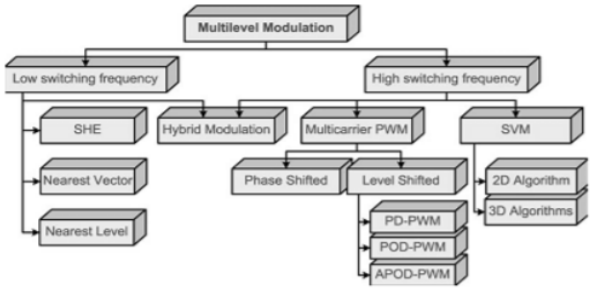


Figure 1: Multilevel converter modulation methods

### *Level Shifted PWM (LSPWM)*

This modulation method is especially useful for NPC converters, since each carrier can be easily associated to two power switches of the converter. LSPWM leads to less distorted line voltages since all the carriers are in phase compared to PSPWM [30]. In addition, since it is based on the output voltage levels of an inverter, this principle can be adapted to any multilevel converter topology. However, this method is not preferred for CHB and FC, since it causes an uneven power distribution among the different cells. This generates input current distortion in the CHB and capacitor unbalance in the FC compared to PSPWM [31-35]. Figure 6 shows the LS-PWM carrier arrangements.

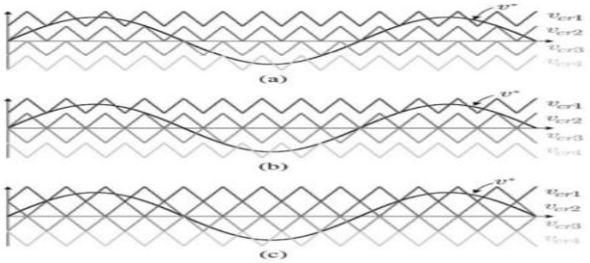


Figure 2: LS-PWM carrier arrangements: (a) PD, (b) POD, and (c) APOD.

### *Phase Shift Pulse Width Modulation*

PWM signals are pulse trains which are applied to the gate of switches to perform the operation of converter. The pulse trains are fixed frequency and magnitude and variable pulse width [36]. There is one beat of settled extent in each PWM period. In any case, the width of the beats changes from period to period as indicated by a regulating signal. At the point when a PWM flag is connected to the entryway of a power transistor, it causes the turn on and kills interims of the transistor to change starting with one PWM period then onto the next PWM period as indicated by the same regulating signal and thus working of converter begins. The recurrence of a PWM flag must be substantially higher than that of the regulating signal, the major recurrence, with the end goal that the vitality conveyed to the heap depends generally on the tweaking signal. The control of yield voltage is done utilizing beat width balance [37, 38].

This technique uses a set of carriers that are all phase-shifted. The four triangular carriers are phase-shifted by $90^{o}$. Using the same sampling period, it has four times larger switching frequency than that of other techniques. This technique is specially conceived for FC and CHB converters. Since each

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FC cell is a two-level converter, and each CHB cell is a three-level inverter, the traditional bipolar and unipolar PWM techniques can be used, respectively. Due to the modularity of these topologies, each cell can be modulated independently using the same reference signal [39].

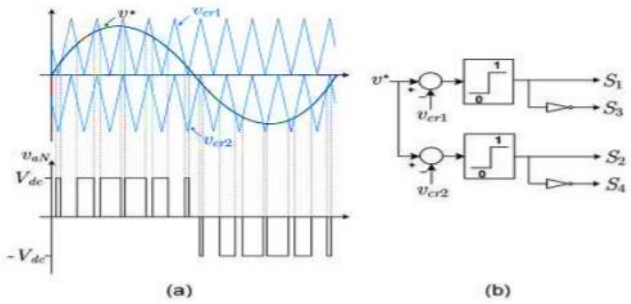


Figure 3: Phase Shift PWM

## IV. PV ARRAY

The photovoltaic cell converts the light energy into electrical energy depending on the irradiation of the sun and temperature in the atmosphere. Basically PVC is a PN junction diode [40-41]. But in PN junction diode DCI AC source is needed to work, but here light energy is used as a source to produce DC output. PVC is a current control source not a voltage control source. The equivalent electrical circuit diagram of PVC is shown in the Figure 4.

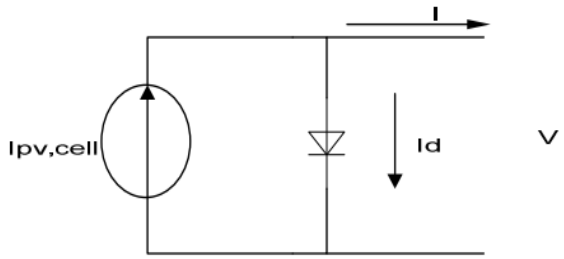


Figure 4: Show ideal photovoltaic cell equivalent circuit

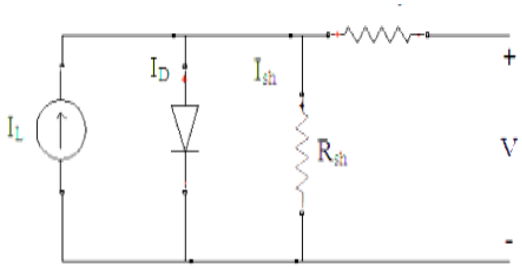


Figure 5: Equivalent Electrical Circuit of PVC

$$I_D = I_0[\exp(V + IR_S)/KT - 1] \quad (1)$$

Therefore PVC output current is given in equation 2.

$$I = I_L - I_D - I_{Sh} \quad (2)$$

$$I = I_L - I_0[\exp(q(V + IR_S))/KT - 1] - (V + IR_S)/R_{Sh} \quad (3)$$

Where $I_D$ the diode is current, $R_{sh}$ is the shunt resistance, $I_L$ is the light generated current of solar array. Solar cell is basically a p-n junction fabricated in a thin wafer or layer of semiconductor. The electromagnetic radiation of solar energy can be directly converted electricity through photovoltaic effect. Being exposed to the sunlight, photons with energy greater than the band-gap energy of the semiconductor are absorbed and create some electron-hole pairs proportional to the incident irradiation. Under the influence of the internal electric fields of the p-n junction, these carriers are swept apart and create a photocurrent which is directly proportional to solar insolation. PV system naturally exhibits a nonlinear I-V and P-V characteristics which vary with the radiant intensity and cell temperature [42].

**MPPT ALGORITHM:-** Because of the lesser efficiency of photovoltaic array most of the energy, impacting over array gets wasted. The algorithm known as maximum power point tracking may be helpful to enhance the performance of solar panel. The MPPT algorithm works on principal of Thevenin, according which the power output of a circuit is maximum when impedance of circuit matches with the load of impedance. So now we have to match the impedance instead of tracking maximum power point [43].

There are different techniques used to track the maximum power point. Few of the most popular techniques are:

- Perturb and observe (hill climbing method)
- Incremental Conductance method
- Fractional short circuit current
- Fractional open circuit voltage
- Neural networks
- Fuzzy logic

***Perturb and observe***

The P&O algorithm and “hill-climbing”, both names refer to the same algorithm depending on how it is implemented. The basic difference between these two is that Hill-climbing involves a deviation of the duty cycle of the power converter and in P&O anxiety on the operating voltage of the DC link between the PV array and the power converter takes place [44]. The deviation of duty cycle of the power converter is the modification of the voltage of DC link between the PV array and the power converter refer as Hill-climbing, so both names refer to the same technique. What should be the next perturbation is decided by considering the sign of the last perturbation and the sign of the last increment in the power.

The perturbation will remain in the same direction if power is incremented, and if power is decreased then next perturbation will be in the opposite direction. The process will be repeated until the point of maximum power will be reached. Then the operating point oscillates around the MPP.

***Incremental conductance***

The slope of the curve between power and voltage of PV module is the deciding factor in incremental conductance algorithm, if it is zero it shows point of MPP positive (negative) on the left of it and negative (positive) on the right.

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- $\Delta V/\Delta P = 0$ at the MPP
- $\Delta V/\Delta P > 0$ on the left
- $\Delta V/\Delta P < 0$ on the right

The change of MPP voltage is identified by comparing the change of the power to increment of the voltage of current curve.

***Fractional short circuit current***

Fractional short circuit current method states that the ratio between array voltage at maximum power $V_{MPP}$ to its open circuit voltage $V_{OC}$ is nearly constant.

$$V_{MPP} \approx k_1 V_{OC}$$

The constant $K_1$ is having value between 0.71 to 0.78. Now the value of $V_{MPP}$ can be calculate by periodically measuring $V_{OC}$. This method is simple and cheap to implement but its efficiency is relatively low due to the utilization of inaccurate values of the constant k1 in the computation of $V_{MMP}$ .

***Total Harmonic Distortion***

The total harmonic distortion (THD or THDi) is a measurement of the harmonic distortion present in a signal and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. Distortion factor, a closely related term, is sometimes used as a synonym.

In audio systems, lower distortion means the components in a loudspeaker, amplifier or microphone or other equipment produce a more accurate reproduction of an audio recording.

In radio communications, devices with lower THD tend to produce less unintentional interference with other electronic devices. Since harmonic distortion tends to widen the frequency spectrum of the output emissions from a device by adding signals at multiples of the input frequency, devices with high THD are less suitable in applications such as spectrum sharing and spectrum sensing.

In power systems, lower THD implies lower peak currents, less heating, lower electromagnetic emissions, and less core loss in motors.

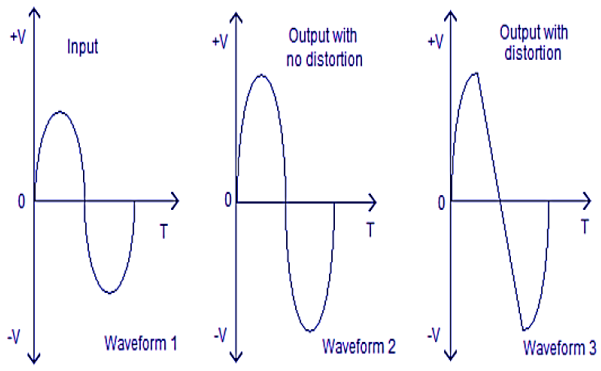


Figure 6: Output Waveform of Distortion

## V. CONCLUSION

The presented research work has been focused on the construction of variable amplitude sinusoidal voltage using the different topologies. The first effort has been related to the development of new MLI topology using diodes and switching devices under symmetric and asymmetric mode. The advantage of the topology articulates any desired voltage level with a reduced total number of devices and sources over basic and similar topology. The reduced stress of the sources achieved through pulse swapping among the cell switches, balances the load power and reduces the voltage stress of the devices.

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