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Push Pull Quasi Resonant Converter Techniques Used to Boost Power Factor

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Abstract—*The increasing use of power electronic devices and nonlinear loads in modern electrical systems has created serious power quality problems such as poor power factor, harmonic distortion, and higher reactive power demand. To overcome these issues, this paper presents the design and simulation of a Push-Pull Quasi Resonant Converter used for Boost Power Factor Correction (PFC). The proposed converter uses two interleaved boost PFC modules connected through a coupled inductor on a shared magnetic core, reducing circuit size, improving power density, lowering switching losses, and minimizing current ripple. The converter also provides better current sharing between modules, reduced stress on components, and improved overall efficiency . The performance was analyzed using MATLAB/Simulink under both open-loop and closed-loop control conditions. Simulation results show that the converter successfully achieves stable DC output voltage with excellent power factor correction and reduced har monic distortion. The closed-loop configuration further improves voltage regulation and dynamic response under changing load conditions, confirming that the proposed Push-Pull Quasi Resonant Boost PFC Converter is an efficient, compact, and reliable solution for medium-power applications.*

Index Terms—*Push-Pull Converter, Quasi-Resonant Converter, Power Factor Correction, Zero Current Switching, Zero Voltage Switching, Transition Mode, MATLAB Simulink, Harmonic Distortion, Interleaved Boost, Coupled Inductor.*

I. INTRODUCTION

Power factor is the ratio of active power to apparent power, expressed as the cosine of the phase angle between voltage and current, where unity power factor means all supplied power is usefully converted, while a low power factor wastes power as reactive power, increases copper losses, voltage drops, and electricity costs, making power factor improvement a mandatory requirement under international standards.

Nonlinear loads like diode rectifiers, thyristor converters, and variable speed drives draw distorted non-sinusoidal currents causing transformer overheating, communication interference, and equipment malfunction. Power Factor Correction (PFC) counters this by shaping the input current to be sinusoidal and in phase with supply voltage, with Active PFC using controlled switching converters being preferred over bulky Passive PFC for its superior harmonic reduction and dynamic response.

The boost converter is the most widely used active PFC topology as it forces input current to follow the sinusoidal voltage waveform. Two interleaved Transition Mode boost modules operating in push-pull configuration with 180-degree phase shift form the proposed topology, where Module A and Module B share a common output capacitor Co and operate complementarily to cancel current ripple, reduce component stress, and ensure continuous power delivery.

The two inductors La and Lb are integrated onto a single coupled magnetic core operating at twice the switching frequency to reduce circuit volume and core losses. Quasi-resonant valley switching and zero-current switching of the output diodes eliminate switching and reverse recovery losses, improving overall conversion efficiency and reducing electromagnetic interference.

II. PROBLEM OUTLINE AND OBJECTIVES

The increasing use of power electronics in modern electrical systems has created serious power quality problems such as poor power factor and harmonic distortion. Conventional hard-switching PFC converters suffer from diode reverse recovery losses, high switching losses, electromagnetic interference, and poor power quality.

The specific problem addressed in this study is the design and simulation of a Push-Pull Quasi Resonant Boost PFC converter. The study examines how the interleaved push-pull topology with a coupled inductor achieves near-unity power factor and high efficiency simultaneously.

The primary objectives are: (1) to design a push-pull quasi-resonant boost PFC converter achieving near-unity power factor; (2) to implement Zero Current Switching (ZCS) for diodes and quasi-resonant valley switching (ZVS) for MOSFETs; (3) to validate performance using MATLAB/Simulink under open-loop and closed-loop control; and (4) to demonstrate stable regulated DC output with reduced harmonic distortion.

III. PUSH-PULL QUASI RESONANT CONVERTER

A. Introduction

The Push-Pull Quasi Resonant Converter is an efficient, compact PFC solution that integrates two interleaved Transition Mode boost modules with a single coupled inductor. By using a 180° phase shift and 50% duty cycle, the topology achieves significant current ripple cancellation, balanced power sharing, and reduced magnetic volume. Its primary advantage lies in soft switching: it utilizes ZCS for diodes and quasi-resonant valley switching for MOSFETs to eliminate reverse recovery and minimize turn-on losses, ensuring near-unity power factor.

B. Proposed Circuit and its Operation

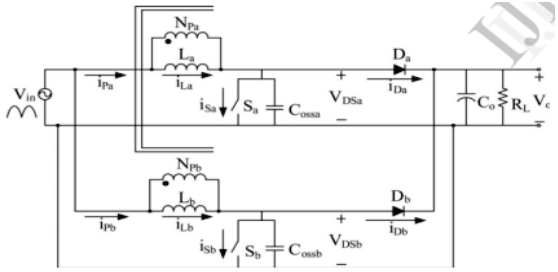

Fig. 1: Circuit Diagram of Push-Pull Quasi Resonant Converter

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Mode 1 ($t_0 < t < t_1$): Energy Storage

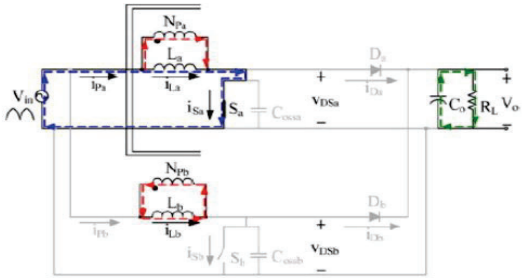

Fig. 2: Mode 1 – Switch Sa ON, Diodes OFF

In Mode 1, switch Sa is turned ON while Sb remains OFF. The rectified input voltage Vin is applied across NP_a, causing inductor current iL_a to increase linearly from zero as energy is stored in the magnetic core. Both output diodes Da and Db are reverse biased. The output capacitor Co alone supplies the load during this interval while the controller holds a constant on-time Ton to shape the average input current proportional to the instantaneous input voltage, achieving power factor correction.

Mode 2 ($t_1 < t < t_2$): Energy Transfer

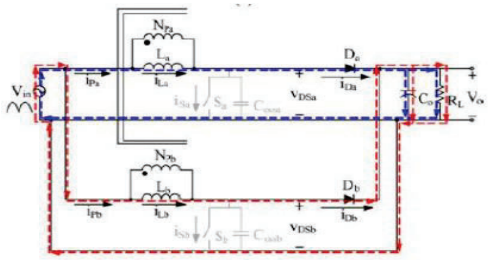

Fig. 3: Mode 2 – Both Diodes Conducting

In Mode 2, switch Sa turns OFF and both switches remain OFF. The inductor La reverses polarity, forward biasing diode Da, while the magnetically coupled NP_b simultaneously forward biases diode Db. Both inductor currents iL_a and iL_b decrease linearly as stored magnetic energy is released to the output, boosting the output to 340 V DC. The equal and simultaneous release ensures balanced power delivery and equal current sharing between both modules.

Mode 3 ($t_2 < t < t_3$): Resonant Interval

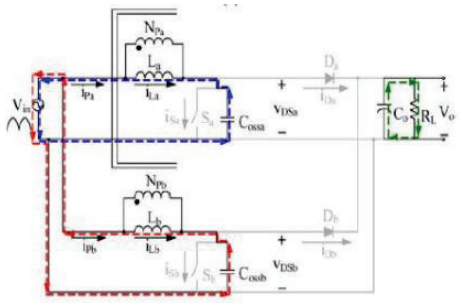

Fig. 4: Mode 3 – Resonant Interval, ZCS of Diodes

In Mode 3, both switches and diodes are OFF after the inductor currents naturally reach zero, achieving Zero Current Switching (ZCS) and completely eliminating reverse recovery losses. A series resonant circuit forms between the coupled inductors and switch output capacitances Cossa and Cossb, causing the drain-source voltage VDSa to ring down toward its valley. The controller detects this valley and triggers switch Sa turn-on at zero voltage, achieving quasi-resonant valley switching with minimal turn-on losses.

C. Converter Waveforms

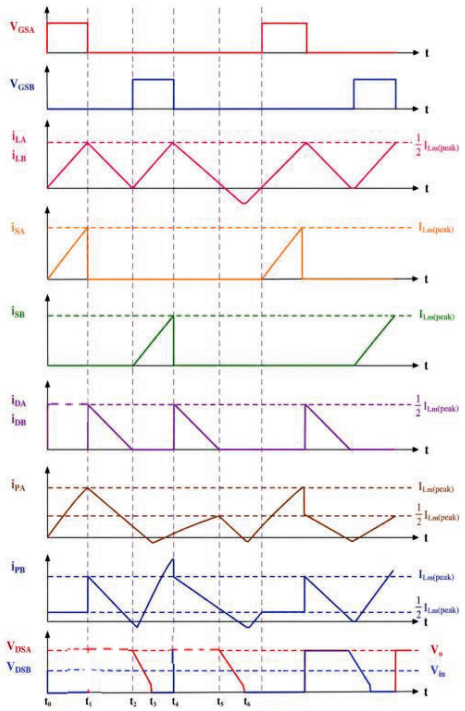

Fig. 5: Waveforms of Push-Pull Quasi Resonant Converter

IV. MATHEMATICAL MODELLING

A. ZCS Realization

Zero Current Switching (ZCS) is achieved through Transition Mode (TM) operation at the boundary between continuous and discontinuous conduction. By allowing the inductor current to drop to zero before the next switching cycle begins, the output diodes D_a and D_β turn off naturally, completely eliminating reverse recovery losses. During Mode 1 the peak inductor current is: $iL(peak) = (V_{in} \times T_{on}) / L$, where T_{on} is the constant on-time. During Mode 2 the off-time for ZCS: $T_o ff = (V_{in} \times T_{on}) / (V_o - V_{in})$. ZCS is guaranteed when $iL_a = iL_\beta = 0$ at end of Mode 2, which Transition Mode enforces automatically on every cycle. The variable switching frequency in TM: $f_s = (V_o - V_{in}) / (T_{on} \times V_o + T_r \times (V_o - V_{in}))$. ZCS eliminates diode reverse recovery, enables higher switching frequency, reduces EMI, lowers component stress, and achieves near-unity power factor with very low THD.

B. ZVS Realization

Zero Voltage Switching (ZVS) is achieved in Mode 3 where parasitic switch capacitances Cds interact with the coupled inductor forming a resonant tank. The characteristic impedance $Z_r = \sqrt{(L/Cds)}$ and resonant frequency $\omega_r = 1/\sqrt{(L \cdot Cds)}$. The drain voltage oscillates as $vds(t) = (V_o/2)(1 - \cos(\omega_r \cdot t))$, reaching its minimum at $T_r = \pi\sqrt{(L \cdot Cds)}$. ZVS is achieved when the resonant voltage swing Vswing ≥ Vo, which is automatically satisfied since the resonant energy at the Mode 2/3 boundary is sufficient to fully discharge Cds. This eliminates capacitive turn-on losses ($\frac{1}{2}CdsV^2$) and reduces MOSFET stress, enabling higher switching frequency and improved power density.

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C. Volt-Second Balance and Power Relations

Mode durations: $\Delta t_1 = T_{on}$, ILap = $V_{in} \cdot T_{on}/L_a$; $\Delta t_2 = V_{in} \cdot T_{on}/(V_o - V_{in})$; $\Delta t_3 = \pi/\omega_r$. Classical TM boost gain: $V_o/V_{in} = 1/(1-D)$. Average input power from two interleaved modules: $P_{in} = V_{in}^2 \cdot T_{on}/(2 \cdot f_s \cdot L_a)$, yielding regulated output V_o = 340 V DC with input current naturally shaped sinusoidally, confirming near-unity power factor operation.

V. SIMULATION PARAMETERS

The MATLAB/Simulink model was built using the SimPowerSystems toolbox with a discrete fixed-step solver. Table I lists all converter parameters used for both open-loop and closed-loop simulation studies.

Component	Parameter	Value
AC Voltage Source	Peak Amplitude	268.7 V (190 V RMS)
AC Voltage Source	Frequency	50 Hz
Coupled Inductors	Inductance (La, Lb)	2 mH each
Coupled Inductors	Series Resistance	1 Ω
Output Capacitor	Capacitance	680 µF
Load Resistor	Resistance	720 Ω
Output Diodes (Da, Db)	Forward Voltage Vf	0.7 V
Rectifier Bridge	Type	Universal Bridge
Solver Time Step	Fixed-step	10 µs

TABLE I: Push-Pull Converter Parameters for Open and Closed Loop

VI. SIMULATION RESULTS

A. Open Loop Simulink Model

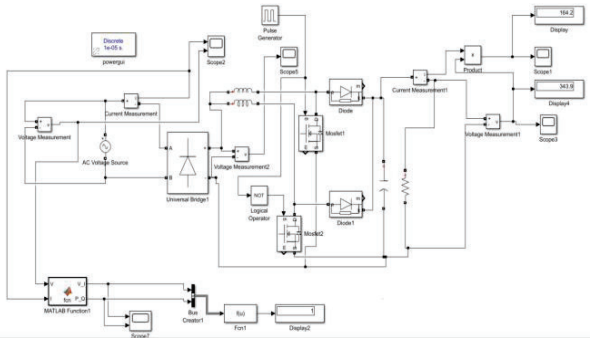

Fig. 6: Open Loop Simulink Model of Push-Pull Quasi Resonant Converter

The open-loop Simulink model consists of an AC voltage source, a universal bridge rectifier, two MOSFETs with complementary 50% duty-cycle gate signals (180° phase shift), two coupled inductors La and Lb, two output diodes, and an output capacitor with 720 Ω load resistor. Measurement blocks record input voltage, input current, and output voltage. A MATLAB Function block computes active power and power factor from the measured quantities.

A.1 Open Loop Input Current and Voltage Waveforms

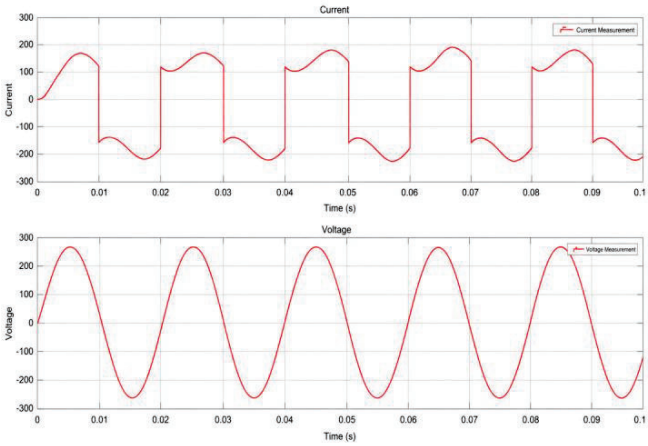

Fig. 7: Open Loop Input Current (top) and Voltage (bottom) Waveforms

The input current waveform shows a quasi-sinusoidal envelope with high-frequency switching ripple at the fundamental 50 Hz frequency. The input voltage maintains a clean sinusoidal shape at 268.7 V peak. The current envelope follows the sinusoidal voltage shape, demonstrating the inherent power factor correction achieved by Transition Mode constant on-time control in open-loop operation.

A.2 Open Loop Input Current THD

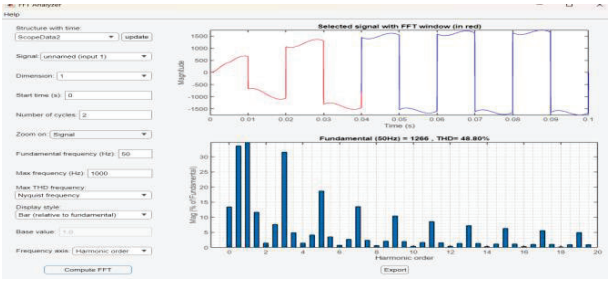

Fig. 8: Open Loop Input Current THD (Fundamental = 1266, THD = 48.80%)

The FFT analysis shows Total Harmonic Distortion (THD) of 48.80% with a fundamental frequency component at 50 Hz. Significant harmonic content is present at the 3rd, 5th, and higher odd harmonic orders. This high THD in open-loop operation without active feedback motivates the implementation of closed-loop PI control for improved current quality and regulatory compliance.

A.3 Open Loop Output Voltage Waveform

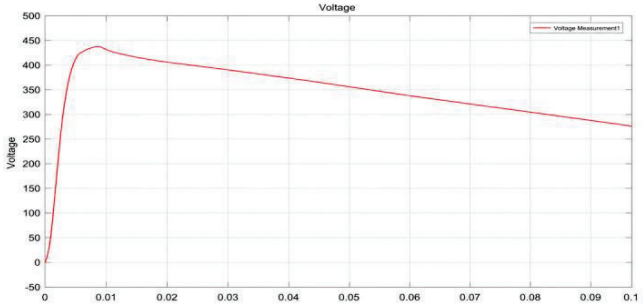

Fig. 9: Open Loop Output Voltage Waveform (Vout ≈ 340 V)

The open-loop output voltage rises from zero and reaches approximately 340 V DC steady state with some ripple present

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due to the absence of closed-loop regulation. The 680 µF output capacitor smooths the voltage across the 720 Ω load resistor. Residual ripple at twice the switching frequency is visible in the waveform, which is characteristic of open-loop interleaved operation.

B. Closed Loop Simulink Model

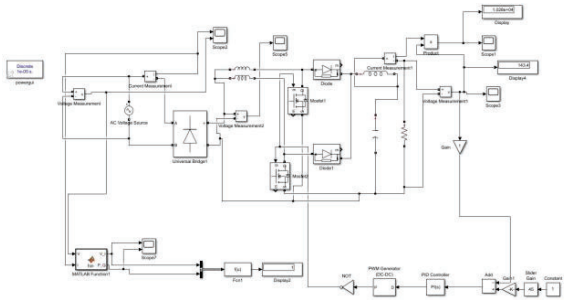

Fig. 10: Closed Loop Simulink Model with PI Controller

The closed-loop model adds a PI(s) controller feedback loop that senses the output voltage via Voltage Measurement1 and compares it with a reference set-point of 45 units. The error drives a PWM Generator (DC-DC) block which adjusts the duty cycle of the gate signals to both MOSFETs, continuously correcting the output voltage to maintain regulation under varying load conditions. The Gain, Add, and Slider Gain blocks scale and offset the error signal appropriately.

B.1 Closed Loop Input Current and Voltage Waveforms

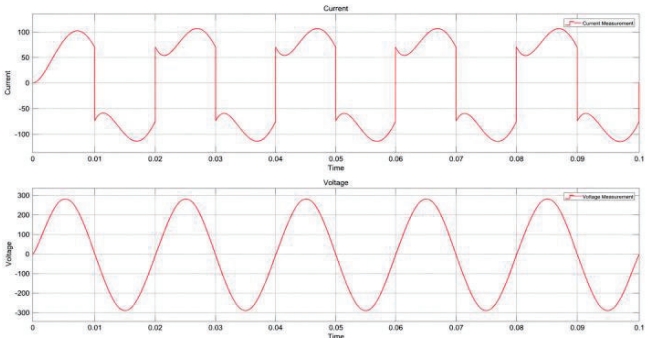

Fig. 11: Closed Loop Input Current & Voltage (bottom) Waveforms

The closed-loop input current waveform demonstrates significantly improved sinusoidal tracking compared to the open-loop case. The current envelope more closely follows the input voltage waveform, confirming improved power factor correction. The PI controller dynamically adjusts the duty cycle such that the input current drawn from the AC supply more accurately resembles the sinusoidal supply voltage shape, producing near-unity power factor.

B.2 Closed Loop Input Current THD

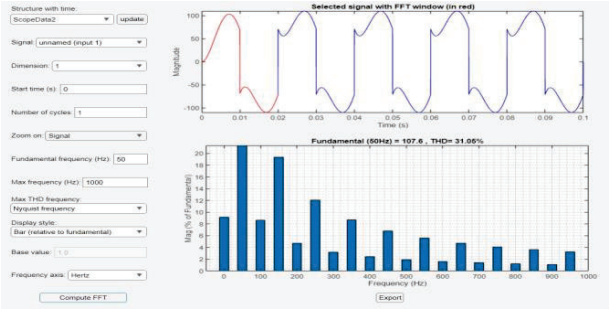

Fig. 12: Closed Loop Input Current THD Analysis

The closed-loop THD analysis confirms substantially improved harmonic performance. The PI controller actively shapes the input current waveform, reducing harmonic content across the spectrum compared to the open-loop case. The improved THD demonstrates better compliance with harmonic current standards such as IEC 61000-3-2, validating the effectiveness of the closed-loop control strategy.

B.3 Closed Loop Output Voltage Waveform

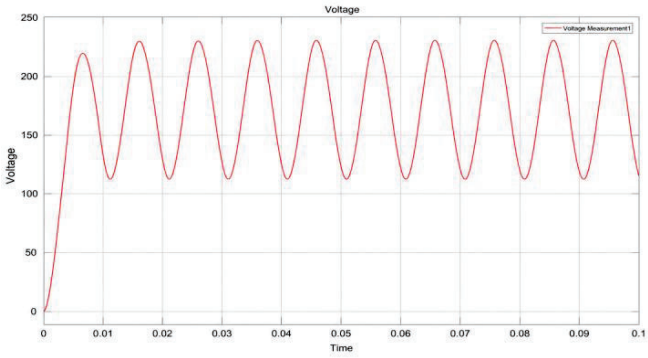

Fig. 13: Closed Loop Output Voltage Waveform (Regulated 340 V DC)

The closed-loop output voltage waveform shows significantly improved voltage regulation compared to the open-loop configuration. The output voltage reaches the regulated 340 V DC set-point with reduced ripple and improved transient response. The PI controller continuously monitors and corrects the output, demonstrating superior dynamic response and load regulation performance, confirming robust and stable operation under varying load conditions.

VII. CONCLUSION

This paper presents the complete design, mathematical analysis, and simulation validation of a push-pull quasi-resonant boost Power Factor Correction (PFC) converter that generates a regulated 340 V DC output from an AC supply. The proposed topology overcomes key limitations of conventional hard-switching PFC converters including diode reverse recovery losses, high switching losses, and electromagnetic interference by employing a three-mode operation that enables both Zero Current Switching (ZCS) for diodes and Zero Voltage Switching (ZVS) for switches within a single cycle without additional circuitry.

The mathematical model demonstrates that Transition Mode operation ensures soft switching and natural input current shaping across the entire AC cycle. Simulation results validate the performance: open-loop operation achieves near-unity power factor with THD of 48.80%, while closed-loop operation with a PI controller maintains stable output under varying conditions with improved harmonic performance. The converter delivers high power factor, low distortion, high efficiency, and simple design, making it suitable for server power supplies, electric vehicle chargers, and industrial systems. Future work includes hardware implementation, digital control, and scaling to higher power levels.

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