Proposed Memristor-based Loop Passive Filter for Phase Locked Loop

Naheem Olakunle Adesina Electrical Engineering and Computer Science Louisiana State University Baton Rouge, USA Ashok Srivastava
Electrical Engineering and Computer Science
Louisiana State University
Baton Rouge, USA

Abstract - This paper highlights a way to introduce memristive device into loop filter circuits for phase locked loop (PLL) applications. The fundamental behaviors of memristor are carefully examined. In light of this, we proposed two commonest topologies of memristor-based passive loop filter (LP) for PLL applications. The transfer functions of the LPs are obtained, and the amplitude-frequency response, phase-frequency response, and noise-frequency response are presented. Finally, Simulation results demonstrate our analyses, and the memristive elements can be extended to other types of loop filters such as active filter, digital loop filter and sequential filter.

Keywords:- Memristor, Loop Filter, Phase Locked Loop, Voltage Controlled Oscillator, Complementary Metal-Oxide Semiconductor (CMOS), Hysteresis Curve, Frequency Response

I. INTRODUCTION - MEMRISTOR

The advent of HP labs' TiO_2 memristor has resulted in a large number of proposed memristor-based models and implementation in recent years [1-3]. Memristor is regarded as a fourth fundamental passive element whose resistance changes with the magnitude and direction of excitation or input signal (voltage or current). Basically, a memristor has two states - R_{ON} and R_{OFF} . We define these states as the weight of memristor which is given in (1).

State variable,
$$x(t) = \frac{W(t)}{D} \epsilon(0,1)$$
 (1)

Where W(t) and D are the widths of doped region and total region respectively as shown in Fig. 1.

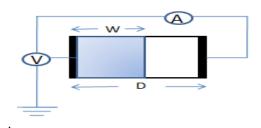


Fig. 1. HP memristor structure

In this paper, we adopt HP TiO_2 memristor model in our design and simulations. Although memristor was introduced by Leon Chua in 1971 [4], it was not developed until 2008 when a team at HP lab, led by Stanley Williams, manufactured the first memristor. The memristor was fabricated by sandwiching TiO_2 (undoped region) and TiO_{2-x} (doped region) between platinum contacts. The doped

region has high carrier or ion concentrations which makes it a low resistance region, R_{ON} , and vice versa for the undoped region, R_{OFF} [5,6].

When an electric current passes through the structure shown in Fig. 2, the boundary between the doped and undoped moves in the same direction, thus, the total resistance R_{mem} of memristor is obtained from the series connection of both doped and undoped regions [5].

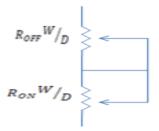


Fig. 2. Equivalent circuit of HP memristor

$$R_{mem}(x(t)) = R_{ON}x(t) + R_{OFF}(1 - x(t))$$
 (2)

It could be inferred from (2) that whenever x(t) increases, R_{mem} decreases and vice versa. The two possible extreme cases are w(t) = 0 and w(t) = D; x(t) = 0 and 1 respectively. Invariably, R_{mem} is clipped to R_{OFF} and R_{ON} respectively, until the applied voltage or current changes its direction.

II. MEMRISTOR-BASED LOOP FILTER

The loop filter (LF) in Phase Locked Loop (PLL) is a low-pass filter, which is used to remove the high frequency components from phase detector/charge pump (PD/CP) [7]. LF is an essential block in PLL because it filters out the ripple in the Voltage Controlled Oscillator (VCO) control voltage and ensures a dc-controlled signal to the VCO. Loop filter does not only filter high frequency components but also control the dynamic characteristics capture, lock range, bandwidth and transient response in PLL. Studies have shown that there are majorly four different topologies of loop filter; passive filter, active filter, digital filter, and sequential filter [8]. In this work, we only examined the two commonest passive loop filter topologies in phase locked loop [7, 9-12].

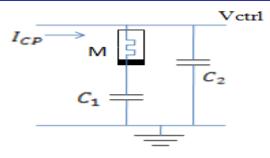


Fig. 3. Proposed type II loop filter

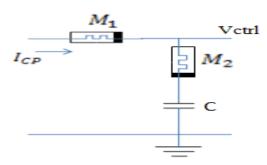


Fig. 4. Proposed type I loop filter

For our proposed second order loop filter, it is worth mentioning that we replaced the resistors with memristors, M, M_1 , and M_2 as shown in Fig. 3 and 4. M, memristance, is the inherent property of a charge-controlled memristor. It is similar to resistance and also has the same unit, Ohm (Ω) .

III. ANALYSIS OF MEMRISTOR-BASED LOOP FILTER

In order to understand the behaviour characteristics of these filters, it is necessary to identify their transfer functions.

The transfer function of loop filter in Fig. 3 has a unit of impedance (Ω) , being the output generated from CP output current [13]. The impedance of the loop filter is denoted as as Z(s).

$$Z(s) = \frac{V_{CTRL}}{I_{CP}} = H(s) = \frac{1 + sT_1}{sT_2(1 + sT_3)}$$
(3)

Where:

$$T_1 = MC_1 \tag{4}$$

$$T_2 = C_1 + C_2 \tag{5}$$

$$T_3 = M \frac{c_1 c_2}{c_1 + c_2} \tag{6}$$

Similarly for Fig. 4, which is a type I second order filter, the transfer function is given in (7).

$$H(s) = \frac{1 + {}^{s}/{}_{W_{z}}}{1 + {}^{s}/{}_{W_{p}}} \tag{7}$$

$$W_z = \frac{1}{M_2 C}$$
 and $W_p = \frac{1}{(M_1 + M_2)C}$ (8)

Equation 8 shows that zero frequency is usually greater than the pole frequency.

IV. SIMULATION RESULTS AND DISCUSSIONS

Fig. 5 – 7 show the simulation results of memristor with a sinusoidal input, V_{source} = Asinwt, where A = 1.2 V, f_1 = 1 Hz, f_2 = 2 Hz, f_3 = 4 Hz and f_4 = 8 Hz. The HP memristor model parameter used are [14,15]: R_{init} = 11 $k\Omega$, R_{ON} = 100 Ω , R_{OFF} = 16 $k\Omega$, D = 10 nm, μ_v = 10 F m^2/sV and P = 10, where R_{init} and P parameters denote the initial resistance and exponent of window function respectively.

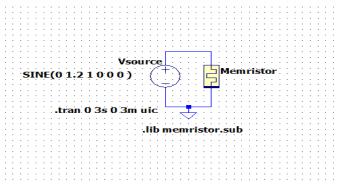


Fig. 5. SPICE simulation circuit of memristor model

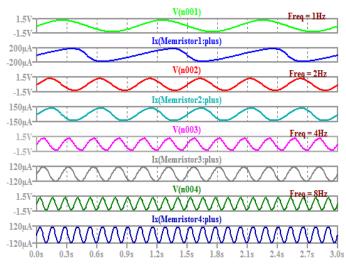


Fig. 6. Voltage and current of memristor at varying frequency

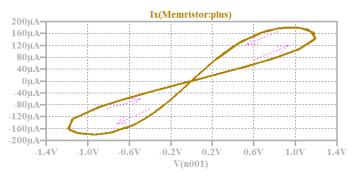


Fig. 7. The pinched hysteresis loop of memristor

ISSN: 2278-0181

Fig. 5 shows that the phase difference between voltage and current reduces as frequency increases. This validates that a memristor behaves similar to a resistor at high frequency.

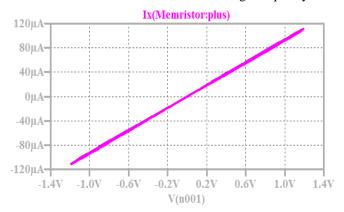


Fig. 8. Linear I-V characteristics of memristor at high frequency

The I-V characteristics of memristor is an pinched hysteresis loop as shown in Fig. 6. The curve collapses as frequency of input excitation increases. This gives the I-V characteristics in Fig. 7. The current linearly varies with voltage.

The frequency responses of our proposed filters are shown in Fig. 9 and 11. From Fig. 9, we obtained a cut-off frequency of 158 Krad/s for the proposed analog loop filter which makes it suitable for high frequency applications such as PLL.

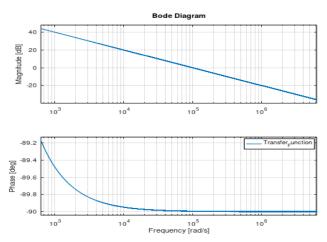


Fig. 9. Frequency response of proposed type II filter

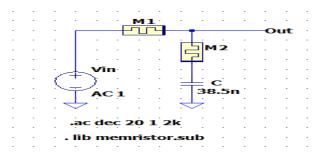


Fig. 10. SPICE simulation of proposed type I filter

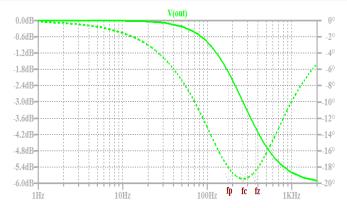


Fig. 11. Frequency response of proposed type II filter

Similarly, Fig. 11 shows the frequency response of our proposed filters. To ensure stable tracking in phase locked loop, we have proposed filter that has equal number of poles and zeros.

It is quite important to analyse the noise-rejection ability of our proposed loop filter. LF should be able to filter noise to ensure stable controlled input voltage to VCO. SPICE simulation of noise analyses are shown in Fig. 12 and 13. The result shows that our proposed filters do not only remove high frequency component from PD/CP output, but also filter noise interference, thus improving signal-to-noise ratio (SNR).

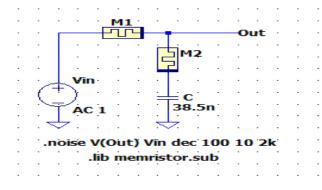


Fig. 12. SPICE simulation of noise analysis of proposed filter

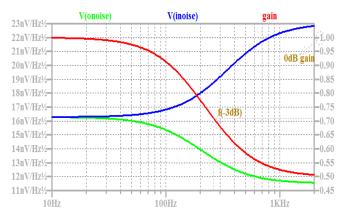


Fig. 13. Noise simulation results

ISSN: 2278-0181 Vol. 8 Issue 04, April-2019

From Fig. 13, it is clearly shown that: $V_{onoise} = Gain * V_{inoise}$ (9)

V. CONCLUSION AND FUTURE WORK

This work started with understanding the behavior of memristor to sinusoidal voltage excitation at varying frequencies. Following this, we examined the two commonest low pass filter topologies that have been used in phase locked loop. We obtained their transfer functions and plotted their Bode plots with Octave and SPICE respectively. In our analyses, we showed that the frequency responses of our proposed filter are consistent with the existing resitancebased loop filter. However, our proposed memristor-based loop filters are not only CMOS compatible (crossbar architecture), but also consume less power and reduced area on the chip without compromising functionalities of filters. Aside the fact that memristor is a suitable choice for nanoelectronic systems and applications, the advent of soluble memristor provides environmentally friendly electronic devices, most especially it prevents valuable information from falling into the hands of enemy. In addition, memristor offers a large resistance value to keep PLL stable, and occupies small area on the chip.

The proposed memristor-based loop filter, together with memristive emulator and MOSCAP, can be designed using EDA tools in current CMOS technology and simulated.

REFERENCES

- S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," Nano Lett., vol. 10, no. 4, pp. 1297–1301, 2010.
- [2] Z. Q. Wang, H. Y. Xu, X. H. Li, H. Yu, Y. C. Liu, and X. J. Zhu, "Synaptic learning and memory functions achieved using oxygen ion migration/diffusion in an amorphous InGaZnO memristor," Adv. Func. Mat., vol. 22, no. 13, pp. 2759–2765, 2012.
- [3] T. Prodromakis, B. P. Peh, C. Papavassiliou, and C. Toumazou, "A versatile memristor model with nonlinear dopant kinetics," IEEE Trans. Electron Devices, vol. 58, no. 9, pp. 3099–3105, 2011.
- [4] L. O. Chua, "Memristor the missing circuit element," IEEE Transactions on Circuit Theory, vol. 18, no. 5, pp. 507-519, 1971.
- [5] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," Nature, vol. 453, pp. 80-83, 2008.
- [6] R. Williams, "How We Found The Missing Memristor," IEEE Spectrum, vol. 45, no. 12, pp. 28-35, 2008.
 [7] Guan-Chyun Hsieh and James C. Hung, "Phase-Locked Loop
- [7] Guan-Chyun Hsieh and James C. Hung, "Phase-Locked Loop Techniques – A Survey," IEEE Transactions on Industrial Electronics, vol. 45, no. 6, pp. 609-615, 1996.
- [8] R. Dinesh and Ramalatha Marimuthu, "A Survey on ADPLL Components and their effects upon Power, Frequency and Resolution," International Journal of Applied Engineering Research, vol. 11, no. 3, pp. 1569-1574, 2016.
- [9] Joonsuk Lee and Beomsup Kim, "A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control," IEEE Journal of Solid-State Circuits, vol. 35, no. 8, 2000.
- [10] Sudhakar Pamarti, Lars Jansson, and Ian Galton, "A Wideband 2.4-GHz Delta-Sigma Fractional-N PLL With 1-Mb/s In-Loop Modulation," IEEE Journal of Solid-State Circuits, vol. 39, no. 1, 2004.
- [11] S. Mirabbasi and K. Martin, "Design of loop filter in phase-locked loop," Electronic Letters, vol. 35, no. 21, pp. 1801-1802, 1999.
- [12] D. M. Fischette, L. S. Loke, R.J. DeSantis, and G. R. Talbot, "An Embedded All-Digital Circuit to Measure PLL Response," IEEE Journal of Solid-State Circuits, vol. 45, no. 8, pp. 1492-1503, 2010.
- [13] Barale, F. (2008), Frequency Dividers design for multi-GHz PLL systems, M.S. Thesis, Georgia Institute of Technology, Atlanta, USA.
- [14] L. O. Chua and S. M. Kang, "Memristive devices and systems," Proc. IEEE, vol. 64, no. 2, pp. 209-223, 1976.
- [15] Massmilliano Di Ventra, Yurry V. Pershin, and Leon O. Chua, "Circuit Elements With Memory: Memristors, Memcapacitors, and Memductors," Proc. IEEE, vol. 97, no. 10, pp. 1-6, 2009.