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Programmable Time to Digital Converter for Nuclear Timing Spectroscopy System

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***Abstract*—The paper describes a new method of time interval measurement using digital technique. Incoming time interval T1 between START and STOP pulse is converted to equivalent voltage V1 using the ramp generator and further elongated into time period T2 using the ramp of opposite polarity. Time period T2 is made sufficiently long so that it can be counted using crystal controlled oscillator and a counter. TDC offers time interval measurement range upto 3276.8 µs. Improved resolution of 25 ns has been obtained using clock frequency of 20 MHz. Designed TDC is programmable, hence range of time interval measurement can be changed by selecting proper ramp slope. TDC makes use of 16 bit dual, parallel, multiplying DACs to generate precise currents which decide ramp slopes. Temperature drift and reference voltage drift is self compensated.**

Keywords— Time To Digital Converter, Nuclear Timing Spectroscopy System, Time Interval Measurement Introduction

I. INTRODUCTION

Time interval (TI) between two physical events needs to be measured in nuclear timing spectroscopy system. These physical events could be gamma rays reaching the detectors. Conventional nuclear timing spectroscopy system is discussed in [1]. Detectors produce linear analog pulse corresponding to the interaction of gamma rays in the detectors. This linear pulse is converted into logical pulse by Time pick-off circuits. These pulses are given as START and STOP pulses to Time to Digital Converter (TDC). TDC produces digital code output corresponding to the time interval between START and STOP pulses. To measure this TI between START and STOP pulses, various methods have been explored [3], [4], [5] and have been summarized [2].

A new method for TI measurement using digital technique is proposed in this research paper.

II. NEW SYSTEM

TI can be measured using digital method i.e. using Positive and Negative slope generator, as shown in **Fig. 1**. At the arrival of START pulse, positive slope generator starts building ramp at the output using Reference Input 1 (negative voltage V-). During time interval T1, ramp increases in positive direction. Ramp slope and voltage magnitude is decided by the designed components of positive slope generator.

When STOP pulse is received, Reference Input 2 (positive voltage V+, having opposite polarity w.r.t. Reference Input 1) is connected to negative slope generator. Ramp starts decreasing in the negative direction during time interval T2. When ramp crosses zero reference voltage (ground line), it is detected by Comparator. Time interval T2 (when ramp is decreasing) is digitally counted by counter. So higher the input time difference between START and STOP pulse, ramp increases in positive direction to large magnitude of voltage, hence time required for negative ramp to reach zero voltage reference is more and so the digital counter output increases in proportion to this time interval.

Depending upon the range of the time interval measurement the positive slope generator circuit will generate calibrated slopes and accordingly negative slope generator circuit will also generate corresponding calibrated negative slopes. These slopes will be decided depending upon the range and resolution required for TDC. Programmable TDC is used to change the slope of the ramp.

III. DESIGN OF THE SYSTEM

System is designed and implemented as shown in **Fig. 2**. Digital-to-Analog Converter (DAC) is used to generate precise current by selecting appropriate digital code at its input. It is 16-Bit, dual, parallel input, multiplying DAC. DAC reference voltages are provided using voltage reference source. Further DAC output current I1, I2 is connected to the input terminals of integrator using analog switch. During time interval T1 (as shown in **Fig. 1**), current I1 flows through the input terminals of integrator, providing positive going ramp output. This ramp is connected to two comparators, comparator 1 and comparator 2. Comparator 2 threshold voltage is sourced using voltage divider. STOP pulse can be generated at various time instances by varying threshold voltage of comparator 2. When STOP pulse is generated, DAC current I2 gets connected to integrator and current I1 is disconnected using analog switch. So integrator starts developing negative ramp at the output.

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STOP pulse is connected to LATCH which generates QOUT. QOUT is connected to LOGIC CIRCUIT which enables clock pulses to the counters during time period T2. Clock period of 50 ns is obtained using Crystal controlled oscillator of 20 MHz frequency. Time interval T2 is counted by counters and digital code of counters is retrieved using arduino DUE microcontroller and stored in Computer for further analysis. Comparator 1 is provided with threshold

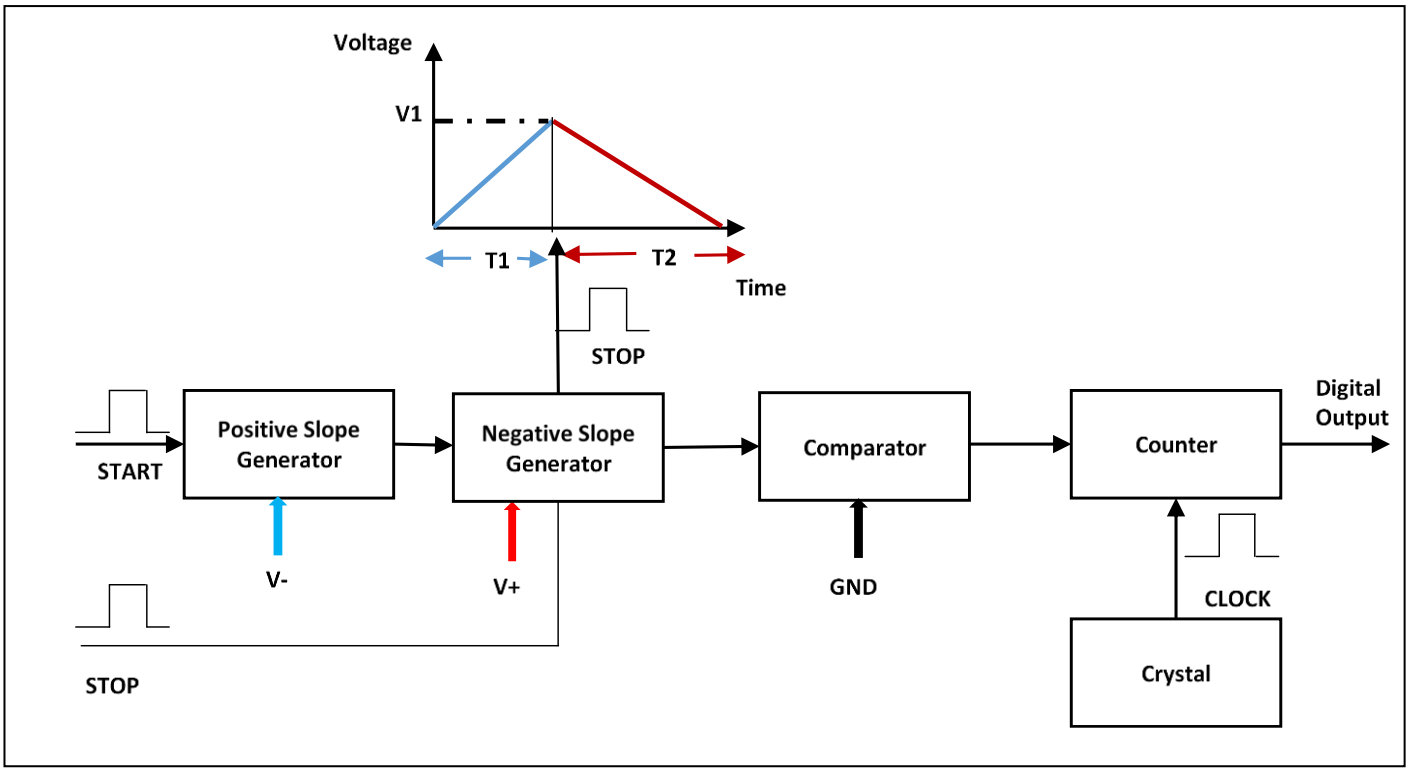

Fig. 1 Time Interval Measurement using TDC

voltage of GND. So when negative going ramp crosses GND threshold, comparator 1 output goes high, which resets the LATCH output QOUT. At this time instant, clock is disabled from the counter ICs using LOGIC CIRCUIT.

Time interval T2 is proportional to the amplitude of the ramp reached during time interval T1. Hence counter output for the period of T2 is proportional to the ramp voltage reached in T1 period and therefore proportional to the time period T1 between START and STOP pulse.

DAC IC internally has two DACs, both DACs are given same digital code, but reference voltage is varied. DAC 1 is provided with -12 V (negative reference voltage) and DA2 is provided with 4.096 V (positive reference voltage). Slope of the ramp is almost double for time period T1 compared to T2. T1 time interval is elongated to time period T2 and then counted by counter. This feature enables to improve resolution of the TDC by elongation/stretching factor K (where K = T2 / T1).

$$T2 = K * T1 = n * To$$

where 'To' is clock time period and 'n' is decimal equivalent of binary count of the counter

$$T1 = \frac{n * To}{K}$$

Resolution of TDC is improved by stretching factor K. As K increases, time period T2 elongates and large no of counter ICs are required to count time period T2. Hence, selected value of K is optimum combination of range and resolution. Clock period is n=50ns, with K=12/4.096=2.92 and resolution offered by TDC=50ns/2.92=25ns approximately. TDC offers improved resolution compared to conventional counter method. Four 4 bit counter ICs are used, so the range of TDC is (2^ 16)*50 ns=3276.8µs. Longer duration of time period T2 increase the conversion time of TDC.

The digital input code to DAC can be controlled through the computer for controlling the values of charging current which in turn will control the slope of the ramp resulting into different ranges of time interval measurement.

A. Temperature Drift in the System

System makes use of DAC to generate precise currents I1 and I2. Integrator develops positive ramp corresponding to current I1 and negative going ramp for current I2, refer **Fig. 1**. Temperature may cause some drift in the current I1 (current I1 reduces as electronic component resistor value R increases

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with temperature), which changes ramp slope and hence the final voltage reached by positive going ramp in time period T1. However temperature changes will induce the similar effect in I2, (reducing value of current I2), which will alter the slope of negative going ramp also. Time period T2 will be elongated accordingly and hence the counter count will remain the same, even though the ramp voltage in time interval T1 is reduced because of temperature effect. This is how temperature effects in current I1 will be balanced by current I2. Temperature drift effect on currents I1, I2 is explained mathematically as following

Positive slope generator develops ramp which reaches to voltage V1 in time interval T1 and it can be expressed as

$$V1 = \frac{1}{C}\int_0^{t1} i1(t)\,dt \quad (1)$$

$$V1 = \frac{T1 \times I1}{C} \quad (1)$$

Negative slope generator develops negative going ramp, which starts at positive voltage V1 and reaches to ground level in time interval T2 and it can be expressed as

$$-V1 = \frac{1}{C}\int_0^{t2} -i2(t)\,dt \quad (3)$$

$$-V1 = -\frac{T2 \times I2}{C} \quad (4)$$

Equating (3) and (4),

$$V1 = \frac{T1 \times I1}{C} = \frac{T2 \times I2}{C} \quad (5)$$

Above equation can be simplified as

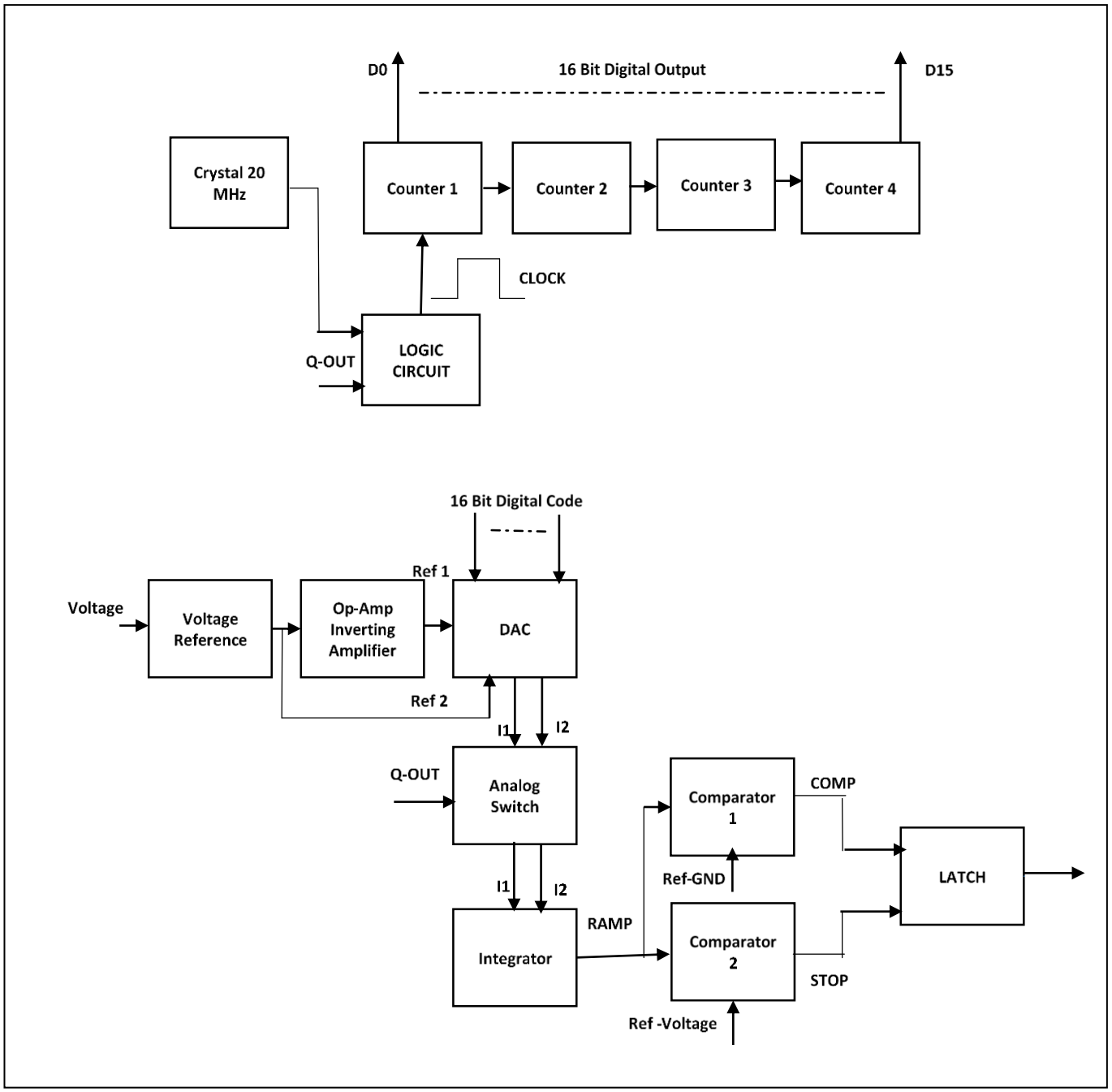

Fig. 2 Design of TDC

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Equating (3) and (4),

$$V1 = \frac{T1 \times I1}{C} = \frac{T2 \times I2}{C} \qquad (5)$$

Above equation can be simplified as

$$\frac{T1}{T2} = \frac{I2}{I1} \qquad (6)$$

If temperature varies, current I1 changes, but current I2 changes in proportion of I1 because both the currents are obtained using dual DAC which has two DACs fabricated in the same IC package. Hence ratio of T1 and T2 is maintained and temperature effects are compensated.

Further I1 and I2 can be written as

$$I1 = \frac{V_{ref}}{R_{eq}}\frac{D1}{(2^n)} \qquad (7)$$

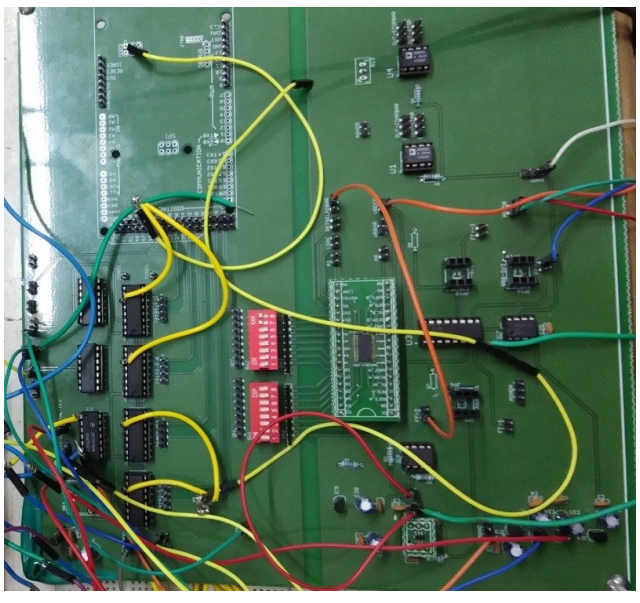

Fig. 4 PCB of TDC

$$I2 = \frac{V_{ref}}{R_{eq}}\frac{D2}{(2^n)} \qquad (8)$$

Where D1, D2 are decimal equivalent of binary code input to DAC1 and DAC2. Vref is reference voltage sourced to DACs and Req is the equivalent resistance internal to DAC.

Using (7) and (8), equation (6) is modified to

$$\frac{T1}{T2} = \frac{I2}{I1} = \frac{D2}{D1} \qquad (9)$$

Above equation (9), shows that the ratios of currents and hence time intervals are maintained constant, as D1 and D2 are kept constant.

Reference voltage to DAC is generated using the same voltage reference source, hence drift if any will be self compensated by DAC currents I1 and I2.

IV. PERFORMANCE OF THE SYSTEM

Performance of the designed system, refer **Fig. 4**., is measured using 6.4 µsec clock initially.

Time interval T1 of 225 µs is generated using integrator system, as shown in **Fig. 3**. STOP pulse of comparator 2 is generated after 225 µs using appropriate threshold voltage.T1

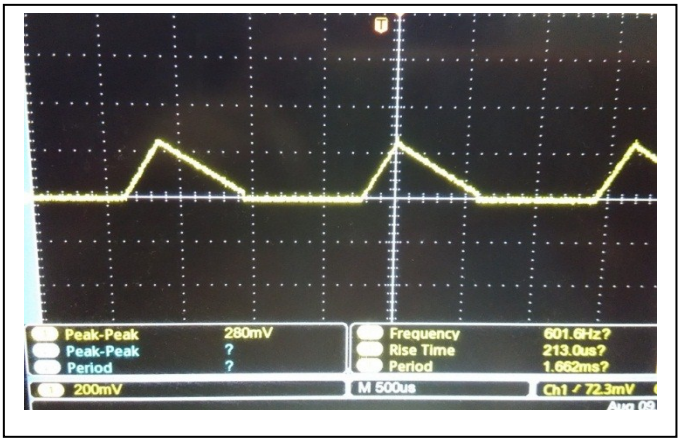

Fig. 3 Time Interval T1 of 225 µs

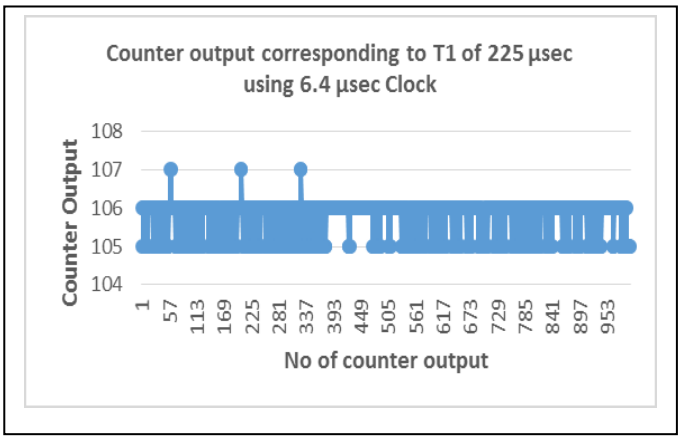

Fig. 5 Counter 1000 readings for time interval T1 of 225 µs

period is elongated to approximately 600 µs time period T2. T2 is counter by counter. Counter output is received using arduino DUE micro-controller. Counter output for 1000 readings is obtained, refer **Fig. 5** and average is computed. Average count of 106 is observed corresponding to T2.

International Journal of Engineering Research & Technology (IJERT)
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Refer **Fig. 6**, time interval T1 of 60 µs is generated using integrator system. STOP pulse of comparator 2 is generated after 60 µs using appropriate threshold voltage.T1 period is elongated to approximately 120 µs T2 period. T2 is counter by counter. Counter output is received using arduino DUE micro-controller. Counter output for 1000 readings is obtained, refer **Fig. 7** and average is computed. Average count of 22 is observed corresponding to T2.

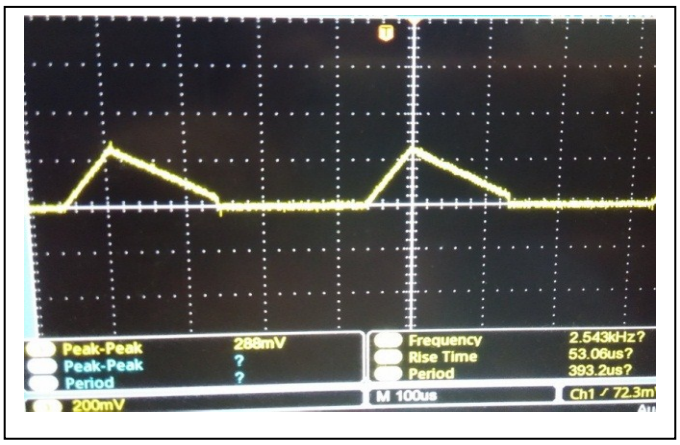

Fig. 6 Time Interval T1 of 60 µs

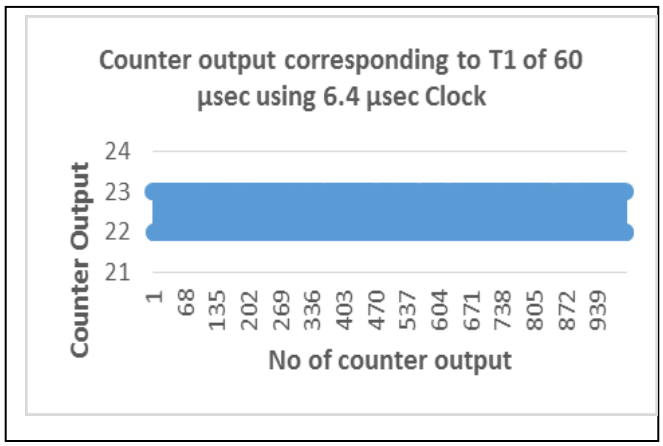

Fig. 7 Counter 1000 readings for time interval T1 of 60 µs

Further the TDC system is tested with 50 ns clock input for time period T2 of 180 µs and 80 µs. Counter output for 1000 readings is obtained, as shown in **Fig. 8**, **Fig. 9**.

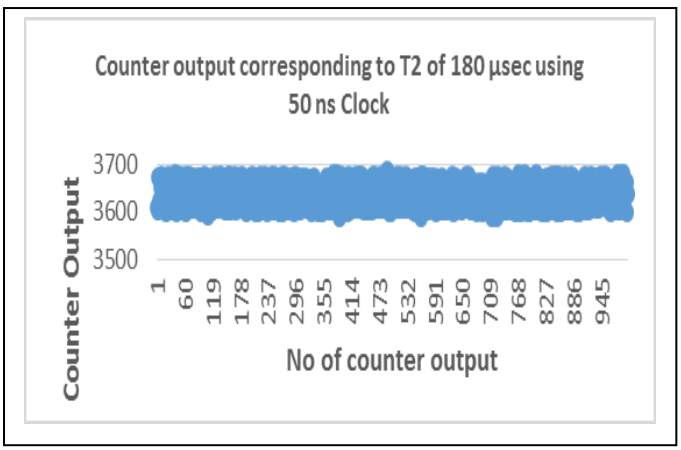

Fig. 8 Counter 1000 readings for time interval T2 of 180 µs

V. CONCLUSION

TDC design is implemented and performance is evaluated as discussed in the above paragraph. Designed system uses programmable TDC which gives user choice for selection of time interval measurement range and resolution. Range of TI gets decided by ramp duration and no of bits of counters whereas resolution of time interval measurement is dependent on the clock period. Further input TI is elongated by stretching factor K, which improves the resolution offered by TDC. TDC design can utilize higher frequency of crystal controlled oscillator which can give better resolution for time interval measurement.

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