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Programmable DC Electronic Load for Testing on-Board Voltage Regulators

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***Abstract* — Many modern applications contain embedded processors and wireless connectivity and these circuits often have separate power management unit. The purpose of the power management unit is to manage power requirements of various SOC and ASIC's by providing required voltage and current in an optimal form. In a Solid State Drive (SSD), components like DRAM, Flash memory, Controller etc. requires specific voltage and current with tight tolerances for the reliable operation. Prescribed voltage and current has to be maintained by the Point of load DC-DC converter, with disturbances within the tolerance level. Proper testing and validation of Point of load (POL) DC-DC converter is essential to decide the performance of an SSD. DC electronic loads are used to emulate the characteristics of various loads in an SSD. The problem with the existing DC electronic loads is that they require wire and cables to connect to the board due to their dimensions. Cables will introduce inductance in the load current path and affect the testing results, especially the current slew rate. The Objective of this project is to design and develop a high slew rate Programmable DC electronic load which is operated as Constant Current Sink and emulates the characteristics of an SSD load such as NAND flash memory, DRAM, controller and other SOC's.**

Keywords— SSD; POL DC-DC converter; Power Management ;Electronic load; Programmabilty.

I. INTRODUCTION

Today's Application Specific Integrated Circuits (ASICs) and System on chips (SOCs) tend to operate at higher currents and lower voltages than their predecessors. Consequently, power supply requirements have become more stringent with typical requirements include low voltages, high currents, fast transient response, tight regulation and supply voltage sequencing. Failure to meet the output voltage, power-on sequencing, and soft-start requirements can result in unreliable power-up and potential damage to the ASIC's and SOCs.

In order to meet the demand of high current and low voltage, circuit manufacturers often rely on discrete power solutions that are complex and take up valuable space and have significant limitations on their power output. Point of Load (POL) regulation has been incorporated into power management systems to meet the power requirements of processors, ASICs and core. In contrast to a controller IC, POL switching regulator ICs integrate the power MOSFETs as well as the control circuitry into a single integrated circuit. POL offers benefits like, high performance, high efficiency, high reliability, smaller and fewer external components and packaging.

In the design of POL switching regulators, the amount of voltage drop when the load on the POL regulator increases and response time of the regulator are key factors of consideration. Tight load regulation and faster loop response is critical to avoid performance problems in sensitive loads like processors, SOCs and ASIC's.

An SSD's power management section incorporates various Point of Load DC-DC converters with low voltage and high current rating that caters the power requirements of the NAND Flash memory, DRAM, Controller and other SOCs. The various voltage levels of these POL DC-DC regulators are 3.3V, 1.8V, 0.9V 1.5V etc with the current limit up to 6A and slew rate up to 20A/µS

POL DC-DC converters require faster loop response and significantly higher loop bandwidth to maintain significantly stable output voltage under the fast fluctuating load conditions. Load transient testing is one of the best ways to check voltage regulators behaviour on several aspects. Applying a fast load transient to any voltage regulator will excite the control loop over a very wide frequency and stressing the control loop towards its stability limits.

A high slew rate DC electronic Load excites the control loop of a POL DC-DC converter with fast load step thus observing the output voltage for optimum regulation. High slew-rate load step also depicts the converter's regulation speed and highlights loop stability problems. Other power converter aspects like input voltage stability, slope compensation, and layout problems can be quickly.

2. LITERATURE SURVEY

Solid state drives promise to greatly enhance enterprise storage performance [1]-[2]. SSDs provide the access time or data transfer rate performance required in demanding enterprise applications online transaction processing, cloud computing, and data mining. Client applications also demand SSDs an alternative to electromechanical disk drives that can enhance the response time and performance substantially, use less power, and fit in smaller mobile form factors.

In light of these demands, chip architects have moved towards tightly integrated System-on-Chip (SoC) that incorporate multiple cores and heterogeneous components such as memory, hardware accelerators controllers etc. into a single chip to extract maximum performance out these storage devices [3]. Compared with the traditional multi-chip system on a board, SOCs offer benefits including higher performance, lower power consumption, smaller size, and enhanced reliability. Different types of cores are usually incorporated into a single SOC design. These cores can

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include CPUs, synchronous RAM, flash memory, digital signal processors, digital-to-analog converters, analog-to-digital converters and phase-locked loops. Efficient power management is an important design element that enables systems developers to overcome increasing demands for low power operation, compact size, and improved functionality. In addition, many electronics systems require low multiple power rails and supply solutions that need to address the few milliamps needed for standby supplies as well as the over 20A requirements for application-specific integrated circuit voltage regulators .

Conventional power management architecture consists of a front-end DC-DC converter, connected to the input voltage source which provides a stable intermediate bus voltage. A number of downstream switch mode power supplies (SMPS) and low-dropout linear regulators are connected to the bus providing multiple output voltages meeting specific steady state and dynamic voltage and current requirements [4].

One of the main drawbacks of the conventional Power management architecture is their size [3].The conventional power management architecture consumes lots of board space, require multiple packages, and add to assembly costs, making them ideal candidates for integration into a power management integrated circuit also known as PMICs. Due to the strict limitation of available space, these architectures are commonly implemented using integrated circuits (ICs), known as power management ICs (PMICs). In PMIC's, the semiconductor switches, along with the controller, gate drivers, and sensing circuitries are packaged on a single silicon die. However, bulky inductors and capacitors often cannot be integrated on a chip or co-packaged with PMICs.

A semiconductor memory, microprocessors, and SoC's furnish transient loads that a voltage regulator must service [3]. Ideally, regulator output is invariant during a load transient. In practice, some variation is encountered and becomes problematic if allowable operating voltage tolerances are exceeded. This mandates testing the regulator and its associated support components to verify desired performance under transient loading conditions. Various methods are employed to generate transient loads, allowing observation of regulatory response [5]

The load transient test is the simplest diagnostic tool available to analyze the loop stability of a DC-DC regulator. The visual appearance of the output voltage as the voltage regulator responds to a change in load current directly correlates to gain and phase margin of the control loop [6]. The voltage regulator must be able to hold its output voltage constant as the load current demand varies anywhere from zero up to full load, even if the change occurs in a relatively short time. The measure of voltage regulator holding its output voltage constant during a step load transient is defined as its load transient response .

3. OPERATION AND DESIGN OF DC-ELECTRONIC LOAD.

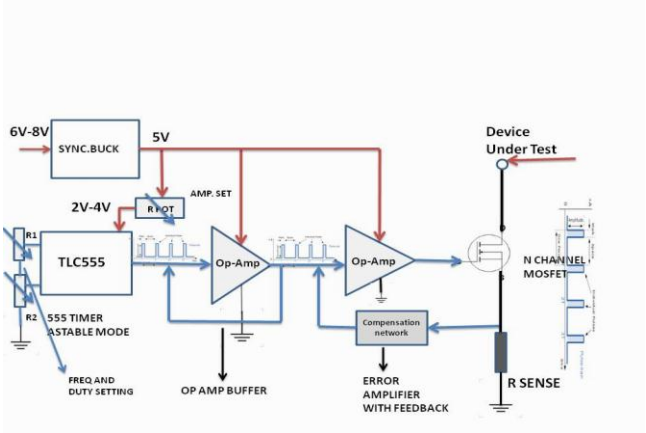

Fig. 1. Block Diagram of Programmbale DC-Electronic load

The Block diagram of programmable DC electronic load is as show in the Fig.1.The input voltage to device is between 6V-10V.Synchronous buck converter regulates the input voltage to constant voltage of 5V.The bias voltage for timer and Op-Amp are derived from the output of buck regulator .IC555 timer generates the required control signal, the output of IC555 timer is continous stream of pulses as per set duty ratio and frequency.An Op-Amp buffer is used to prevent loading on the IC555 timer.Power MOSFET is used to switch the load current of the voltage regulator under test.Error amplifier compares the reference control signal with the voltgae drop across Rsense and modulates the comductivity of the MOSFET such that the error between the refercene and actual current is zero.Error amplifier has to be compensated properly inorder to obtain rinigng free output current.

Design of programmable load.

Power MOSFET is the most critical component of a DC electronic load, switching delay time, slew rate, rise time ,fall time and the gate drive requirement are firmly related to the MOSFET characteristic. Nearly all of the power from the voltage regulator which is being tested has to be dissipated across the Power MOSFET thereby affecting thermal performance and heat sink design, therefore proper selection MOSFET dictates the overall performance of the DC electronic load.

Care must be taken such that the operating point of the MOSFET is within Safe operating area of the MOSFET. During switch mode operation the MOSFET, the goal is to switch between the lowest and highest resistance states of the device in the shortest possible time. Ultimately, the switching performance of the MOSFET transistor is determined by how quickly the voltages can be changed across these capacitors. Therefore, in high speed switching applications, the most important parameters are the parasitic capacitances of the device. These capacitance has to be minimum as possible.

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Selection of Potentiometer R1

Synchronous buck converter provides constant 5V bias to the IC555 timer .A resistor divider network with potentiometer is used to scale down the bias voltage in the range 2V-3V.

The range of potentiometer is calculated from the equation (1)

VDD=VB × [R2 ⁄ (R1+R2)].....(1)

where Vdd is the bias voltage required by IC555 timer

Vb= Output voltage of synchronous buck regulator.

Fixing the value of R2 at 5 K ohm. The range of potentiometer can be found for minimum and maximum values of VDD

For VDD=2V ,VB=5V and R2=5K Ω

R1=7.5K Ω

For VDD=3V, VB=5V and R2=5KΩ

R2=3.33 KΩ

Therefore a surface Mount Potentiometer of the range 1 K ohm to 10 K ohm is chosen for this project.

External components of IC 555 timer

In the circuit 3., while charging, the capacitor charges through R1 and D1 by passing R2. While discharging, it discharges through D2 and R2.

Therefore, the charging time constant is given by

Ton = 0.693 X R1 X C ..... (2)

The discharging time constant given by

Toff = 0.693×R2 × C.....(3)

Therefore, the duty cycle D is given by

D = R1÷(R1+R2).....(4)

Total Time Period T can be expressed as

T=Ton+Toff.....(5)

The switching frequency F can be computed from the equation

F=1⁄T.....(6)

For switching frequency 1KHz and 50% duty ratio .

If R1 is set at 10KΩ

R2 can be calculated from equation (4) for 50% duty ratio

R2=10KΩ

The value of Capacitor C can be computed from the equation (2)

C=9.5µF

4. SIMULATION RESULTS

Simulation of programmable DC load is carried out in TINA design suite developed by texas instruments.

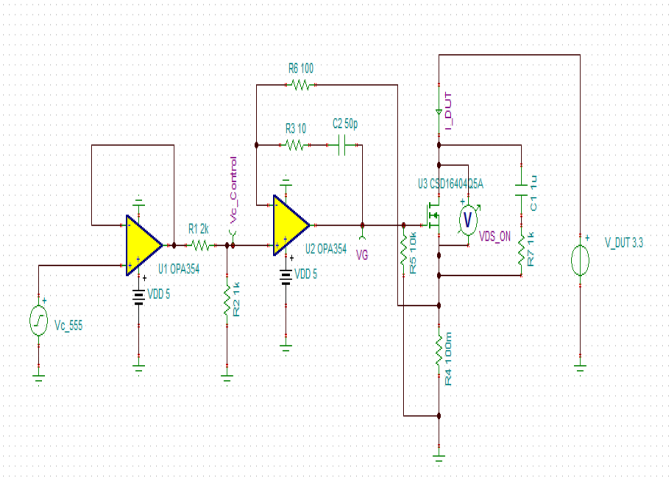

Fig.2 Simulation setup of DC Electronic load

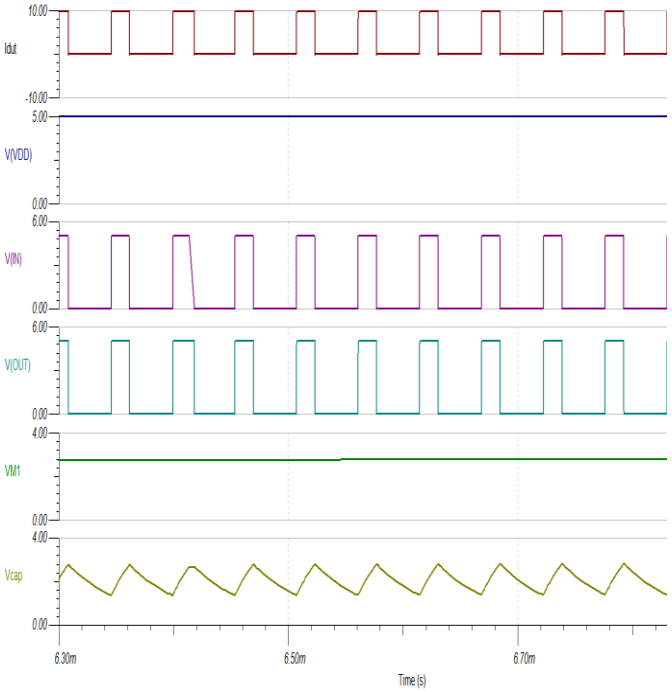

Fig.3 Waveforms of DC Electronic Load

Simulation setup and waveforms of DC electronic load are as shown in Fig.2 and Fig 3.The control signal for the load is derived from IC555 timer (not shown in simulation) .Voltage regulator under test is modeled as constant voltage source V_DUT. Current I_DUT can be controlled by control signal by setting the frequency, duty ratio and amplitude of the IC555 timer .

5. HARDWARE SETUP AND RESULTS.

Hardware setup of programmable DC electronic load is as shown in the Fig.6

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Fig.4 Hardware setup of DC Electronic load

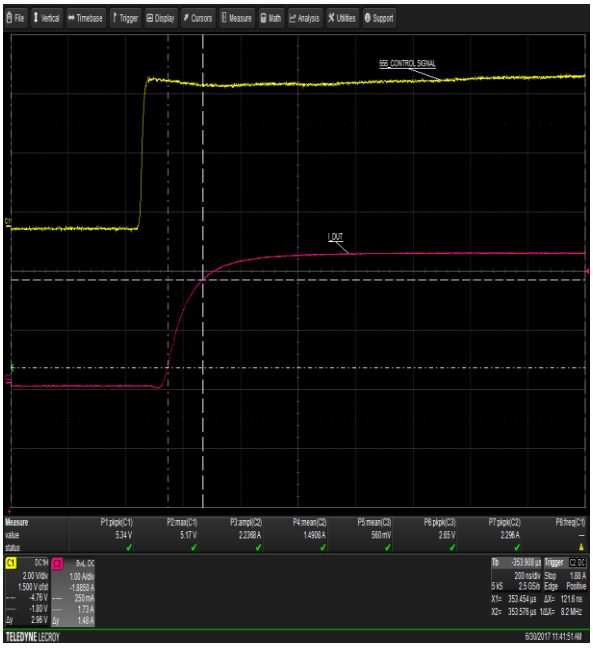

Fig.5. Slew-rate measurement waveform

Fig.6 Load transient waveforms of DC Electronic load

The hardware setup and waveforms are as shown in the Fig.4, Fig.5 and Fig.6 TPS65342A buck converter is used for testing the load transient behavior .The frequency of the load transient is set to 1KHz with amplitude of 3A peak. The duty cycle is set to 50%. The max slew rate obtained is 20A/µs

6. CONCLUSION

This paper shows the implementation of high slew rate DC electronic load used in testing of on board voltage regulators in an SSD. It also shows the method to overcome slew rate limitation faced with traditional bench top DC electronic load. The solution is implemented with the help of minimal possible components such as IC555 timer, Op-Amp, MOSFET and few external passive components. The Dimension of the PCB is 40mm×40mm. Thus enabling verification of small DC voltage regulator modules with ease. slew rate of 20A/us and maximum current rating of 6A peak with 5KHz transient and duty ratio of 50% achieved considering thermal limitations.

7. REFERENCES

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