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Pre-Silicon Validation Techniques to Improve Robustness of an IP

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Abstract— **Pre-Silicon Validation is a collection of activities that is performed for functional correctness, complying with timing, power and performance constraints of an Analog or Digital Circuit in an Intellectual Property (IP). It sometimes also involves preparing test-cases for Post Silicon Validation activities for testing robustness against physical stress or thermal glitches in the environment of a design by manufacturing a test-chip. Meeting the timing criteria of a digital circuit is crucial in the operability of the design along with synchronized clock signals in most cases. It is also essential that the logic stabilizes itself on a expected value within a stipulated time ensuring robustness in the value generated. It is harder to meet such constraints when significantly large circuits are designed and hence it's necessary to functionally validate these timing paths through suitable techniques which can be used to assure if critical timing paths are being met. This paper discusses about Robust Path Delay validation techniques and also about Test vectors generation for Post-Silicon Validation activities to improve robustness of testing a design implemented on a Test-chip.**

Keywords—Pre-Silicon Validation, IP ,Robust Path Delay Testing, Test chip

I. INTRODUCTION

A Silicon IP is a reusable design which is an intellectual property of a particular company/party. Semiconductor engineers design Analog /Digital circuits using Electronic Design Automation (EDA) tools. These designs are done which are mapped to a particular technology for example 10nm, 12nm etc. The circuits which are critical for the operation of any chip for example an entire processor chip needs multiple standard cells, analog cells, Analog Digital Converter (ADC) etc.;. These cells needs to be silicon proven .Silicon proven means to ensure the logic realized on software can be implemented on Silicon with a few admissible margins for the said technology. It is also necessary that these cells not only work in their optimum best in normal conditions but also work efficiently in various Process, Voltage and Temperature (PVT) conditions. The collection of these conditions are called as PVT and these conditions affect the performance of any device.

The test chip is used to verify if the IP is designed correctly and meets the functional specifications of the protocol. It is also used to verify that IP is provided with sufficient margin to mitigate deviations due to process tolerances. A series of rigorous validation and testing activities are performed at the pre-silicon and post-silicon levels to provide a specific level of understanding and confidence in the performance of the mounted chips. The verification and validation boundary conditions are illustrated in figure as shown in Fig 1.

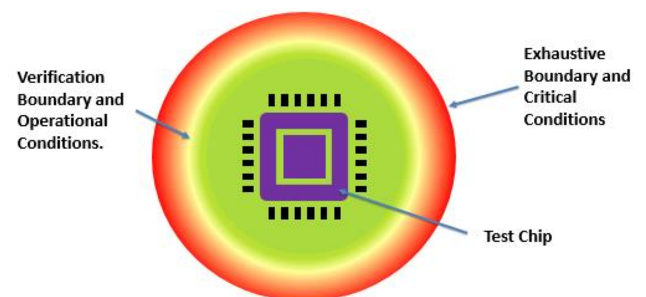

Fig 1: Test Chip depicting it's Verification & Validation boundary conditions

All high performance hardware IP goes through this test chip/ silicon validation process. Marginality is often identified at this stage [2].Test Chips play a crucial role when futuristic nodes are being developed or explored as these research activities become important before the IP is released into the market for chip integration and mass scale fabrication. It is also important to avoid huge losses if any failure is found after tape-out of a mass produced chip as these IP's are complex in their functionality. The following paper discusses

II. SILICON VALIDATION

A. *Design & Specifications Review*

The first step involved in pre silicon validation usually involves design review. The architecture of the design is analyzed and various key testing blocks incorporated are reviewed. The designs are written in Hardware Descriptive Language (HDL) adopting various modelling techniques such as behavioral, gate level or sometimes mixed level modelling.

B. *Verification*

Functional Verification of Design is the process of analyzing the functional correctness of the RTL. It is mainly done to identify any bugs present and to check if the specifications of the design are being satisfied. It is a crucial step in analyzing the design. It is necessary that the design is free of bugs and harmful bugs if any are identified at the initial stages. In the initial stages only the high level architectural specification of the designs are available. Abstract virtual models are obtained later and are primarily employed as a prototyping framework for development and validation.

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C. Silicon Validation

Validation activities essentially involve performing and running test cases on a simulator in a lab setup. In order to ensure re-spins are avoided at this level, Pre-silicon validation is performed on the prototyped chip before tape-out. These validation sets are performed at various PVT corners of the design to understand how the behavior of the design is affected at varying processes, threshold voltages and temperature conditions.

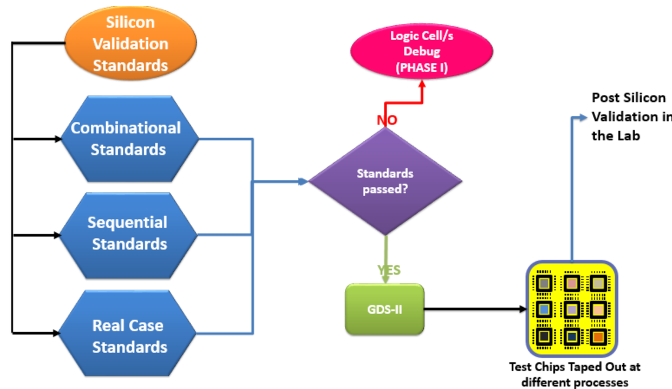

Fig 2: Pre Silicon Validation

The Pre Silicon data collected is crucial for analyzing and correlating the timing windows and power values of circuits with Silicon data obtained while performing Post Silicon Validation. The Pre Silicon validation meets a sets of standards as depicted in the flow shown in Fig 2. Test vectors for performing various testing activities is also generated in the Pre-Silicon Validation phase. These test vectors have to be robust in order to ensure that the timing paths evaluated don't fail their constraints. Different kind of test vectors for testing the behavior of the blocks to meet timing, functionality are generated and are run at system speeds.
Delay testing plays a crucial role to meet timing on chip while testing to mitigate paths that could potentially harm the chip's performance when the required timing window isn't met.[5] Though it's harder to model the same on software at times, it becomes essential to generate test vectors to analyze the circuit's behavior for all timing paths and hence understand how timing of these chips can be guaranteed. Static Timing Analysis is hence done at this stage additionally to ensure the design is optimal and meets the Performance, Power and Area (PPA) mitigating unnecessarily complicated designs and prevent silicon escapes and performance based yield loss.[4]
Post Silicon Validation happens initially for discrete features and interfaces of the chip and later also involves running real software/applications that stress tests the design features[1]. A post silicon validation environmental setup is shown in Fig 3.

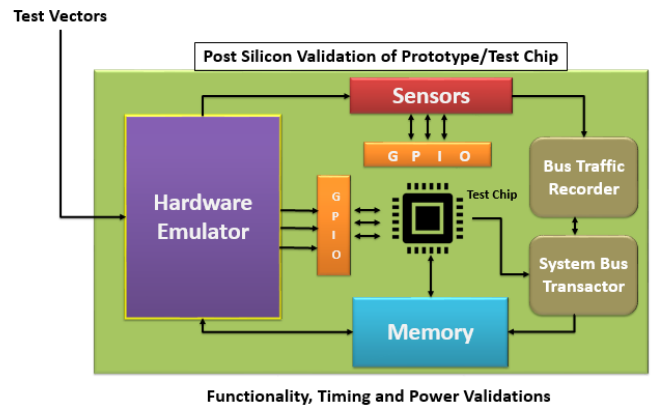

Fig 3: Post Silicon Validation

The test vectors generated are applied on the test-chip fabricated and the tests are run at system speeds.

D. Correlation of Validation data

Once the Post Silicon testing is done based on the defined testing plan, the data is collected and correlated with Pre-Silicon data comprising of timing, power values, leakage current's etc. and conclusions are done based on how the design has performed at various types of testing as shown as an example in Fig 4. The test vectors generated will play a vital role in this process to determine faulty timing paths or abnormal values if any.

III. PRE-SILICON VALIDATION TECHNIQUES FOR ROBUSTNESS OF DESIGN

Preparing an effective test plan for validating the timing of the circuits efficiently is an important factor in determining robustness. The following technique describes a static timing analysis based path selection method.
The arrival time of various signals are distilled using STA and hence more precise path delays are obtained to enable higher correlation ratio between STA and silicon data. This technique hence results in a more accurate detection of potentially detectable path delay faults with critical paths based on precise estimates.

A. Essential Input Allocation

Essential input assignments include the values that a test for the faults must assign to lines in the circuit. The inputs necessary assignments are computed in polynomial time and provide a unique framework for identifying undetectable faults and for generating tests for undetectable faults[1] .Considering path delay faults, these input allocations provide a integrated structure to identify undetectable faults and to generate tests for detectable faults in standard scan circuits.

B. Collection of Path Delay Faults

The goal of the test generation procedure is to ensure that the inputs allocations mitigate the path delay faults associated with long paths in a circuit. Considering the process of ordering longest path lengths. A set of path delay faults can be defined for each path delay fault separately. The number of paths considered for test vector generation are restricted to a constant N.

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Paths of length L can be listed by extending sub-paths starting from inputs. Path counts reaching greater than N can be stored for later consideration [1].Once the set of path delay faults are exhausted, the remaining paths can be restored.

C. Detection of Path Delay Faults

Path delay faults can be detected robustly using high quality test patterns for which the off path inputs are static non- controlling values. If the controlling values of a gate is 1 in the case of an OR gate, the off path input is controlled to static. The robust path tests sensitize the path of interest only. [2]It is important to choose the correct set of paths for correlation since it can have implications on the feasibility and usefulness of the correlation analysis. Static timing paths inside involving a hard macro such as a memory is usually not considered as it may be extremely difficult to control such a macro entirely. Functional Vector based paths are the paths affected by a critical timing vector. The paths provide a good set of data for analyzing path delay faults.

IV. RESULTS AND DISCUSSION

The functional test vectors generated for testing and the STA based path delays estimation helped in understanding the critical timing paths. The delay measured and the silicon data are correlated. The various timing paths analyzed for set of N paths are depicted in Fig 4.

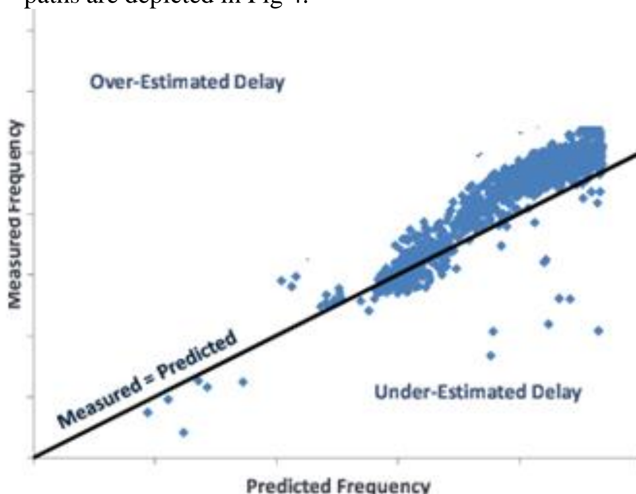

Fig 4: Correlation of Pre Silicon and Post Silicon Timing Data

The STA timing are analyzed at slow device .The graph in Fig4. also depicts that the median silicon data is fairly in correlation with typical STA. The Silicon delay points were calculated from the spread of readings across multiple timing paths ranging from 150 to 200.

It is also understood that the good correlation of the data is predicted by path delay tests which are robust in nature. This also eliminates delay from off path inputs. The confidence in the design also increases substantially when the timing constraints are met and hence this methodology serves vital for Silicon validation process in the current newly addressed nodes.

CONCLUSION

In summary, the following paper discusses about Pre-Silicon validation techniques that will help improve correlation methodology by employing Path Delay testing The path delay faults pattern based STA signoff will prove important in timing critical designs and in IP's. The methodology can be extended to denser circuit chains and also can be improved in future research activities by optimizing the way how the path delay faults are identified.

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