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# Power Stress Reduction In Single-Stage Power Factor Correction By AC/DC Fly Back Converter

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## Abstract

This paper discusses the major issues that exist in the single-stage ac/dc converters with power factor correction (PFC) and presents a novel converter based on a quasi-active PFC scheme. Two additional windings wound in the transformer of a conventional dc/dc fly back converter are used to drive and achieve continuous current mode operation of an input inductor. In addition, direct energy transfer paths are provided through the additional windings to improve the conversion efficiency and to reduce the dc bus capacitor voltage below 450 V for universal line applications. The proposed converter can be easily designed to comply with IEC 61000-3-2 Class D requirement and to achieve fast output voltage regulation. By properly tuning the converter parameters, a good tradeoff between efficiency, dc bus capacitor voltage stress, and harmonic content can be achieved. Operating principles, analysis, and experimental results of the proposed method are presented.



## 1.Introduction

**R**ECENTLY, many high-frequency active power factor correction(PFC) topologies and current shaping techniques for ac/dc converters have been developed [1] to meet standards such as IEC 61000-3-2. In conventional converter design, a two stage scheme was usually employed insimultaneously performing PFC and fast output regulation by using two independent controllers and optimized power stages. However, the cost and complexity of the converter increases with the increased component count. A cost-effective solution known as a singlestage PFC (S2PFC) converter was developed, in which the PFC stage and the dc/dc converter are combined into one stage [2]–[4]. These S2PFC converters usually use a boost converter to achieve PFC with discontinuous conduction mode (DCM) operation. A detailed review of the S2PFC topologies using DCM boost converter is presented in [3].Some other integrated S2PFC schemes are also implemented using DCM buck-boost or buck converter [5]–[9]. Generally, the power factor (PF) of a conventional two-stage converter is much higher than the single-stage scheme. However, the input current harmonics of S2PFC converters still can meet the regulatory standards. Although the single-stage scheme is attractive in low-cost and low-power applications due to its simplified power stage and control circuit, major drawbacks such as low efficiency, high dc bus voltage stress, and working in DCM of the input PFC stage still exist. The DCM operation gives a lower total harmonic distortion (THD) of the input current compared to the continuous current mode (CCM). On the other hand,the CCM operation yields a slightly higher efficiency compared to the DCM operation [19].

To overcome the drawbacks of the single-stage scheme, several converters with input currentshaping have been presented [10], [11], in which a high-frequency ac voltage source is connected in series with the rectified input voltage to shape the input current. The variable switching frequency control technique that

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is proposed in [12] can reduce the dc bus voltage stress. The method is unable to suppress the dc bus voltage below 450 V for universal line applications (100–240 V ac), and it complicates the design of the inductive components due to the wide-range switching frequency operation. Some alternative designs using additional coupled feedback windings are introduced in [13]–[20], wherein the dc bus capacitor voltage is reduced below 450 V. Nevertheless, the feedback windings also induce a dead angle in the input current, hence resulting in a high line current distortion. The coupled feedback winding concept is also implemented using a center tap transformer and a synchronous rectifier to improve the PF and efficiency [21].The converter is operated at the boundary of the DCM and CCM using a variable frequency controller to reduce theswitching turn-on loss. In addition, a dead angle still exists in the input current wave form.The topologies proposed in [22] and [23] overcome the dc bus capacitor voltage stress using the parallel PFC concept.

In this paper, a new quasi-active PFC circuit is presented. The circuit is based on adding two auxiliary windings coupled to the transformer of a cascaded dc/dc flyback converter. The PFC cell is placed between the input rectifier and the low-frequency filter capacitor, capacitor, which is a similar approach to the conventional activePFC design but without an active power switch. Since the dc/dc converter is operated at high switching frequency, the auxiliary windings produce a high-frequency pulsating source such that the input current conduction angle is lengthened and the inputcurrent harmonics is reduced. Furthermore, the high-frequency pulsating source requires smaller size components, resulting to a lower cost. The input inductor current can be designed to operate in CCM. By properly designing the converter parameters, a good tradeoff between efficiency, dc bus capacitor voltage stress, and harmonic content can be achieved. The structure and operating principles of the proposed converter are presented in Section II. The design example and the experimental results are presented in Section III. Section IV gives the conclusion.

## 2. Proposed Quasi-Active PFC Circuit

The proposed quasi-active PFC circuit is discussed in this section. As shown in Figure 1, the circuit is comprised of a bridge

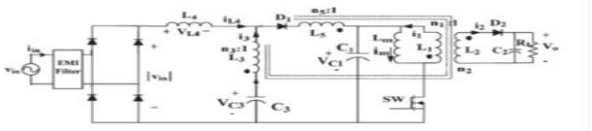

Figure 1.**P**roposed quasi-active PFC circuit diagram.

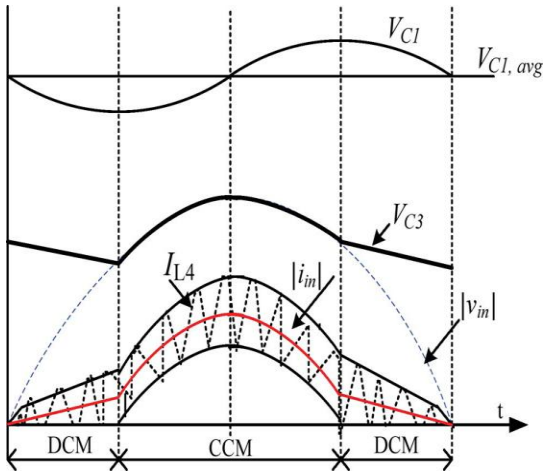


Figure 2. **I**nput inductor current *IL*4 illustrating its conduction modes during half line current period.

rectifier, a boost inductor *L*4, a capacitor *C*3, an intermediate dc bus capacitor *C*1, and a discontinuous input current power load (a DCM fly back converter in this case). Two auxiliarywindings *L*3 and *L*5 are added to the primary side of the transformer in order to shape the input current. In the proposed quasi-active PFC scheme, the dc/dc converter section is not directly involved in the PFC; it simply offers a driving power by applying a series of discontinuous current pulses. Compared to the circuit reported in [35], the proposed circuit shown in Figure 1 is different in two ways: the dotted convention of the third winding (*L*3) of the fly back transformer is reversed, and an additional winding *L*5 is inserted. If the third winding (*L*3) is wound such that the dotted terminal of *L*3 is similar to *L*1 and *L*5 and opposite to the secondary winding *L*2, the circuit operation and analysis will be fundamentally different. Consequently, these changes will bereflected mainly on the input inductor *L*4 which operates in CCM/DCM, as shown in Figure 2.Compared to [35], the input inductor alwaysoperates in DCM. Although the DCM gives lower THD of the line current, however, CCM operation required a smaller EMI filter, and the harmonic content of the line current can still be maintained below the IEC 61000-3-2 Class D requirements. Furthermore adding the winding *L*5 in the proposed circuit offers more flexibility in maintaining the dc bus capacitor voltage *VC*1well below 450 V for universal line flexibility in maintaining the dc bus capacitor voltage *VC*1well below 450 V for universal line applications . As a result, the voltage stress across the power switch can be reduced. In addition, two direct energy transfer paths are provided by the two feedback windings, which can improve the conversion efficiency. When the switch is

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turned on, part of the energy

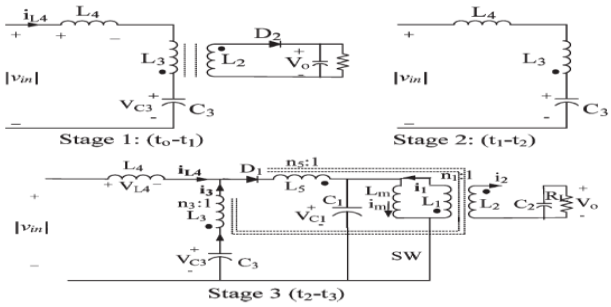


Figure 3. **E**quivalent circuits for the three stages of operation of the proposed pfc circuit

.rom the input inductor is directly transferred to the transformer. When the switch is turned off, part of the energy.from the input is transferred to the secondary output capacitor through the winding *L*3. As a result, the conversion efficiency is expected to remain high, as achieved in Furthermore, the size of the capacitor *C*3 in series with the winding *L*3 is smaller

To simplify the analysis, the following assumptions are made.

1) All semiconductor components are ideal.

2) The power transformer is ideal (no leakage flux).

3)The voltages across the capacitors are constant.

4) The switching frequency is much higher than the line frequency. Therefore, the input voltage is constant during a switching cycle.

## 2.1. Operation stages

This section presents the principle of operation of the proposed PFC circuit. A typical input inductor current produced by the circuit is shown in Figure 2. It can be seen that, during a half cycle of the supply, the waveform of the input current *iL*4 always has two parts, namely, the DCM and CCM parts.When |*v*in| < *VC*3, the current *iL*4 is low, and hence, the input inductor *L*4 operates in DCM. With the increase of the input voltage such that |*v*in| ≥ *VC*3, the inductor current increases and becomes continuous (CCM). At steady state, the topology has three operating stages, as shown in Figure 3. The key switching waveforms for bothCCM and DCM parts are shown in Figs. 4 and 5, respectively. *Stage 1* (*to*−*t*1)*:* At *t* = *to*, the switch (SW) is turned off, and diode *D*1 is reverse biased due to (*VC*1 + *VL*5), which is always higher than |*v*in|. The inductor *L*4 absorbs energy from the input source, and therefore, the current *iL*4 is increased linearly. During this stage, the capacitor *C*3 is charging. Meanwhile, diode *D*2 is forward biased, and the load absorbs energy from both the magnetizing inductor through primary winding *n*1 and the input voltage through the auxiliary winding *n*3. Therefore, there is a DPT from the input source to the load during this

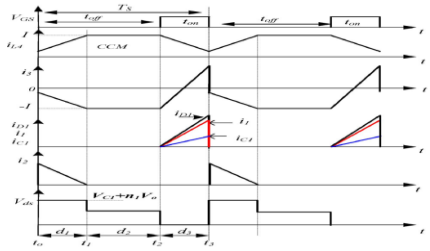

Figure 4. **K**ey switching waveforms of the proposed PFC with CCM operation

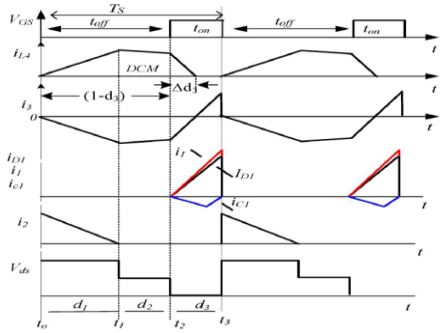

Figure 5. **K**ey switching waveforms of the proposed PFC with DCM operation.

period. As a result, the efficiency is improved. This stage ends when the secondary current *i*2 becomes zero at (*t* = *t*1)

*Stage 2* (*t*1−*t*2)*:* During this stage, the switch (SW) and both diodes *D*1 and *D*2 are turned off. The input current continues to flow through the circuit formed by |*v*in|, *L*4, *L*3, and *C*3. The capacitor *C*3 is still charging at this stage. The current *iL*4 slightly decreases when |*v*in| < *VC*3 (for DCM part) and is constant when |*v*in| ≥ *VC*3 (for CCM part).This stage ends when the switch (SW) is turned on at *t* = *t*2.

*Stage 3* (*t*2−*t*3)*:* At *t* = *t*2, the switch (SW) is turned on, and diode *D*1 is conducting. Therefore, the stored energy in *L*4 and *C*3 is transferred to the primary windings *n*1 and *n*5, so more energy is stored in the magnetizing inductor of the transformer. Hence, the primary winding current increases linearly. In addition, when |*v*in| < *VC*3 (DCM part), the dc bus capacitor *C*1 discharges its energy to the transformer primary winding. Note that, because |*vin*| is low, the current *iL*4 will decrease to zero (DCM) before the switch is turned off. Once *iL*4 = 0, the capacitors *C*3 and *C*1 continue to supply the energy to the primary windings of the transformer. However, when |*v*in| ≥ *VC*3 (CCM part), the input voltage is high enough such that it can provide most of the energy to the primary windings *n*1

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and *n*5 and also to the bulk capacitor *C*1. Therefore, when the switch (SW) is turned on, the current difference between *iD*1 and *i*1 will charge the dc bus capacitor *C*1.At *t* = *t*3, the switch (SW) is turned off again, and the primary current *i*1 decreases to zero. Therefore, *D*1 is turned off due to (*VC*1 + *VL*5), and the output diode *D*2 is forward biased. The current *i*3 reverses its direction again, where it is equal to *iL*4, and the switching cycle repeats.

## 2.2. Steady-State Analysis

The voltage conversion ratio of the proposed converter can be estimated from the volt-second balance on inductances and theinput–output power balance. Consider the waveforms shown in Figure (5) From the volt-second balance on *L*4, it yields

$(|v_{in}|+n_3v_0-v_{c3})d_1=(v_{c3}-|v_{in}|)d_2+(v_{c1}(1+\frac{n5}{n1})-|v_{in}|)\,\Delta\, d_3(1)$

where*d*1 is the on-time of the output diode *D*2, *d*2 is the time period when the switch (SW) and both diodes *D*1 and *D*2 are turned off, and *d*3 is the on-time of the switch (SW).

From the volt-second balance on *L*3, it yields

$$n_3v_0d_1=(v_{c1}\left(1+\frac{n_5}{n1}\right)-(v_{c3})d_3=(\frac{n_3}{n1})v_{c1}d_3$$

or

$n_3v_0d_1=(v_{c1}-(v_{c3})d_3=(\frac{n_3-n_5}{n_1})v_{c1}d_3(2)$

From the volt-second balance on *L*1(*Lm*)

$$n_3v_0d_1=v_{c1}d_3 \qquad (3)$$

From (2) and (3), we can derive

$\frac{v_{c3}}{v_{c1}}=1+\frac{n_5}{n_1}-\frac{n_3}{n_1}=\frac{n_3-n_5-n_3}{n_1}=\frac{d_1}{d_3}$ (4)

Now, the average inductor current

$$I_{L4}=\frac{T_S}{2L_4}\Big[(V_{C3}-n_3V_0-|V_{in}|)d_1(d_1+d_2)+\left(v_{c1}\left(1+\frac{n_5}{n_1}\right)-|v_{in}|\right)\Delta d_3(d_2+\Delta d_3)\Big] \qquad (5)$$

From (2), we have

$$v_{c1}=v_{c3}+(\frac{n_3-n_5}{n_1})v_{c1}$$

$I_{L4}=\frac{T_S}{2L_4}[(v_{c3}-n_3v_0-|v_{in}|d_1(d_1+d_2+(v_{c1}\left(\mathbf{1}+\frac{\boldsymbol{n_5}}{\boldsymbol{n1}}\right)\boldsymbol{v_{c1}}-(\boldsymbol{v_{in}}))\times\Delta d_3(d_2+\Delta d_3)]$ (**6**)

$I_{L4}=\frac{T_S}{2L_4}[(v_{c3}-|v_{in}|\text{A}-n_3v_0d_1(d_1+d_2)+(\frac{n_{3-n_5}}{n_1})v_{c1}\Delta d_3(d_2+\Delta d_3)]$ (7)

where $\text{A}=d_1(d_1+d_2)+\Delta d_3(d_2+\Delta d_3)]$

Substituting for $n_3v_0$from (2) into (7) yields

$I_{L4}=\frac{T_S}{2L_4}[(v_{c3}-|\text{v}_{\text{in}}|\text{A}+\frac{n_{3-n_5}}{n_1})v_{c1}(\text{B})]$ (8)

Where $\text{B}=-d_3(d_1+d_2)+\Delta d_3(d_2+\Delta d_3)$

In Figure 5, it can be seen that $d_1+d_2=1-d_3$

$\text{A}=d_1(1-d_3)+\Delta d_3(d_2+\Delta d_3)$, and

$\text{B}=-d_3(1-d_3)+\Delta d_3(d_2+\Delta d_3)$.

The discharging time $\Delta d_3$ can be found from (1) as

$\Delta d_3=\frac{(|v_{in}|-v_{c3})(d_1+d_2+n_3v_0d_1)}{v_{c1}\left(1+\frac{n_5}{n1}\right)-|v_{in}|}$.

or

$$\boldsymbol{\Delta d_3}=\frac{(|v_{in}|\_v_{c3})\left(1-d_3+\frac{(n_3}{n_1}\right)v_{c1}d_3}{v_{c1}\left(1+\frac{n_5}{n1}\right)-|v_{in}|} \qquad (9)$$

.

Therefore , for the DCM part of the input current $I_{L4}$, $\Delta d_3\leq d_3$. At the boundary condition

$$\Delta d_3=d_3 \qquad (10)$$

Substituting (10) into (9) yields

$(\boldsymbol{v_{in}})=\boldsymbol{v_{in}}=v_{c3}$. (11)

Substituting (10) and (11) into (8) yields the input current atthe boundary condition

$$\boldsymbol{I_{L4}}=\frac{\boldsymbol{T_S}}{\boldsymbol{2L_4}}[\frac{\boldsymbol{n_3-n_5}}{\boldsymbol{n_1}}\boldsymbol{v_{c1}d_3(d_3+d_1)}]$$

$$=\frac{\boldsymbol{T_S}}{\boldsymbol{2L_4}}(\boldsymbol{v_{c1}}-v_{c3})\boldsymbol{d_3(d_3-d_1)}$$

$\boldsymbol{I_{L4}}=\frac{\boldsymbol{T_S}}{\boldsymbol{2L_4}}(\boldsymbol{v_{c1}}-|\boldsymbol{v_{in}}|\boldsymbol{d_3(d_3-d_1)})=\frac{|v_{in}|}{2_{l4}}(\frac{v_{c1}}{|v_{in}|}-1)d_3^2T_S(1-\frac{\text{d}_1}{\text{d}_3})$. (12)

Substituting (4) into (12) yields

$$I_{\text{in}}=I_{L4}=\frac{|v_{in}|}{2_{l4}}\frac{n_3}{n_1-n_3-n_5}\boldsymbol{d_3^2}T_S\left(\frac{n_{3-n_5}}{n_1}\right) \qquad (13)$$

where|*v*in| = *Vm*sin(*ωt*). The average input power is given by

$$P_{in}=\int_0^{\pi}|V_{in}|I_{in}\,d\omega t$$

*P*in

$$=\frac{{v_m}^2}{4_{l4}}\frac{n_3}{n_1-n_3+n_5}\boldsymbol{d_3^2}T_S\left(\frac{n_{3-n_5}}{n_1}\right) \qquad (14)$$

where$V_m$is the peak value of the input voltage. The averageoutput power of the DCM flyback converter [26] is given by

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$$P_0 = \frac{V_{C1}^2}{2L_m} d_3^2 T_s \quad (15)$$

In a half line cycle, the input energy is equal to the outputenergy at steady state such that *P*in = *Po*. Therefore, the dc buscapacitor voltage is written as

$$v_{c1} = v_m \sqrt{\frac{n_3}{n_1 - n_3 + n_5} \times \frac{l_m}{2_{l4}} \left(\frac{n_3 - n_5}{n_1}\right)} \quad (16)$$

From (16), it can be seen that the dc bus voltage *VC*1 is independent from the load changes, and it is a function of theinductance values, turn ratios, and input voltage. Therefore, high voltage stress can be overcome byproperly designing the ratio of the inductance ratio *Lm*/2*L*4 and the number of turns *n*1, *n*3, and *n*5.

## 3. Design Example and Experimental Results

The performance of the new quasi-active PFC circuit shown in Figure 1 was designed and experimentally verified. The main design objectives of the proposed circuit can be divided into two directions. First, it achieves low THD of the line current to comply with the IEC 61000-3-2 Class D standard with a CCM operation of the input inductor (*L*4) as much as possible. Second, it limits the voltage stress of the dc bus capacitor *VC*1 below 450 V for a universal input voltage (100–240 Vac). From the preceding analysis in Section II, assuming that the secondary winding *n*2 = 1, it is found that the number of turns (*n*1, *n*3, and *n*5) and the inductors ratio *Lm*/2*L*4 are the key design parameters. Specifically, the turns ratio (*n*3/*n*1) has a significant impact on both the quality of the input current and the dc bus capacitor voltage. The DCM flyback converter was designed for *V*in,rms (100–240 V), *Vo* = 50 V, and output power of 80 W, and the overall efficiency of 86% is assumed.The switching frequency is 100 kHz, and the maximum duty cycle is 0.45

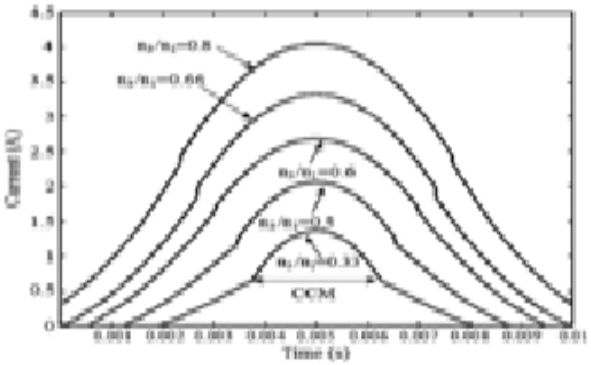



Fig 6.**A**verage input current waveform for a half line cycle and difference turns ratio($\frac{n3}{n1}$)

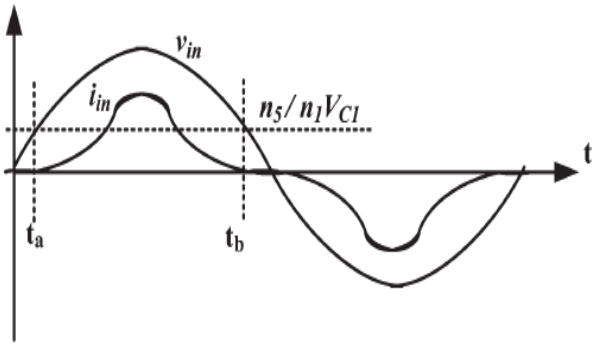



Figure 7. **I**nput voltage and current waveforms showing the effect of the numberof turns n5

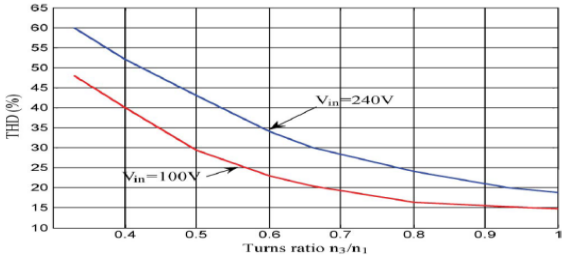



Figure 8. **THD** of the input current as a function of the turns ratio (*n*3/*n*1).

Based on (8) and (9), Figure 6 shows the average input current waveform for a half line cycle as a function of the turns ratio (*n*3/*n*1) for an input voltage of 100 V. It is assumed that all of the other parameters are constant. It can be seen that, to reduce the dead angle of the input current and to provide a continuous current flow, the turns ratio (*n*3/*n*1) must be greater than or equal 0.5. In addition, the number of turns*n*5 also affects the dead time of the input current, as shown in Figure 7. The higher the number of turns (*n*5) is, the bigger the dead time will be. Therefore, the turns ratio (*n*3/*n*1) and (*n*5) must also be selected such that the input current delay times (*ta* and *tb*) are approximately equal to zero. Figs. 8 and 9 show the calculated

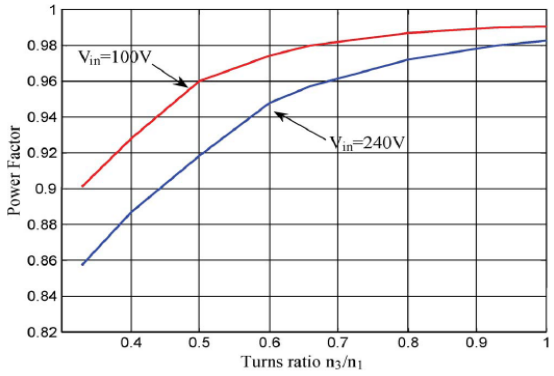



Figure 9 **I**nput PF as a function of the turns ratio (*n*3/*n*1).

Fig. 9. Input PF as a function of the turns ratio ($n_3/n_1$).

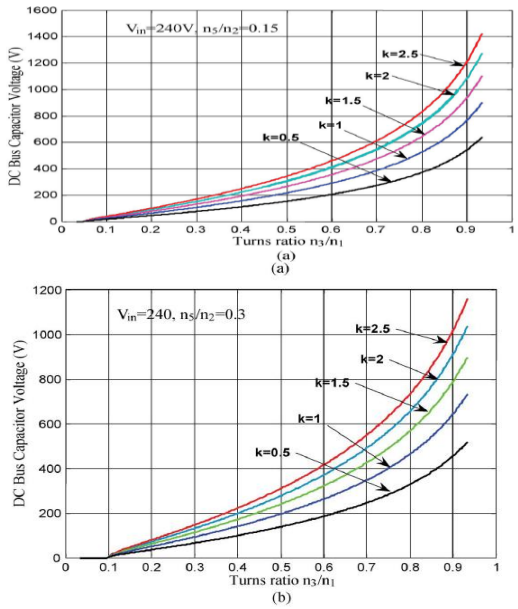



Figure 10. **C**alculated dc bus capacitor voltage versus turns ratio (*n*3/*n*1) for*V*in = 240 V. (a) *n*5/*n*2 = 0.15. (b) *n*5/*n*2 = 0.3.

THD and PF of the input current as a function of the turns ratio (*n*3/*n*1) for input voltages of 100 and 240 V. It can be observed that the turns ratio (*n*3/*n*1) controls the quality of the input current. The higher the turns ratio is, the lower is the THD, and the higher is the PF obtained. However, based on (16), a higher

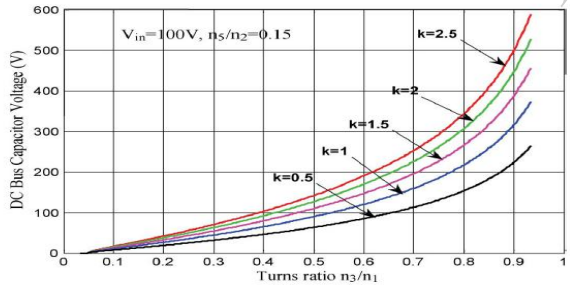
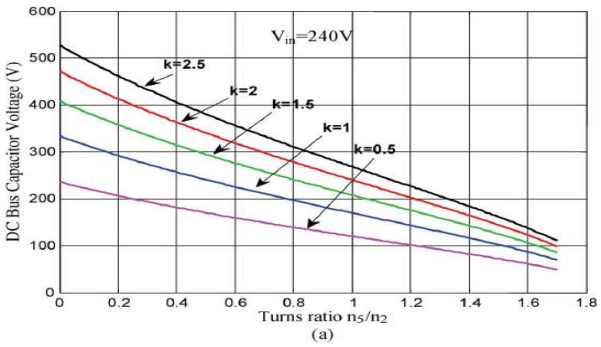



Figure 11. **C**alculated dc bus capacitor voltage versus turns ratio (*n*3/*n*1) for *V*in = 100 V.



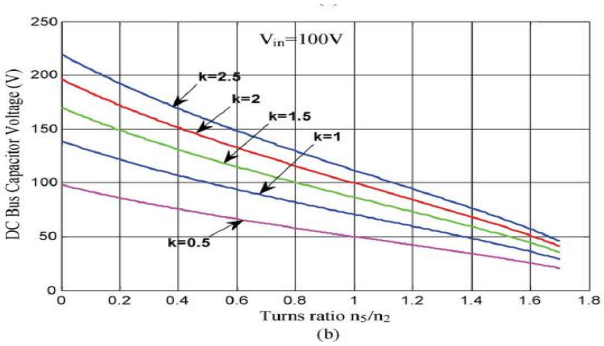




Figure 12. **T**urns ratio *n*5/*n*2 with*n*3/*n*1 = 0.6. (a) *V*in = 240 V. (b) *V*in = 100 V.

turns ratio (*n*3/*n*1) means a higher dc bus capacitor voltage(*VC*1) stress. Figure 10–12 show the relationship between the dc bus capacitor voltage and circuit parameters, turns ratio (*n*3/*n*1) and (*n*5/*n*2), and inductance ratio (*k* = *Lm*/2*L*4) for input

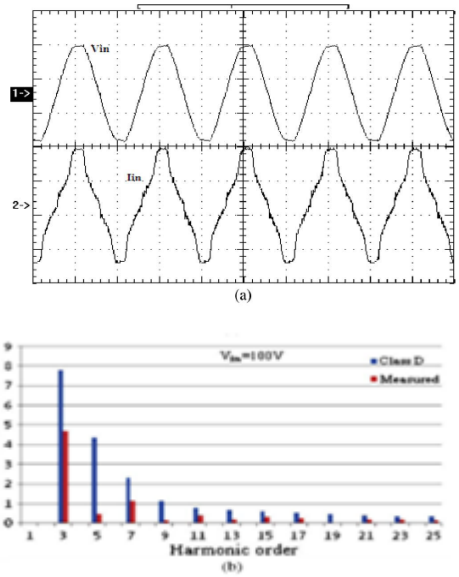



Figure 13. (a) **M**easured input voltage (*V*in; 100/Div) and filtered input current(*I*in; 1 A/Div) for *V*in = 100 V. (b) Corresponding harmonics content(THD = 22%).

Voltages of 240 and 100 V, respectively. It is shown in Figs. 10 and 11 that, for a given value of *k* and *n*5, if the turns ratio *n*3/*n*1 >0.6, the relationship between the dc bus capacitor voltage and the turns ratio becomes nonlinear, and a small change in the turns ratio results in a very high capacitor voltage stress. Therefore, a tradeoff between the input current quality and the dc bus capacitor voltage must be made. For a universal input voltage, the maximum capacitor voltage must be limited to 450 V. Therefore, in Figs. 6 and 8–11, for the range of *k* = 1–2 and for a turns ratio value of *n*5/*n*2. Finally, Figure 12 shows the relationship between the turns ratio *n*5/*n*2 and the dc bus capacitor voltage (*VC*1)

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for a turns ratio $n3/n1 = 0.6$. It can be seen that, for given values of $k$ and turns ratio ($n3/n1$), a higher turns ratio ($n5/n2$) leads to a lowercapacitor voltage ($VC1$). However, a higher turns ratio ($n5/n2$) may induce a dead time in the input current, as shown in Figure 7. Therefore, $k$ = 2and $n3/n1 = 0.6$ and $n5/n2 = 0.2$ are selected in this design, which ideally give $VC1 \approx 408$ V for $Vin = 240$ V. However, practically, the voltage $VC1$ could be lower due to unavoidable circuit losses. In addition, a capacitor with a voltage rating of 450–500 V could be used since it is available in the market. The conventional fly back transformer is constructed with the number of turns $n1 = 46$, $n2 = 15$, $n3 = 28$, and $n5 =$ 3and magnetizing inductance $Lm = 200\ \mu$H. The input inductor $L4 = 50\ \mu$H. The capacitor values are selected as $C1 =$

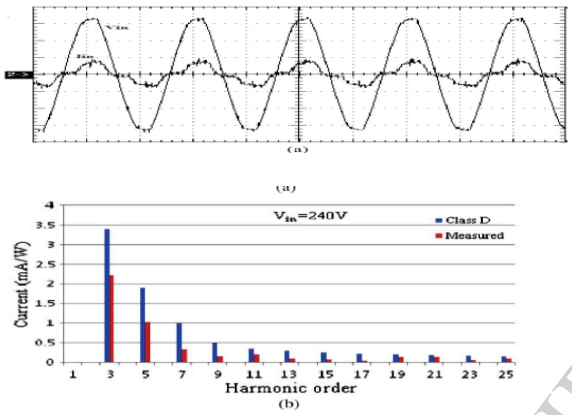



Fig 14. **M**easured input voltage (v in ;100/div) and filtered input current(b)corresponding harmonic current

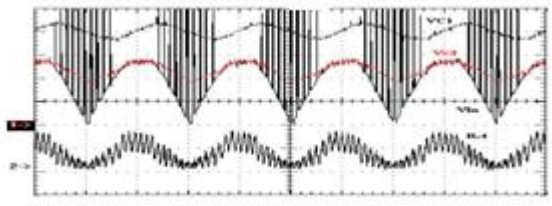


Fig 15. **M**easured waveforms for $V$ds (switch voltage) 47 $\mu$F/500 V and $C2 = 2\times 470\ \mu$F.

Assuming that$\Delta Vc3 = 100$ V, $P$in,min = 15 W, $V$rms = 240 V (worst cases cenario) , $t = 10$ ms (half of the half line period for discharge),and then $C3 \leq 6.25\ \mu$F. Therefore, $C3 = 4.7\ \mu$F/450 V is selectedsuch that $VC3$ follows the input voltage, and the capacitor has to be discharged much faster than the 50-Hz input. Based on the aforementioned design example, the converter was built using the following components: the diode bridge = KBU8J, $D1$ = MUR1560, $D2$ = MUR1510, and SW = SPW22N60C3. Figure 13(a) shows the measured waveforms of the input voltage and input current for a100-Vac input voltage. The harmonic content of the input current compared to Class D regulation standard is shown in Figure 13(b). Similarly, Figure 14(a) and (b) shows the

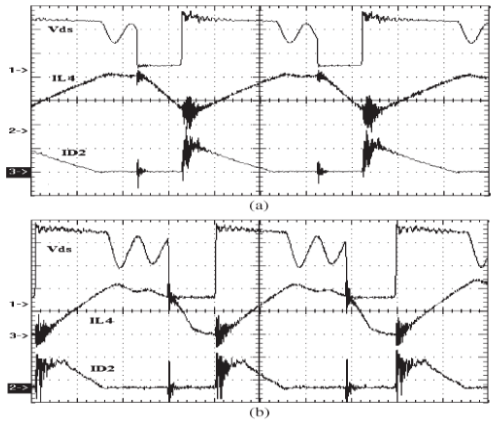



Figure 16. **M**easured waveforms for $V$ds (switch voltage), $IL4$, and $ID2$. (a) CCM operation. (b) DCM operation

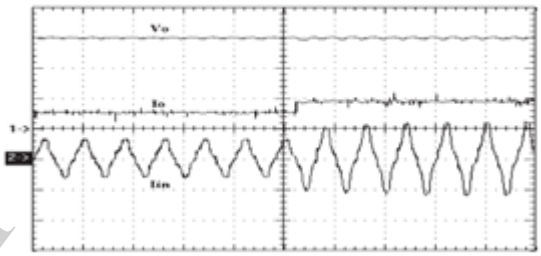
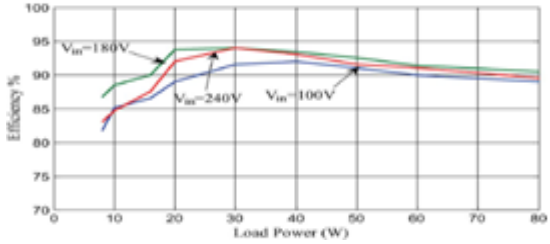



Fig 17. **T**ransient response for a step load change

measured input voltage, input current, and harmonic content for$V$in = 240 V. It can be observed that the standard specification IEC 61000-3-2 Class D is easily fulfilled. Figure 15 shows the measured waveforms of the rectified input voltage, capacitor voltage $C3$, dc bus voltage $VC1$, and input inductor current$iL4$. It can be observed that, when $|vin| < VC3$, the inductor current is in DCM, and when $|vin| = VC3$, the current is in CCM. Figure 16(a) and (b) shows the key waveforms of the switch voltage ($V$ds), input inductor current $IL4$, and output diode current $ID2$ for both operation modes, i.e., CCM and DCM, respectively. Figure 17 shows the transient response of the converter for astep change of load from 50% to 100%. As can be observed, afast dynamic response is obtained. Figure 18 shows the measured efficiency of the converter for a range of loads and three different input voltages. It can be observed from the figure that the efficiency of the converter is above 85% for higher loads.



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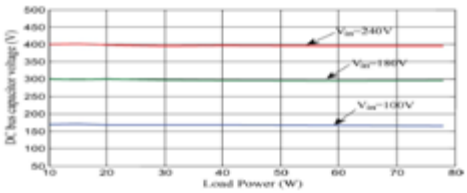


Figure 18.**DC** bus capacitor voltage *VC*1 versus load power for different inputvoltages.

Figure 18 shows the measured dc bus capacitor voltage *VC*1 fora range of load and input voltage variations. It can be seen that the capacitor voltage can be maintained below 450 V by properly designing the number of turns (*n*1, *n*3, and *n*5) and the inductors ratio (*k*).Finally, Table I summarizes the comparison of several singlestage ac/dc converters presented in [13]–[15], [19], [21], [25], and [32] with the proposed converter in terms of circuit implementation and performance. The main advantage of the proposed converter over the topologies presented in Table I is that the proposed converter presents a high-quality CCM input current with the lowest THD = 22%. Usually, in a single-stage converter, there is always a tradeoff between the CCM operation and THD of the line current, where, by the CCM operation, it usually causes high harmonic current. Furthermore, in all of the published approaches listed in the table, increasing the turns ratio of *Nau*/*Npc*an reduce the input PF by inducing a dead angle in the line current, whereas in the proposed converter, the higher the turns ratio *n*3/*n*1 is, the higher is the PF. However, the turns ratio cannot be arbitrarily large because of the maximum limit of the dc bus capacitor voltage. The maximum dc bus capacitor stress is *VC*1 = 400 V for the proposed converter, and it can be maintained always below 450 V by properly selecting the number of turns (*n*1, *n*3, and *n*5) and the inductors ratio *Lm*/*L*4. Although the dc bus voltage stress in the circuits presented in [14], [15], [19], [21], and [25] is lower than 400 V, those solutions penalized the current qualitywith high THD. The proposed converter can also be designed to achieve a dc bus voltage stress which is lower than 400 V,but the THD of the input current will increase slightly due toa small dead angle in the input current waveform. Therefore ,the design parameters are optimized to maintain a low THDwithout any dead angle and tolimit the capacitor voltage stress below 450 V.In addition, the proposed converter achieves ahighefficiency (>82%) due to the DPT paths provided by thetwo auxiliary windings.conversion efficiency in [15] and[21] is almost.similar to the proposed converter. Nevertheless,their harmonic currents are considerably higher, and they alsorequire a variable frequency control.

## 4. Conclusion

In this paper, a new quasi-active PFC circuit has been presented.In the proposed scheme, auxiliary windings are addedto the transformer of a dc/dc DCM flyback converter. Sincethe dc/dc converter is operated at high switching frequency, theauxiliary windings produce a high-frequency pulsating source such that the input current conduction angle is lengthened and the input current harmonics is reduced. The input inductor can operate in DCM+CCM. The single-stage PFC circuit has high efficiency when it operates in CCM. Hence, by properly designing the converter parameters, a high efficiency can be obtained while maintaining the total current harmonic content well below the IEC 61000-3-2 Class D standard specifications. The operating principles, analysis, and experimental results ofthe proposed method have been presented.

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