Power Reduction in TPG Based Built- in Self-Test (BIST) using LP/BS-LFSR on FPGA

Annie Chandra. D[1],Thatchayani. K[2]
[1]Department of VLSI, ,Arasu Engineering College, Kumbakonam
[2]Assistant professor, Department of ECE,Arasu Engineering College, Kumbakonam
Tamil Nadu-612501, India

Abstract: **- In this paper presents a test pattern generator which is most suitable for built in self test (BIST) structure. A modified linear feedback shift register (LFSR) proposed which targets to reduce the power consumption during the test pattern generation . The main objective of BIST is to reduce power dissipation without affecting the fault coverage. It reduces the power consumption in circuit under test. LP/BS-LFSR makes the counter is going to reduce the average and peak power and reduces the switching transition . The experiments results applied in the ISCAS'89 and LP-LFSR is implemented in VHDL and Spartran 3E.power has been analysed in Xpower analyzer.From the experimental results ,the proposed method consumes reduced testing power by a significant percentage.**

Keywords: Linear Feedback shift register, low power, bit swapping

I. INTRODUCTION

Power dissipation is a challenging problem in today's system on chip(soc) design and test . In general power dissipation of a system test mode is more than in normal mode .This is because a significant correlation exists between the cosecutive test vectors applied during the circuits normal mode of operation,where as this may not be necessarily true for applied test vector in test mode of opertion .low correlation between test vector switching actvity and eventually leads to power dissipation in the circuit.In VLSI circuits,BIST are used for testin.The main objective of Built in Self Test(BIST) is to reduce the power dissipation without affecting the fault coverage[1].

BIST and LFSR are very most essential method for testing process and it is necessary for process the test sequence.BIST is usually executed at system clock rate and its execution typically results in considerably high circuit activity. BIST is activated when the device fully packaged ,then the consumption of power may overflow the device package limits,this problem is even more critical when testing system –on-chip(SOC)[6].

Then BIST uses the LFSR as test pattern generator (TPG).TPG consist of low power test patterns that reduces the number of transitions at the input of the circuit under test using bit swapping technique and to synthesize is done to extract power.Furthermore the pseudorandom behavior of the LFSR correlation among test vectors.The increased switching activity in the CUT this often causes more power dissipation in test mode of operation.There are sevearl reasons for this power increased in test mode.

1.To test large circuit

2.Due to the lack of at speed availabity

3.Delay is introduced in the circuit

II. PROLOGUE

Low power consumption has become increasingly important in hand held communication systems and battery operated equipment,such as laptop computers, audio and video-based multimedia products and cellular phones. For this new class of battery-powered devices, the energy consumption has a critical design concern since it determines the lifetime of the batteries[7]. The increased power may be responsible for cost,reliability, performance verification. modified LFSR having a large scope to achive the low power test mode operation although in normal mode of switching activity.Many low power testing technique have been proposed and discussed can be founded in[2].

To reduces power and energy BIST technique is based on a modified clock scheme for the TPG and clock tree feeding the TPG.Then test-per-clock scheme has been proposed in[3].The power dissipation during test mode is 200% more than in normal mode[4].The Dual-speed LFSR is to reduce the switching activity in circuit.This method used two types of speed LFSRs to control the inputs that have been elevat transition[5].

In this paper a modified LFSR are used in which reducing number of transition of test pattern .The paper is organized as follows: ,section 3 describes the bakground and related work ,section 4 motivation ,section 5 having proposed work and section 6 explains experimental results.

III. BACKGROUND AND RELATED WORK

Modeling of power

There are basically two types of power models acheived, average power and peak power in the circuits.

Average power consumption is given by the ratio of energy and test time and reliability problems may be produced by large amount of power consumption

The evalutaion of power consumption of CMOS circuits are dafined below .

$$E_i=1/2V_{dd}^2C_0F_iS_i \quad (1)$$

Where V_{dd} is the supply voltage ,$C_0$is the load capacitance.The product of $F_i$and S_i is called weighated switching activity of internal circuit node i.

The average power consumption of internal circuit node i can be given by,

$$P_i =1/2V_{dd}^2C_0F_iS_if \quad (2)$$

F is the clock frequncy.the p_i node is named as average power consumption. It can be obtain from the (1) and (2) the power is mainly depends on the switching transition[4].

Peak power as a percentage of the total operating time.The power is that two to three times of their normal output ratings. Peak power onsumption is to the highest switching activity generated in the CUT during one clock cycle.

IV. MOTIVATION

Motivation of this proposed work arises from the earlier work observation.Literature focuses on the test stimuli and the test stimuli sequences from the LFSR.

The aim of this paper has to design minimaized power dissipation while producing the test stimuli sequence from the LFSR.The proposing work cause the low switching activity in scan chain method.

V. PROPOSED METHODOLOGY

In the proposed approach,an LFSR act as the LP-LFSR that produces the modified test vectors to minimize the switching activity and consumes less power as compared to the normal LFSR .For low power BIST circuit partitioning suitable method to reducing the power.This approch consists in partitioning the original circuit into structral subcircuits so that each sub-circuits can be successively tested through different BIST sessions. The above figure1 shows the modified LFSRTPG.the idea behined the use of such a low power TPG is to reduce the number of transition on primary inputs at each clock cycle of the test session ,hence it reduces the total switching activity generated in the CUT.

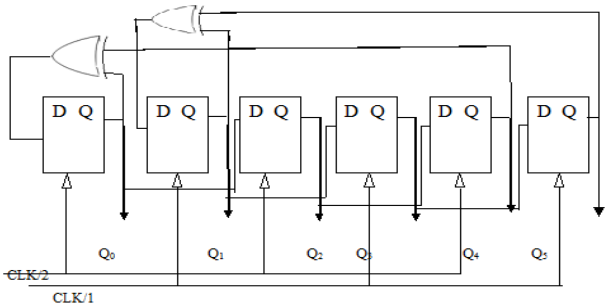

Figure 1 an example of modified LFSR TPG

The above TPG which described partitioning of CLK signal this reduce some amount of delay simultaneously increase the speed of the circuit which used in the proposed work.

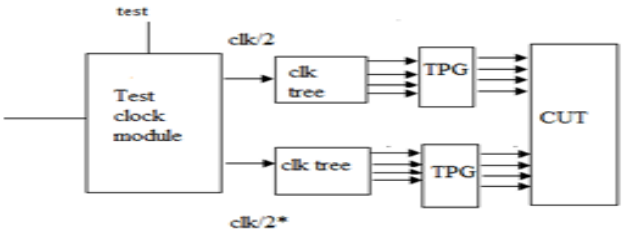

Figure 2 TPG structure

The TPG structure of this paper is depicted in fig2.The structure first composed of a test clock module which provide the clock signal to the two clock trees the signal "test" allows the switch transition from test mode to the normal mode. Then different speed of clock signals are needed to the TPG,two CLK signals used in their present work the TPG structure is finally connected to the CUT.

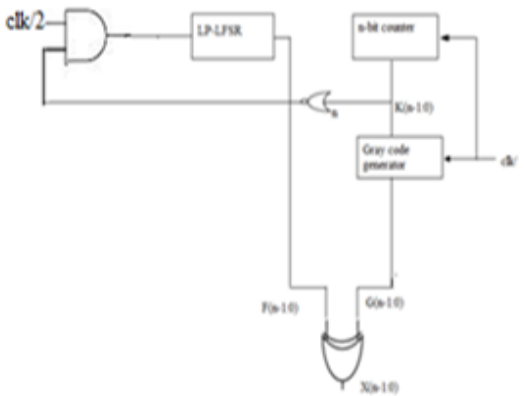

Figure 3 Low Power Test Pattern Generator

To simplify the circuit and achive less area occupation ,linear feedback shift register[LFSR] has used for generating the test patterns.in this proposed architecture consist by the LP-TPG with n-bit counter ,gray counter,NOR gate structure and XOR array.

The algorithm for low power LFSR is given below

- Consider a N-bit either external or internal linear feedback shift register (LFSR) [n>2]

- For example n-bit ,external LFSR is taken, which consists of n-flip flop in series. Acommon clock signal is partitioned and applied to the all flip flop ,act as control signal.
- If the last stage of flipflop output is one, any one of the flip flop output is swpped with its adjacent flip flop output value.
- If the last stage flip flop output is zero,no swapping will be carried out.
- Gray code generator modifies the counter output such that two successive value of its output are differing in only one bit.gray coverters can be implemented as shown below.

g [n-1]=k[n-1]
g[n-2]=k[n-1] XOR k[n-2]
.
.
.
g[2]=k[2] XOR k[3]
g[1]=k[1] XOR k[2]
g[0]=k[0] XOR k[1]

The proposed structure of test patterns generated can be implemented from the following equation.

x[0]=f[0] XOR g[0]

x[1]=f[1] XOR g[1]

x[n-1]=f[n-1] XOR g[n-1]

The XOR result of the sequences is single input changing sequence.It reduces the switching activitty ,then the power dissipation is very less compared with the normal LFSR.The gray code generator changs the counter output,gray code output is following below,

g0=000

g1=001

g2=011

g3=010

g4=110

g5=111

g6=101

g7=100

The n-bit counter is intialized with zeros and it generates test pattern sequence in the two set i.e disscused below

Fibonacci series starting with 1,each new number in the seriesis simply the sum of the two before it.so take "1" and add it to the previous number "0" and get next number as "1".then 1+1=2 etc.eventually the sequence of numbers that look like this 0,1,1,2,3,5,8...

Galois field the elements of galois field gf(p^n) is defined as

Gf(p^n)=(0,1,2,...,p-1)U

(p,p+1,p+2,...,p+p-1)U

(p^2,p^{2+1},p^{2+2},...,p^2+p-1)U...U

(p^{n-1},p^{n-1}+1,p^{n-1}+2,...,p^{n-1}+p-1)

The order of the field is given by p^n while p is called the characteristic of the field.gf stands for Galois field. It is particularly useful in translating computer data as the represented in binary forms.

VI. EXPERIMENTS AND ANALYSIS

In order to analyze the power reduction from the proposed TPG architecture ,we have evaluated the power consumption in bit range from upto 80 with the modified clock scheme.xilinx 11.1platform was used to perform synthesize opertion and it produces the RTL view of LP LFSR control unit in fig 5.Total power consumptiion were calculated by the Xpower analyzer. table 1, shows that the results.Modelsim SE6.2 has been used for simulation results. Modelsim SE6.2 produces the simulation for the modified LFSR i.e. shown in the figure 4. This simulation producing the test pattern generation for 80 bits .

Table 1 comparision of power consumption

Parameter	Normal LFSR	LP/LFSR
Slices	176	105
Flipflop(FF)	173	167
Frequency(MHz)	393.55	143.441
Toggle rate(%)	-	12.5
Power dissipation(mW)	80.65	80.18

Table 2 power consumption of testbench circuits

Parameter	S5378	S1512	S13207
Clock	10	9	10
Logic elements	188	118	155
Signals	241	152	206
I/Os	10	10	10
Power dissipation (mW)	80.98	80.98	80.98
Toggle rate (%)	12.5	12.5	12.5

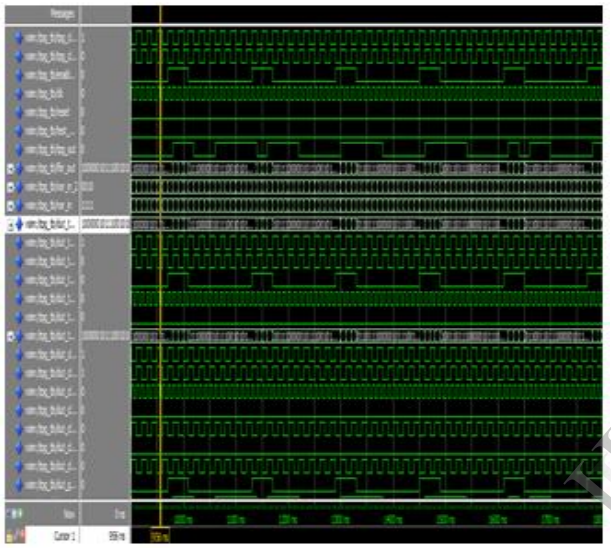

Figure 4 simulation results

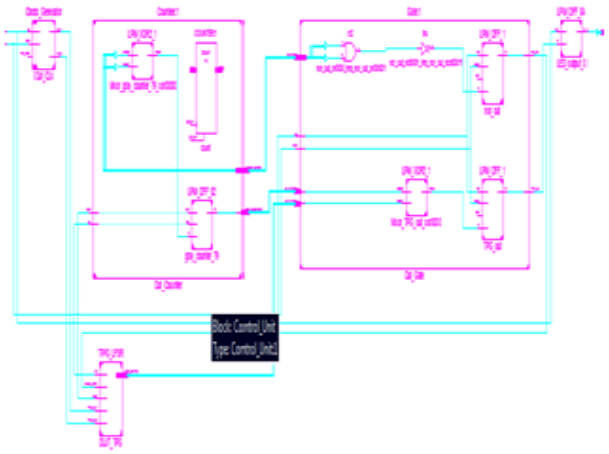

Fig 5 RTL view of LP LFSR control unit

VII. CONCLUSION

A low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR).The test pattern generated from the LP-LFSR is EX-Ored single input changing sequence generated from the gray code generator , which reduces the switching activities. Thus ,the proposed method reduces the power dissipation during the test mode with minimum switching activity using LP/BS-LFSR instead of normal LFSR. It is concluded that low power LFSR is very much useful for power consumption.

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