Power Quality Enhancement of Modified Multilevel Inverter with Minimum Number of Switches

Praveen Pateriya PG scholar / Dept. of EE Samrat Ashok Technological Institute Vidisha, Madhya Pradesh, India

Shivendra Singh Thakur Assistant Professor / Dept. of EE Samrat Ashok Technological Institute Vidisha, Madhya Pradesh, India

S. P. Phulambrikar Associate Professor & HOD/ Dept. of EE Samrat Ashok Technological Institute Vidisha, Madhya Pradesh, India

Abstract— This paper presents the design and implementation of modified nine level inverter for improving the power quality with less number of switches. We focus here two methods, first is Cascaded H-Bridge multilevel inverter topology and second is modified inverter topology. In both methods pulse generator is used for generating suitable switching pulses. The modified topology output quality is better as compared to Cascaded H-Bridge multilevel inverter. In the modified topology, when the levels are increased then less number of switches are required compared to cascaded Hbridge inverter. Hence it reduces initial cost and circuit's complexity, also applicable for industrial applications. Working of the modified topology is explained and finally results are analyzed by MATLAB/SIMULINK software.

Keywords—Multilevel Inverter, Total Harmonic Distortion (THD), MATLAB, pulse generator, Insulated Gate Bipolar Transister (IGBT).

1 INTRODUCTION

Inverter is a power electronic converter that converts dc power into ac power at desired output voltage and frequency. Block diagram of inverter is shown in fig.1. Single phase fullbridge inverter that gives three level output voltage square waveform. Overall performance of the inverter does not meet the industrial requirements. Hence multilevel inverters are emerged.

For obtaining nearest to sinusoidal waveform we focus on multilevel inverter. The advantages of the multilevel inverters are good power quality, low switching losses and higher voltage capability.

Multilevel inverter not only achieves higher power rating but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind and fuel cell can be easily interfaced to a multilevel inverter

First I would like to thanks my Prof. S.P. Phulambikar (HOD) and my guide Prof. S.S. Thakur for his valuable guidance and motivation.

I would like to thanks my friends Vijaya Raju Vasipalli, Ashok Patel and Vikalp Kulshrestha for their innovating ideas

Especially I would like to thanks to Mr. Sagar sir, who opened Lab always for me.

a high power application. [1]

system for



Fig. 1. Basic diagram of inverter

Some domestic and industrial applications of multilevel inverters are such as adjustable-speed ac drives, induction heating, stand by air-craft power supplies, uninterrupted power supplies (UPS) for computers etc.[3]-[4].

Two topologies are discussed here these are Cascaded H-Bridge multilevel inverter topology and modified multilevel topology.

In both topologies IGBT switches are used, these switches have higher switching frequency and low conduction losses.

In nine level Cascaded H-Bridge inverter topology, four single phase full bridge inverters are connected in series. That requires 16 IGBT switches and four separate dc voltage sources. For increasing voltage level number of switches are increased. Hence the voltage stresses and switching losses will increase and circuit will become more complex [6] [7]. By using modified topology number of switches are reduced hence power quality and efficiency will enhancement.

TRADITIONAL INVERTER 2

The power in the battery is in DC mode but AC motors require AC power, therefore conversion from DC to AC by a power converter is required. Hence inverter can do this conversion.

A. Three level inverter

In single phase full-bridge inverter or three level inverter have four switches and single DC voltage source is required. This is explained with the help of fig. 2.



Fig. 2. Three level inverter

In three level inverter zero level is added with two level inverter. The output voltage waveform is similar to the two level inverter [2]. The output voltage waveform is shown in fig. 3.



Fig. 3. Output voltage of three level inverter

B. Gate Signal and Inverter Operation

The output voltage level; $+V_{dc}$, zero and $-V_{dc}$.

In $+V_{dc}$ output voltage level, switch S1 and S2 are ON and remaining switches are OFF.

In Zero output voltage level, either S1 and S2 switches are ON or S3 and S4 switches are ON.

In $-V_{dc}$ output voltage level, switch S3 and S4 are ON and remaining switches are OFF. The switching scheme for three level inverter is shown in the table1.

Switching state	S1	S2	S 3	S4	V _{out}
1	On	On	Off	Off	+Vdc
0	Off	On	On	Off	Zero
-1	Off	Off	On	On	-Vdc

TABLE 1 The switching scheme for Three Level Inverter



From the figure 4 THD analysis of Traditional three level inverter output voltage waveform is 26.20%.

3. CASCADED H-BRIDGE MULTILEVEL INVERTER

When two or more single phase full bridge inverters are connected in series, that is known as Cascaded H-Bridge Multilevel inverter. Cascaded H-Bridge Multilevel inverter is two types:- (a) Symmetrical and (b) Asymmetrical Cascaded H-Bridge multilevel inverter.

Application of the Cascaded H-Bridge Multilevel Inverter are static-var generation, photovoltaic and fuel cells power conversion, uninterruptible power supplies, an interface with renewable energy sources and battery-based application [4].

In this topology, each single phase full bridge inverter need separate dc voltage source (SDCS). Each H-Bridge inverter can generate three different output voltage levels; positive, negative or zero voltage level. The final AC output voltage is the sum of all H-bridge inverter voltage.



Fig. 5. Cascaded H-Bridge 9-level Inverter

The main advantage of cascaded H-Bridge multilevel inverter to other topology {Neutral point clamped (NPC) or Diode clamped, and Capacitor clamped or Flying capacitor (FC)} are simple control system and module structure, so it becomes first choice for higher voltage application.

For study and comparison of nine level inverter is considered here; it requires 16 IGBT switches and 4 dc voltage sources. The power circuit of cascaded H-Bridge 9-level inverter is shown in figure 5.

The AC output voltage $V_{out} = V1+V2+V3+V4$. are obtained.



Fig. 6. Cascaded H-Bridge 9-level Inverter switching pattern

The other advantage of Cascaded H-Bridge inverter, it needs less number of components comparative to the Diode clamped or Flying capacitor topology, so that the price and weight of the inverter is less compare to these type inverter. The switching pattern of the Cascaded H-Bridge inverter can be explained with the help of fig. 6.



Fig. 7. Output voltage, speed, torque and main winding current of Cascaded H-Bridge with Induction motor load

In this topology, the number of output phase voltage levels in a Cascaded H-Bridge inverter is:- 2P+1, where P is the number of separate dc voltage source. The Cascaded H-Bridge inverter Output voltage and single phase induction motor speed, torque, and main winding current is explained in fig. 7.

The number of switches is reduced by using modified topology.

4. MODIFIED NINE LEVEL INVETER TOPOLOGY

The main objective of this topology is to generate nearly sinusoidal output ac voltage waveform with improved power quality of multilevel inverter and reduced number of switches.



Fig. 8. Modified 9-level Inverter

In modified 9 level inverter is considered; it requires 8 IGBT switches and 4 dc voltage source. The power circuit of modified inverter is shown in fig. 8. Inverter performance is obscured by connecting single phase Induction motor load in fig 10.

A. Gate Signal and Inverter Operation

The operation of modified 9-level inverter:-

For positive half cycle

- For V_{dc} output voltage level circuit allow is; first V1 dc voltage source, switches S1, load, S4 & S5 and back to the V1 dc source.
- For 2V_{dc} output voltage level circuit allow is; V1 & V2 dc voltage sources, switches S1, load, S4 & S6 and back to the V2 dc voltage source.
- For 3V_{dc} output voltage level circuit allow is; V1, V2 & V3 dc voltage sources, switches S1, load, S4 & S7 and back to the V3 dc source.
- In 4V_{dc} output voltage level circuit allow is; V1, V2, V3 & V4 dc voltage sources, switches S1, load, S4 & S8 and back to the V4 or lower dc source.

But in the negative half cycle, switches S1 and S4 are replaced by S2 and S3 respectively. The switching pattern can be explained in figure 9.



Fig. 9. Proposed 9-level Inverter switching pattern

TABLE 2. INDUCTION MOTOR PARAMETERS



Fig. 10. Output voltage, speed, torque and main winding current characteristics of modified topology with single phase induction motor load

5 COMPARISION STUDY

The modified inverter topology not only decreases the number of switches and also it has required lower ON - state switches in each level. We know that ON - state switches are representative of voltage drops. Therefore the voltage drop in the output waveform will be less.

Inverter type	9 level Cascaded H-Bridge inverter	9 level modified multilevel inverter	
Number of switches	16	8	
THD in output voltage	20.44%	9.52%	
Electromagnetic torque	(+17 to -17)N*m	(+10 to -10)N*m	
Main winding current	(+15 to -15)Amp.	(10 to -10)Amp	

TABLE 3. Comparison between Conventional and proposed MLI



Fig. 11. Harmonic spectrum of output voltage of nine level H-Bridge inverter



Fig. 12. Harmonic spectrum of output voltage of nine level modified inverter

6 CONCLUSSION

The simulation of the Nine level multilevel inverter is successfully done using pulse generator technique for the modified inverter topology and Cascaded H-Bridge inverter. Simulation result have shown modified inverter topology, generates nearly sinusoidal output voltage and current, lower switching losses, high performance torque regulation and significant reduction in torque ripple.

REFERENCES

- J.S.Lai and F.Z.Peng, "Multilevel Converters _A new Breed of Power Converter" IEEE Trans. Ind. Application, vol. 32, pp. 509-517, may/june 1996.
- [2] K.Gobinath, S.Mahendran and Dr. I. Gnanambal, "Novel Cascaded H-Bridge Multilevel inverter with Harmonics Eliminaation" Green High Performance Computing (ICGHPC), IEEE Internal conference on march 14-15, 2013.
- [3] Muhammad H. Rashid, Power Electronics circuits, devices, and applications, 2004 by pearson education Inc.
- [4] Dr. P. S. Bimbhra, power electronics, 2012 by Khanna Publishers.
- [5] Faetefilho, leon M.Tolbert, Yue cao and BurakOzpinineci, (sept./oct. 2011) "Real-time Selective Harmonic minimization for multilevel inverters connected to solar panels using Artificial Neural Network angle Generation" IEEE Trans. Ind. Applications, vol. 47, no. 5, pp2117-2124.
- [6] Hossein sepahvand, Jingsheng Liao and Mehdi Ferdowsi,(nov. 2011) "Investigation on Capacitor voltage regulation in Cascaded H-Bridge Multilevel converters with fundamental frequency switching", IEEE Transaction on industrial electronics,vol. 58, no. 11, pp 5102-5111.
- [7] Jason R. Wells, XinGengPatrick L. chapman Philip T. Kreinand Brett M. Nee, (jan. 2007) "Modulation-Baxed Harmonic Elimination", IEEE Transaction on power electronics, vol. 22, no. 1, pp336-340.