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Power Quality Enhancement by using Multi Converter Unified Power Quality Conditioner

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***Abstract*— In power system, generating station is connected with the loads through long transmission and distribution line. In this network, the power quality issues are not new, but the electric utilities are becoming aware of these quality problems. The quality of electric power is degraded due to increase in use of electronic loads like microprocessor based systems, which are nonlinear in nature which is much sensitive to the electric power quality. Power quality issues like voltage swell, sag, interruptions, harmonic current and voltage harmonics are becoming a serious challenge to the utilities. The current harmonics results into several problems like, increase in losses of the power system, over heating of conductor, burden of reactive power, malfunctioning of relays, poor power factor. The voltage and current harmonics, voltage swell and voltage sag are mitigated by using the combination of shunt active power filter and series active power filter (APF). In this paper, multi converter unified power quality conditioner (MC-UPQC) and its control algorithm is developed by simulation. The proposed configuration is simulated in PSCAD/EMTDC on a two-bus/two-feeder.**

Keywords—Power quality, APF, MC-UPQC, voltage swell, voltage sag

I. INTRODUCTION

Power quality is one of the major challenges in modern power systems. It may cause several problems such as malfunction, instabilities, short lifetime, and so on. Therefore it is required not only to identify the power quality problems but also to mitigate power quality disturbances. Transients are one of the power quality problems usually experienced by power system equipment. For power quality issues Active Power Filters (APFs) are preferred which are being dynamic and fast, over passive filters to compensate. Series APF mainly compensates for supply voltage related power quality problems such as voltage sag, swell and harmonics. On other hand, shunt APF mainly compensates for load current related power quality issues such as poor power factor, unbalance, and harmonics. UPQC is a combination of back to back connected series and shunt APFs sharing a common DC link capacitor. UPQC, integrating benefits of both series and shunt APF, compensates for most power quality issues.

In this paper, multi converter configurations for PQ improvement in adjacent feeders are discussed. For example, the interline unified power-quality conditioner (IUPQC), which is the extension of the IPFC concept at the distribution level, has been proposed in [1]. The IUPQC consists of one series and one shunt converter. It is connected between two feeders to regulate the bus voltage of one of the feeders, while regulating the voltage across a sensitive load in the other feeder. In this configuration, the voltage regulation in one of the feeders is performed by the shunt-VSC. However, since the source impedance is very low, a high amount of current would be needed to boost the bus voltage in case of a voltage sag/swell which is not feasible. It also has low dynamic performance because the dc-link capacitor voltage is not regulated.

In the following discussion, the multi converter unified power quality conditioner (MC-UPQC) is covered for multi feeders. In MC-UPQC third converter is added to support dc bus. The third converter is connected either series or parallel with feeder. It can control and manage flow of real power between multi feeders. The proposed topology can be used for simultaneous compensation of voltage and current imperfections in both feeders by sharing power compensation capabilities between two adjacent feeders which are not connected. The system is also capable of compensating for interruptions without the need for a battery storage system and consequently without storage capacity limitations.

II. CONFIGURATION OF MC-UPQC SYSTEM

A. Circuit Configuration

The proposed single line diagram for MC-UPQC in multi feeder system is shown in Fig.1. As shown in the above figure, two feeders connected to two different substations supply the loads L1 and L2.

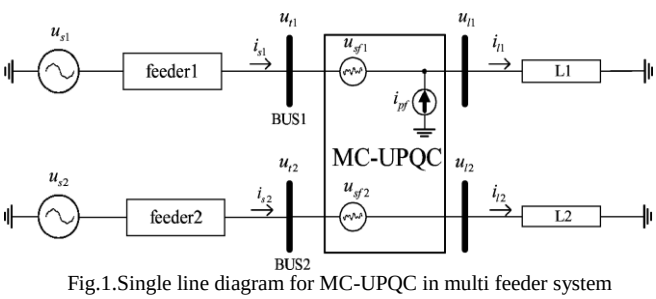

Fig.1.Single line diagram for MC-UPQC in multi feeder system

The MC-UPQC is connected to two buses BUS1 and BUS2 with voltages of U_{t1} *and* U_{t2}, respectively. The shunt part of the MC-UPQC is also connected to load L1 with a current of i_{l1}. Supply voltages are denoted by U_{s1} *and* U_{s2} and while load voltages are U_{l1} *and* U_{l2}. Finally, feeder currents are denoted by i_{s1} *and* i_{s2} and load currents are i_{l1} and i_{l2}. Bus voltages U_{t1} *and* U_{t2} are distorted and may be subjected to sag/swell. The load L1 is a nonlinear/sensitive

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load which needs a pure sinusoidal voltage for proper operation while its current is non-sinusoidal and contains harmonics. The load L2 is a sensitive/critical load which needs a purely sinusoidal voltage and must be fully protected against distortion, sag/swell, and interruption. These types of loads primarily include production industries and critical service providers, such as medical centers, airports, or broadcasting centers where voltage interruption can result in severe economic losses or human damages.

B. MC–UPQC Structure

The internal structure of the MC–UPQC is shown in Fig.2. It consists of three VSCs (VSC1, VSC2, and VSC3) which are connected back to back through a common dc-link capacitor. In the proposed configuration, VSC1 is connected in series with BUS1 and VSC2 is connected in parallel with load L1 at the end of Feeder1. VSC3 is connected in series with BUS2 at the Feeder2 end. Each of the three VSCs in Fig. 2 is realized by a three-phase converter with a commutation reactor and high-pass output filter. The commutation reactor and high pass output filter are connected to prevent the flow of switching harmonics into the power supply.

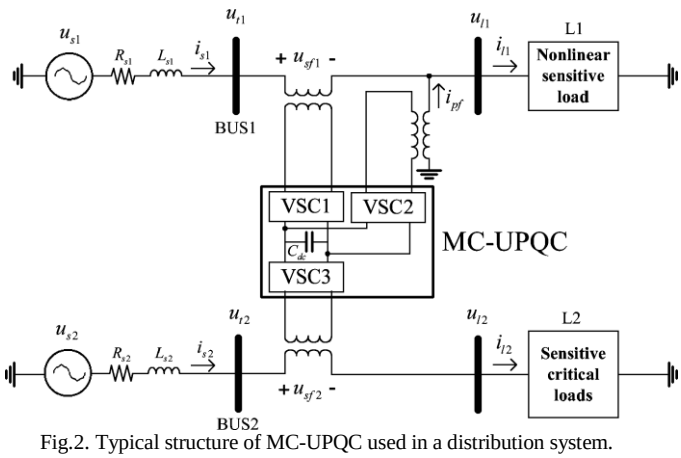

Fig.2. Typical structure of MC-UPQC used in a distribution system.

As shown in Fig. 2, all converters are supplied from a common dc-link capacitor and connected to the distribution system through a transformer. Secondary (distribution) sides of the series-connected transformers are directly connected in
series with BUS1 and BUS2, and the secondary (distribution)
side of the shunt-connected transformer is connected in parallel with load L1. The aims of the MC-UPQC shown in Fig. 2 are:

1) to regulate the load voltage against sag/swell and disturbances in the system to protect the nonlinear/sensitive load L1;

2) to regulate the load voltage against sag/swell, interruption, and disturbances in the system to protect the sensitive/critical load L2;

3) to compensate for the reactive and harmonic components
of nonlinear load current.

In order to achieve the above goals, series VSCs (i.e., VSC1 and VSC3) operate as voltage controllers while the shunt VSC (i.e.,VSC2) operates as a current controller.

C. Control Strategy for Shunt and Series VSC Converters

The switching control strategy for series VSCs and the shunt VSC are selected to be sinusoidal pulse width modulation (SPWM) voltage control and hysteresis current control, respectively. Details of the control algorithm, which are based on the method [2], will be discussed later.

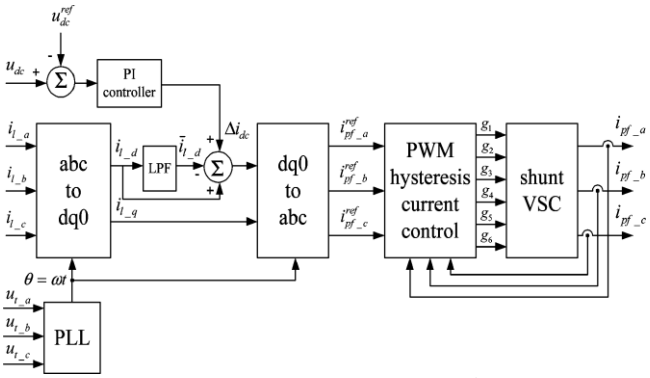

Fig. 3 PWM hysteresis current control block diagram for the shunt VSC

Shunt-VSC: Functions of the shunt-VSC are:
1) to compensate for the reactive component of load L1 current;
2) to compensate for the harmonic components of load L1 current;
3) to regulate the voltage of the common dc-link capacitor.
Fig. 3 shows the control block diagram for the shunt VSC. The measured load current (i_{l_abc}) is transformed into the synchronous reference frame (dq0).

By this transform, the fundamental positive-sequence component, which is transformed into dc quantities in the and
axes, can be easily extracted by low-pass filters (LPFs). Also, all harmonic components are transformed into ac quantities with a fundamental frequency shift.

Switching losses cause the dc-link capacitor voltage to decrease. Other disturbances, such as the sudden variation of load, can also affect the dc link. In order to regulate the dc-link capacitor voltage, a proportional–integral (PI) controller is used as shown in Fig. 4. The input of the PI controller is the error between the actual capacitor voltage and its reference value. By using PWM hysteresis current control, the output-compensating currents in each phase are obtained.

Series-VSC: Functions of the series VSCs in each feeder are:
1) to mitigate voltage sag and swell;
2) to compensate for voltage distortions, such as harmonics;
3) to compensate for interruptions (in Feeder2 only).

The control block diagram of each series VSC is shown in Fig.4. The bus voltage (U_{t_abc}) is detected and then transformed into the synchronous reference frame (dq0).

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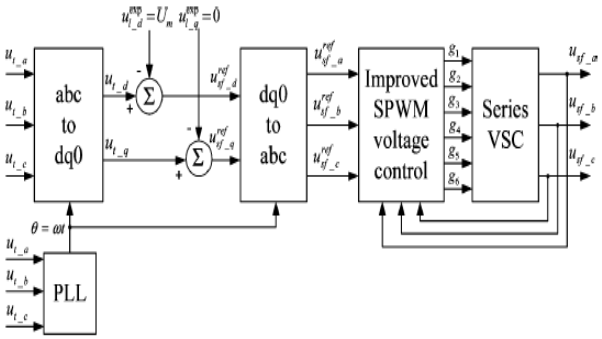

Fig. 4 Improved SPWM Voltage Control block diagram for the series VSC

U_{t1P}, U_{t1n}, U_{t1o} are fundamental frequency positive, negative and zero-sequence components, respectively, and is the harmonic component of the bus voltage.

According to control objectives of the MC-UPQC, the load voltage should be kept sinusoidal with a constant amplitude even if the bus voltage is disturbed. Therefore, the expected load voltage in the synchronous reference frame (dq0) only has one value.

By using an improved SPWM voltage control technique (sine PWM control with minor loop feedback)[3], the output compensation voltage of the series VSC can be obtained.

III ANALYSIS OF MC-UPQC

In MC-UPQC, the power rating is an important factor in terms of cost. The best model which requires the minimum power rating is considered by analyzing two models of UPQC. All voltage and current phasors used in this section are phase quantities at the fundamental frequency.

There are two models for a UPQC in which one is quadrature compensation (UPQC-Q) and another one is inphase compensation (UPQC-P). In the quadrature compensation scheme, the injected voltage by the series-VSC maintains a quadrature advance relationship with the supply current so that no real power is consumed by the series VSC at steady state. This is a significant advantage when UPQC mitigates sag conditions. The series VSC also shares the volt-ampere reactive (VAR) of the load along with the shunt-VSC.

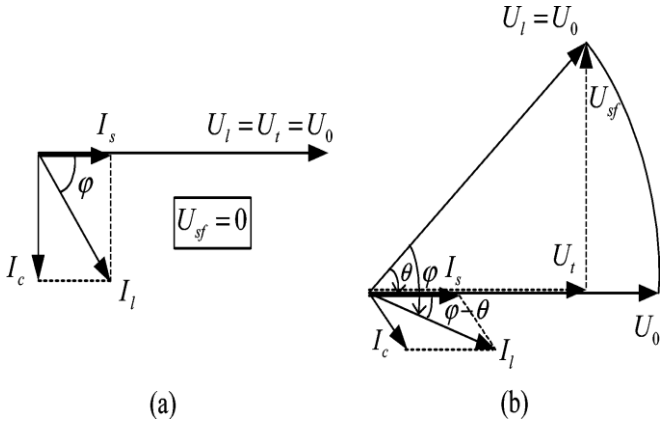

Fig.5. Phasor diagram of quadrature compensation. (a) Without voltage sag, (b) With voltage sag.

Fig. 5 shows the phasor diagram of this scheme under a typical load power factor condition with and without a voltage sag. When the bus voltage is at the desired value, the series-injected voltage is zero [Fig. 5(a)]. The shunt VSC injects the reactive component of load current , resulting in unity input-power factor.

Furthermore, the shunt VSC compensates for not only the reactive component, but also the harmonic components of the load current. For sag compensation in this model, the quadrature series voltage injection is needed as shown in Fig. 5(b). The shunt VSC injects in such a way that the active power requirement of the load is only drawn from the utility which results in a unity input-power factor.

In an inphase compensation scheme, the injected voltage is inphase with the supply voltage when the supply is balanced. By virtue of inphase injection, series VSC will mitigate the voltage sag condition by minimum injected voltage. The phasor diagram of Fig.6 explains the operation of this scheme in case of a voltage sag.

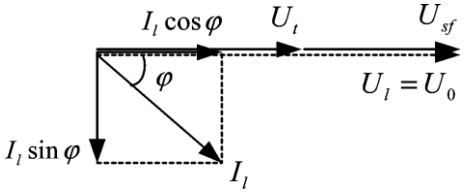

Fig.6. Phasor diagram of inphase compensation (supply voltage sag)

A comparison between inphase (UPQC-P) and quadrature (UPQC-Q) models is made for different sag conditions and load power factors in [4]. It is shown that the power rating of the shunt-VSC in the UPQC-Q model is lower than that of the UPQC-P, and the power rating of the series-VSC in the UPQC-P model is lower than that of the UPQC-Q for a power factor of less than or equal to 0.9. Also, it is shown that the total power rating of UPQC-Q is lower than that of UPQC-P where the VAR demand of the load is high.

As discussed in the above section, the power needed for interruption compensation in Feeder2 must be supplied through the shunt-VSC in Feeder1 and the series VSC in Feeder2. This implies that power ratings of these VSCs are greater than that of the series one in Feeder1. If quadrature compensation in Feeder1 and inphase compensation in Feeder2 are selected, then the power rating of the shunt VSC and the series VSC (in Feeder2) will be reduced. This is an important criterion for practical applications.

Based on the afore mentioned discussion, the power-rating calculation for the MC-UPQC is carried out on the basis of the linear load at the fundamental frequency. The parameters in Fig.5 are corrected by adding suffix “1,” indicating Feeder1, and the parameters in Fig. 6 are corrected by adding suffix “2,” indicating Feeder2. As shown in Figs. 5 and 6, load voltages in both feeders are kept constant at regardless of bus voltages variation, and

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the load currents in both feeders are assumed to be constant at their rated values (i.e., and , respectively).

The load power factors in Feeder1 and Feeder2 are assumed and the per-unit sags, which must be compensated in Feeder1 and Feeder2, are supposed to be and, respectively.

If the MC-UPQC is lossless, the active power demand supplied by Feeder1 consists of two parts:
1) the active power demand of load in Feeder1;
2) the active power demand for sag and interruption compensation in Feeder2.

III SIMULATION RESULTS

In this section, the proposed MC-UPQC and its control schemes have been tested through extensive case study simulations using PSCAD/EMTDC. The obtained simulation results are presented, and the performance of the proposed MC-UPQC system is shown.

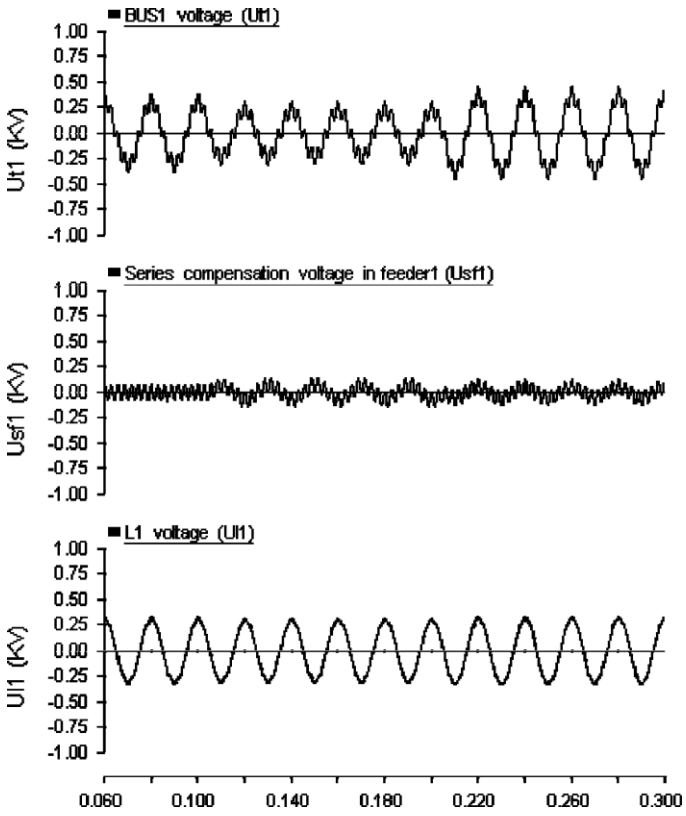

Fig.7. BUS1 voltage, series compensating voltage, and load voltage in Feeder1

A. Voltage Distortion and Sag/Swell on the Bus Voltage

Let us consider that the power system in Fig.2 consists of two three-phase three-wire 380(v)(rms, L-L), 50Hz utilities. The BUS1 voltage (U_{t1}) contains the seventh-order harmonic with a value of 22%, and the BUS2 voltage(U_{t2}) contains the fifth order harmonic with a value of 35%. The BUS1 voltage contains 25% sag between 0.1s < t < 0.2s and 20% swell between 0.2s < t < 0.3s. The BUS2 voltage contains 35% sag between 0.15s < t < 0.25s and 30% swell between 0.25s < t < 0.35s. The nonlinear/sensitive load L1 is a three-phase rectifier load which supplies an RC load of 10Ω and 30 μF. Finally, the critical load L2 contains a balanced RL load of 10 Ω and 100mH.

The MC–UPQC is switched on at 0.02 s. The BUS1 voltage, the corresponding compensation voltage injected by VSC1, and finally load L1 voltage are shown in Fig.7. In all figures, only the phase waveform is shown for simplicity. Similarly, the BUS2 voltage, the corresponding compensation voltage injected by VSC3, and finally, the load L2 voltage are shown in Fig. 8. As shown in these figures, distorted voltages of BUS1 and BUS2 are satisfactorily compensated for across the loads L1 and L2 with very good dynamic response.

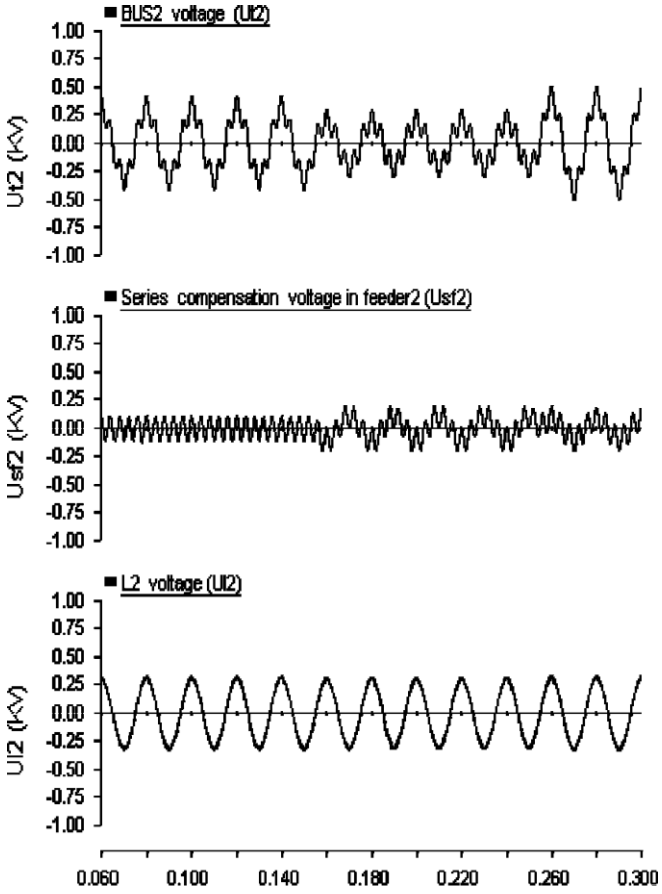

Fig.8. BUS2 voltage, series compensating voltage, and load voltage in Feeder2

The nonlinear load current, its corresponding compensation current injected by VSC2, compensated Feeder1 current, and, finally, the dc-link capacitor voltage are shown in Fig.9. The distorted nonlinear load current is compensated very well, and the total harmonic distortion (THD) of the feeder current is reduced from 28.5% to less than 5%. Also, the dc voltage regulation loop has functioned properly under all disturbances, such as sag/swell in both feeders.

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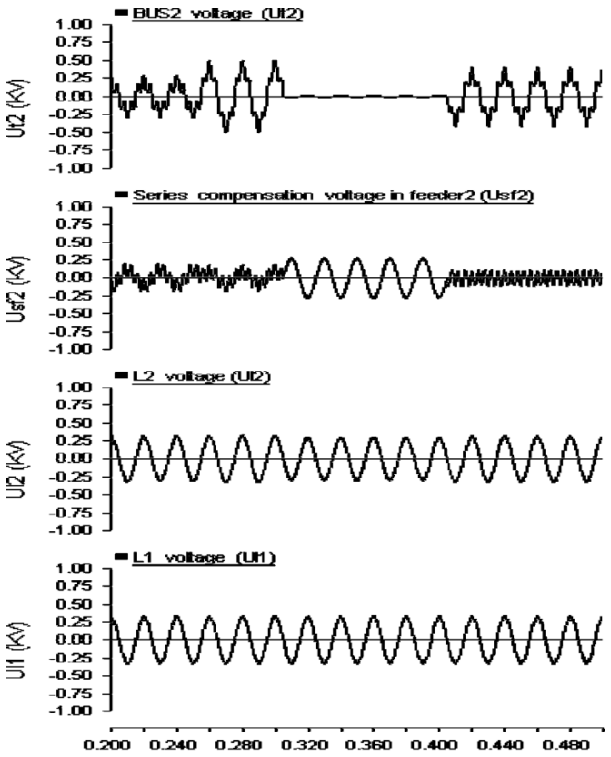

Fig.8. BUS2 voltage, series compensating voltage, and load voltages in Feeder2

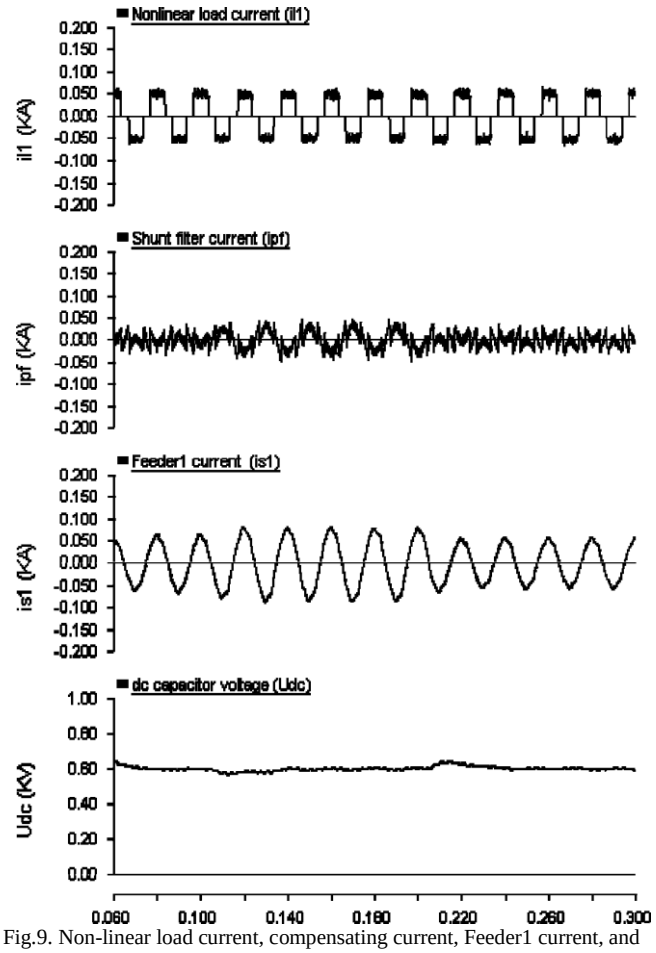

Fig.9. Non-linear load current, compensating current, Feeder1 current, and capacitor voltage

B. Upstream Fault on Feeder2

When a fault occurs in Feeder2 (in any form of L-G, L-L-G and L-L-L-G faults), the voltage across the sensitive/critical load L2 is involved in sag/swell or interruption. This voltage imperfection can be compensated for by VSC2. In this case, the power required by load L2 is supplied through VSC2 and VSC3. This implies that the power semiconductor switches of VSC2 and VSC3 must be rated such that total power transfer is possible. This may increase the cost of the device, but the benefit that may be obtained can offset the expense. In the proposed configuration, the sensitive/critical load on Feeder2 is fully protected against distortion, sag/swell, and interruption.

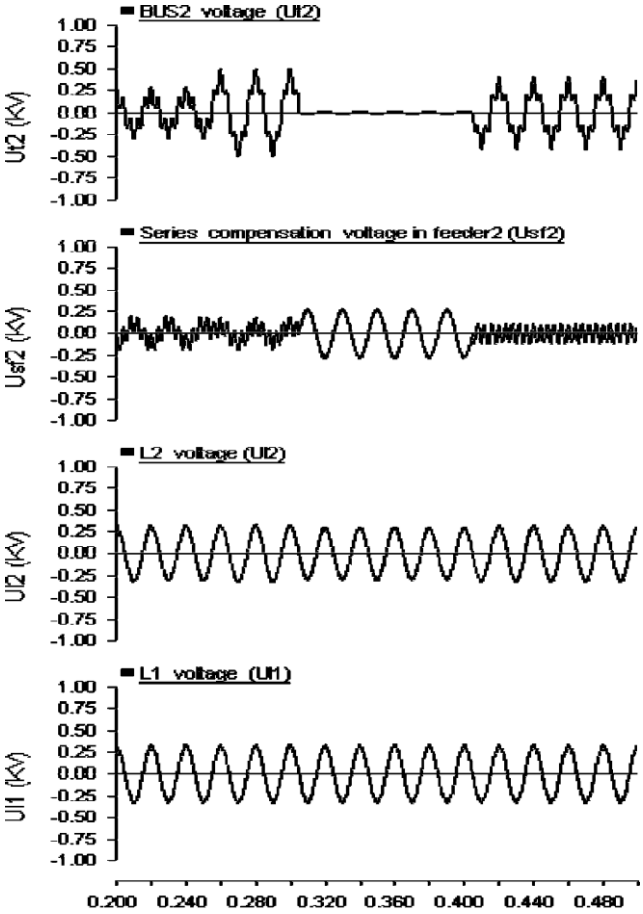

Fig.10. Simulation results for an upstream fault on Feeder2: BUS2 voltage, compensating voltage, and loads L2 and L1 voltages

Furthermore, the regulated voltage across the sensitive load on Feeder1 can supply several customers who are also protected against distortion, sag/swell, and momentary interruption. Therefore, the cost of the MC-UPQC must be balanced against the cost of interruption, based on reliability indices, such as the customer average interruption duration index (CAIDI) and customer average interruption frequency index (CAIFI). It is expected that the MC-UPQC cost can be recovered in a few years by charging higher tariffs for the protected lines. The performance of the MC-UPQC under a fault condition on Feeder2 is tested by applying a three-phase fault to ground

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on Feeder2 between 0.3s<t<0.4s. Simulation results are shown in Fig.10.

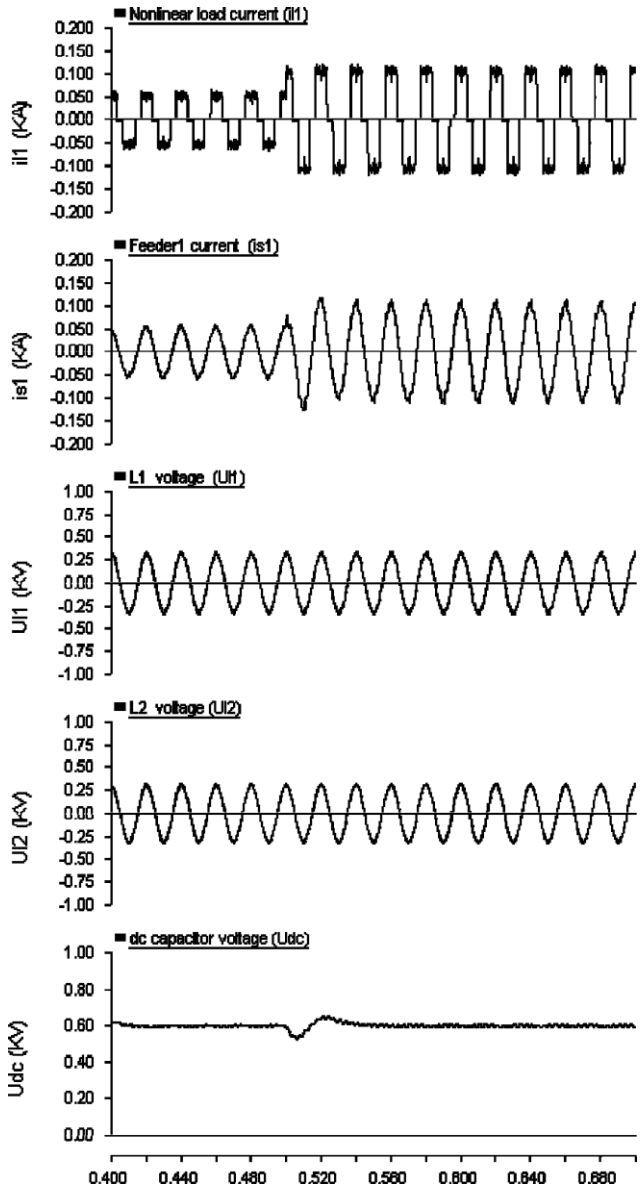

Fig.11. Simulation results for load change: nonlinear load current, Feeder1 current, load L1 voltage, load L2 voltage, and dc-link capacitor voltage

C. Load Change

The system behavior during a load change is evaluated by the nonlinear load L1 is doubled by reducing its resistance to half at 0.5 s whereas the other load is kept unchanged. The system response is shown in Fig.11. It can be seen that as load L1 changes, the load voltages and remain undisturbed, the dc bus voltage is regulated, and the nonlinear load current is compensated.

D. Unbalance Voltage

The control strategies for shunt and series VSCs, which are introduced in Section II, are based on the d-q method. They are capable of compensating for the unbalanced source voltage and unbalanced load current. To evaluate the control system capability for unbalanced voltage compensation, a new simulation is performed. In this new simulation, the BUS2 voltage and the harmonic components of BUS1 voltage are similar to those given in Section IV. However, the fundamental component of the BUS1 voltage is an unbalanced three-phase voltage with an unbalance factor of 40%. The simulation results for the three-phase BUS1 voltage, series compensation voltage, and load voltage in feeder 1 are shown in Fig.12. The simulation results show that the harmonic components and unbalance of BUS1 voltage are compensated for by injecting the proper series voltage. In this figure, the load voltage is a three-phase sinusoidal balance voltage with regulated amplitude.

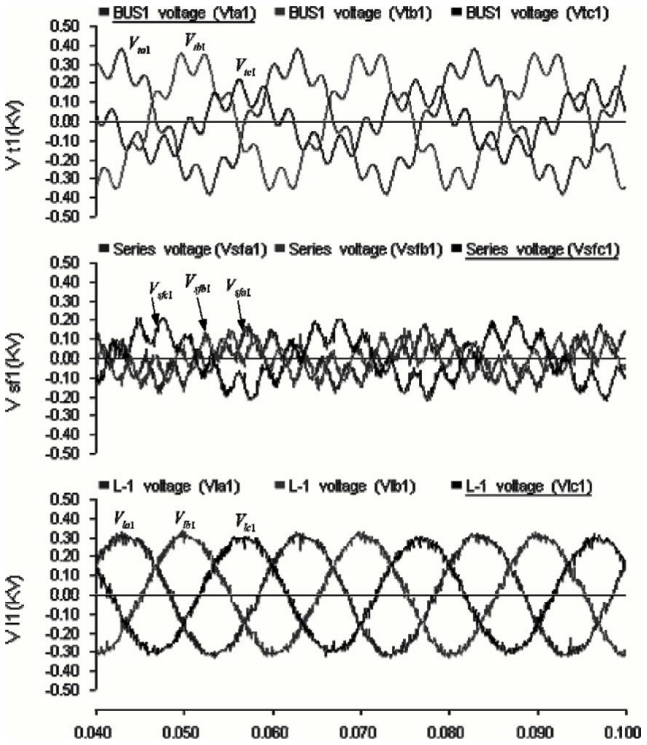

Fig.12. BUS1 voltage, series compensating voltage, and load voltage in Feeder1 under unbalanced source voltage

V CONCLUSION

The paper is focused on a MC-UPQC configuration for simultaneous compensation of voltage and current in adjacent feeders. The proposed topology is compared with conventional topology which is capable of fully protecting critical and sensitive loads against distortions, sags/swell, and interruption in two-feeder systems. The same idea can be theoretically extended to multibus/multifeeder systems by adding more series VSCs. The performance of the MC-UPQC is evaluated under various disturbance conditions and it is shown that the proposed MC-UPQC offers the following advantages:

1) power transfer between two adjacent feeders for sag/swell and interruption compensation;

2) compensation for interruptions without the need for a battery storage system and, consequently, without storage capacity
limitation;

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3) sharing power compensation capabilities between two adjacent feeders which are not connected.

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