Power Optimized Reversible Sequence Generator

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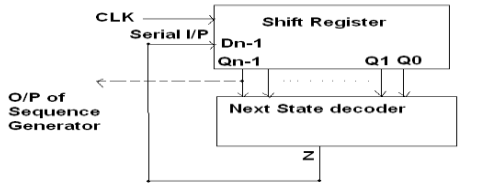
***Abstract* - Low power consumption has emerged as a principle theme for almost every category of design. Due to population growth, economic expansion & urban development, the demand for portable battery powered mobile devices, appliances & services in communication system are increasing rapidly. These appliances require low power circuits. As increased power consumption may be responsible for cost, reliability, performance verification & technology related problems. Reversible logic is thus becoming an important figure of merit in today's modern era due to their ability to build circuits with zero internal power dissipation. It has wide range of applications in several emerging technologies such as low power CMOS design, quantum computing, advanced computing & Nano technology. Recently several researchers have proposed optimized design & synthesis of various reversible sequential logic circuits. Here I introduce a novel design of reversible logic based sequence generator. The motivation to design reversible logic based sequence generator is its wide application in cryptography & constitute a novel design in complex reversible sequential logic circuits.**

Keywords: Reversible logic, Sequence generator, sequential circuits, low power consumption

1. INTRODUCTION

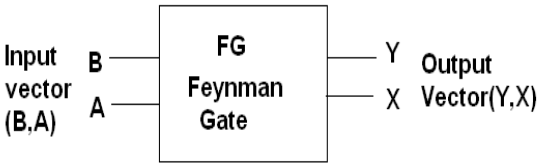
Sequence Generator is a circuit that generates a desired sequence of bits in synchronization with a clock. The sequence generator can be constructed using shift register and a next state decoder. The output of next state decoder (Z) is a function of Qn-1, Qn-2,……Q1,Q0 and is connected to the serial input of the shift register



Block Diagram of a Sequence Generator

Any logic circuit based on Irreversible hardware results in energy dissipation due to information loss. For example: Two input EX-OR gate with Input vector (A, B) and output vector(Y).It transforms two input bits into a single output bit i.e. one bit is lost leading to power dissipation. Even we can't derive inputs from output, For example if we get 1 at output, we can't predict that input vector taken is (1, 0) or (0, 1).Compression of states from 2:1, there is decrease of entropy of hardware and it leads to dissipation of energy. Research has already proposed for: Feynman gate most well known as reversible (2, 2) logic gate, Toffoli gate popular as (3, 3) reversible logic gate, Fredkin gate etc.These gates are used as a part of reversible logic based circuits instead of AND, OR, XOR gates used by conventional irreversible logic based circuits. Here we design sequence generator based on reversible (2, 2) Feynman gate, reversible (3, 3) Toffoli gate.

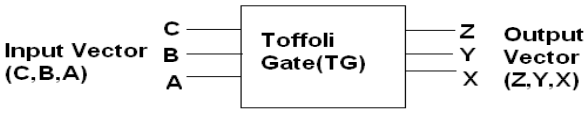
Take a (2, 2) Feynman gate as shown in Fig: 2. This gate implements logic function as Y=B, X=A XOR B



Truth table:-

B	A	Y	X
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

If we put A=0, then Y=B, X=B and Feynman gate acts as a copying gate. Similarly if we put A=1, Then Y=B, X= Bar (B) and Feynman gate acts as a not gate. Now take a (3, 3) Toffoli gate as shown below in Fig: 3. This gate implements logic function as Z=C, Y=B, X= A XOR CB



Truth table:-

C	B	A	Z	Y	X
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

If we put A=1, then $X=\overline{BC}$ .Hence Toffoli gate acts as a NAND gate.

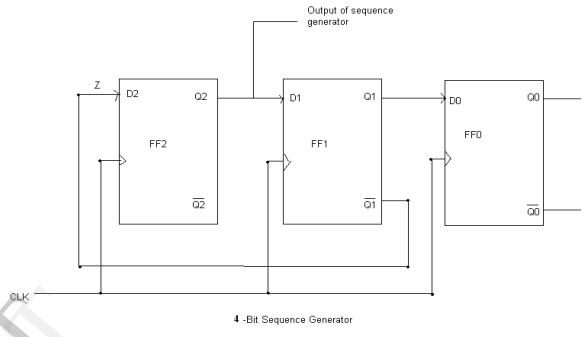
2. LITERATURE REVIEW

Power consumption has become one of the most important issues in contemporary digital circuit design .For decades now electronic industry has been able to produce devices that are smaller, faster & use less power years after year. Now the world is facing phenomenal growth of demand for energy and power consumption is a major concern today .On 13 April 2005, Gordon Moore stated in an interview that the law cannot be sustained indefinitely: "It can't continue forever. Your job is to delay forever by minimizing power consumption. An extremely new paradigm may provide the solution. The use of reversible logic in building chips may provide the solution.

In the current literature, lot of work has been found in the designing of reversible combinational circuits e.g. BCD adder, subtractor,Reversible ripple carry binary adder etc.Now a days many researchers found a new direction in the field of reversible sequential circuits such as work in Thapliyal et al. [2005], Chuang and Wang [2008] and Rice [2008].This work is mainly focused on latches & flip-flops & optimizing reversible sequential designs in terms of number of reversible gates, garbage outputs,ancilla inputs, quantum cost, delay .Optimization issues are mainly focused by Thapliyal et al.[2010].This work is further promoted & many other circuits are optimized such as shift registers[10],counters[1][4][5],barrel shifters[13] etc.

In this work, I introduce novel design of reversible logic based sequence generator. The motivation to design reversible logic based sequence generator is its wide application in cryptography & it also serves as an example of complex reversible sequential circuits.

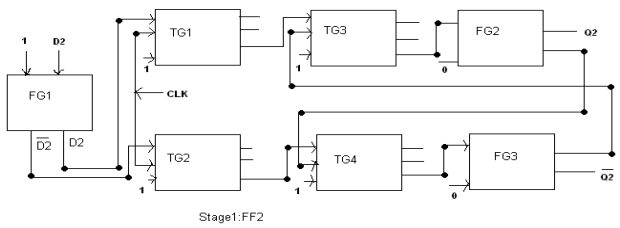
3. 4-BIT SEQUENCE GENERATOR BASED ON CONVENTIONAL IRREVERSIBLE (D FLIP-FLOP)



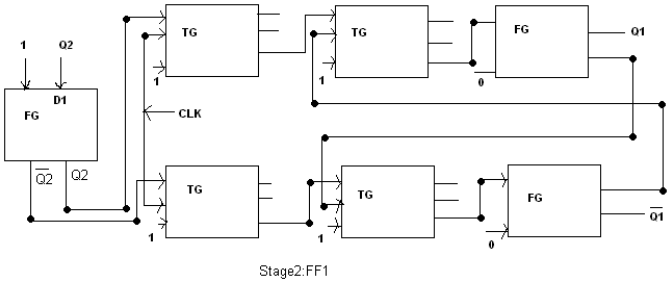
4. PROPOSED REVERSIBLE SEQUENCE GENERATOR

Complete design of sequence generator is divided into three stages. In the first stage FF2 (D Flip-Flop) is drawn by using **Feynman gate(FG)** acting as a **copying gate** & **NOT gate** and **Toffoli Gate(TG)** acting as a **NAND gate**. Here FG1is acting as a NOT gate and copying gate both and proving D2 & both.D2 is provided as input to TG1 acting as NAND gate & is provided to TG2 acting as another NAND gate. Similarly TG3 & TG4 are also NAND gates. Now Cross coupling of TG3 & TG4 is done with the help of Feynman gates (FG2 &FG3) as they support feedback.

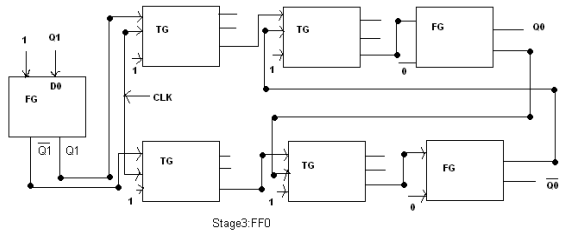
Stage 1



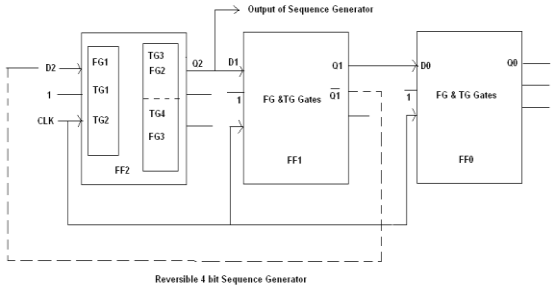
- Similarly in the second stage FF2 (D flip-Flop) is drawn via connecting output Q2 of first stage with D1 input of second stage.



- Then in the third stage FF1 (D Flip-Flop) is drawn via connecting output Q1 of Second stage with D0 input of third stage.



Hence cascading of three stages shown above leads to a reversible 4-bit Sequence Generator



5. CONCLUSION

Sequence generator is proved by various researchers with different low power architectures & they focused on increasing the through put rate as well as reducing the power dissipation. But every conventional sequence generator is based on irreversible logic.

In this work I present a novel design of reversible logic based sequence generator which is optimum in terms of power dissipation. So avoiding power dissipation will be the main objective of study & that will add on a novel efficient design in complex reversible sequential circuits. Conventional sequence generator will be optimized by novel designed reversible logic based sequence generator in terms of power consumption then further different designs will be made to optimize reversible logic based sequence generator in terms of quantum cost,delay,garbage outputs & ancilla inputs

REFERENCES

1. Gupta, Shubham, Vishal Pareek, and S. C. Jain. "Low Cost Design of Sequential Reversible Counters." *International Journal of Scientific & Engineering Research* 4.11 (2013): 1234-1240.
2. Singla, Pradeep, et al. "An Optimized Design of Reversible Sequential Digital Circuits." *arXiv preprint arXiv:1306.2556* (2013).
3. NG, Mr Sandesh, and Mr Manojkumar SB. "Design and Synthesis of Sequential Circuit Using Reversible Logic." *International Journal of Innovative Research and Development (ISSN 2278–0211)* 2.6 (2013).
4. Ramprasd, K., R. Sudheer Kumar, and G. Srikanth. "A Novel Approach for Design and Verification of 4-Bit Asynchronous Counter Using Reversible Logic Gates." Internat ional Journal of Computational Engineering Research,vol 03,issue,6:16-21,June2013
5. Banu, Tehniat, and Manjunath Kounte. "Performance Analysis of Irreversible and Reversible Counter." HCTL Open Science and Technology Letters, Edition on Recongurable Computing - Embedded, FPGA based, VLSI and ASIC Designs, June 2013, e-ISSN: 2321-6980, ISBN (Print): 978-1-62776-963-1
6. Niknafs, Aliakbar, and Majid Mohammadi. "Synthesis and optimization of multiple-valued combinational and sequential reversible circuits with don't cares." *Integration, the VLSI Journal* 46.2 (2013): 189-196.
7. Al Mamun, Md Selim, and David Menville. "Quantum Cost Optimization for Reversible Sequential Circuit." *Quantum* 4.12 (2013).
8. Thapliyal, Himanshu, and Nagarajan Ranganathan. "Design, Synthesis and Test of Reversible Circuits for Emerging Nanotechnologies." *VLSI (ISVLSI), 2012 IEEE Computer Society Annual Symposium on*. IEEE, 2012.
9. Drechsler, Rolf, and Robert Wille. "Reversible circuits: Recent accomplishments and future challenges for an emerging technology." *Progress in VLSI Design and Test*. Springer Berlin Heidelberg, 2012. 383-392.
10. Krishnaveni, D., and M. Geetha Priya. "A Novel Design of Reversible Universal Shift Register with Reduced Delay and Quantum Cost." *Journal of Computing* 4.2 (2012): 164-173.
11. Feinstein, D.Y.; Thornton, M.A. "Using the Asynchronous Paradigm for Reversible Sequential Circuit Implementation", *Multiple-Valued Logic (ISMVL), 2012 42nd IEEE International Symposium on*, On page(s): 305 – 310
12. Soeken, M.; Wille, R.; Otterstedt, C.; Drechsler, R. "A Synthesis Flow for Sequential Reversible Circuits", *Multiple-Valued Logic (ISMVL), 2012 42nd IEEE International Symposium on*, On page(s): 299 – 304
13. Kotiyal, S.; Thapliyal, H.; Ranganathan, N. "Design of a reversible bidirectional barrel shifter", *Nanotechnology (IEEE-NANO), 2011 11th IEEE Conference on*, On page(s): 463 – 468
14. Nagapavani, T.; Rajmohan, V.; Rajendaran, P. "Optimized shift register design using reversible logic", *Electronics Computer Technology (ICECT), 2011 3rd International Conference on*, On page(s): 236 - 239 Volume: 2, 8-10 April 2011
15. Rajmohan, V.; Ranganathan, V. "Design of counters using reversible logic", *Electronics Computer Technology (ICECT), 2011 3rd International Conference on*, On page(s): 138 - 142 Volume: 5, 8-10 April 2011
16. Drechsler, R.; Wille, R. "From Truth Tables to Programming Languages: Progress in the Design of Reversible

Circuits", *Multiple-Valued Logic (ISMVL), 2011 41st IEEE International Symposium on*, On page(s): 78 – 85

17. Banerjee, Anindita. "Reversible cryptographic hardware with optimized quantum cost and delay." *India Conference (INDICON), 2010 Annual IEEE*. IEEE, 2010.
18. H. Thapliyal and N. Ranganathan, "Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay, and Garbage Outputs," ACM Journal on Emerging Technologies in Computing Systems, 2010.
19. Nayeem, Noor Muhammed, et al. "Efficient design of shift registers using reversible logic." *2009 International Conference on Signal Processing Systems*. IEEE, 2009.
20. Mohammadi, Majid, and Mohammad Eshghi. "On figures of merit in reversible and quantum logic designs." *Quantum Information Processing* 8.4 (2009): 297-318.
21. Chuang, Min-Lun, and Chun-Yao Wang. "Synthesis of reversible sequential elements." *ACM Journal on Emerging Technologies in Computing Systems (JETC)* 3.4 (2008): 4.
22. Rice, J. E. "An Analysis of Several Proposals for Reversible Latches." *Advances and Innovations in Systems, Computing Sciences and Software Engineering*. Springer Netherlands, 2007. 203-206.