Power Optimization Techniques at Circuit and Device Level in Digital CMOS VLSI – A Review

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***Abstract*—Since the invention of the first IC, designers have been looking for methods to speed up digital circuits and to reduce the area of their design. Recently, advances in VLSI fabrication technology have made it possible to put a complete System On a Chip. The penalty was that power dissipation became a critical parameter in digital VLSI design. This paper puts an insight into the various sources of power dissipation in digital CMOS and the power optimization techniques at circuit and device level.**

***Keywords*—lowpower, CMOS,power reduction,circuit,VLSI, device, leakage current, transistor stacking,dynamic power, static power, short circuit power, variable threshold, variable supply, clock gating.**

I. INTRODUCTION

Power dissipation is defined as the rate of energy delivered from source to system. In the past, major concern of VLSI designers were performance and miniaturization. With the substantial growth in portable computing, power dissipation has become a major concern now. Costumers are expecting portable applications to have the same level of performance as their non-portable counter parts, without compromising battery lifetime. This results in an increase in chip density and operating frequency. Direct effect of an increase in power dissipation is an increase in temperature, which ultimately leads to a device breakdown, unless taken care of. Costly packaging and cooling arrangements are required to control the temperature, which further escalates the system cost. This paper discusses the different sources of power dissipation and the probable power reduction techniques at circuit and device level.

II. SOURCES OF POWER DISSIPATION

Average power dissipation [2],[12] in a CMOS digital circuit is given by the equation:

$$\mathbf{P_{avg} = P_{dynamic} + P_{static} + P_{short\ circuit}} \quad \textbf{(1)}$$

Where P_{avg} = average power dissipation, $P_{dynamic}$ = dynamic power dissipation, P_{static} = static power dissipation, $P_{short\ circuit}$ = short circuit power dissipation. The three sources of power dissipation are discussed briefly in the following section with the help of a basic CMOS inverter.

A. Dynamic power dissipation

Power dissipation during a switching event [1], when the output of the gate makes a logic transition; which results in charging and discharging of parasitic capacitances.

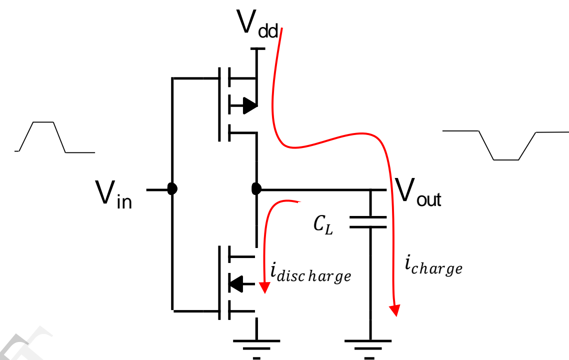

Fig. 1. Charging And Discharging Currents In Dynamic Power Dissipation

$$\mathbf{P_{dynamic} = \alpha C_L V_{dd}^2 f} \quad \textbf{(2)}$$

Where α- switching activity factor ;which is the effective number of power consuming voltage transitions experienced per clock cycle , C_L – load capacitance ; which is the sum of device capacitance and interconnect capacitance, V_{dd}– supply voltage, *f*- clock frequency.

B. Static power dissipation

Power dissipation due to the flow of leakage current when the transistors are in the quiescent condition. Static power dissipation is becoming comparable to dynamic switching power with the continuous scaling down of CMOS technology.There are three main components that constitute leakage current.

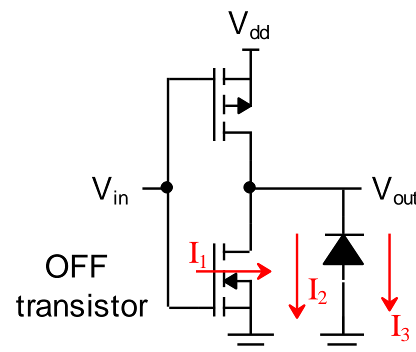

Fig. 2. Leakage currents in static power dissipation

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$$\mathbf{P_{static}= I_{leakage} V_{dd}} \qquad (3)$$

Where V_{dd} – supply voltage, $I_{leakage}$ – sum of all leakage currents (I1+I2+I3) explained below:

Reverse biased PN junction leakage

This leakage, I3 occurs when the pn-junction between the drain and bulk of the transistor is reverse biased. The reverse biased drain junction conducts a reverse saturation current which is drawn from the supply.In the case of an inverter with a high input voltage, the output voltage becomes '0' since the NMOS transistor is ON. The PMOS transistor is turned OFF but its drain to bulk voltage is equal to supply voltage (-V_{dd}). The resulting diode leakage current is given by the equation:

$$I_L = A_D J_S (e^{(qV_{bias}/kT)} - 1) \qquad (4)$$

Where A_D- area of drain diffusion, J_S- leakage current density, V_{bias} - reverse bias voltage across the junction.

Subthreshold leakage

Ideally, MOS transistor is said to be in the OFF condition for a $V_{gs}<V_t$. But practically, there is the existence of a weak inversion layer due to which current rolls down exponentially for $V_{gs}<V_t$. This constitutes the subthreshold leakage, I2as given by the equation:

$$\mathbf{I_{sub} = I_{sub0}\, e^{\frac{V_{gs}-V_t}{n\, v_T}} \left[1 - e^{\frac{-V_{ds}}{v_T}}\right]} \qquad (5)$$

$$\mathbf{I_{sub0} = \mu_0 C_{ox} \frac{W_{eff}}{L_{eff}} v_T^2 e^{1.8}}$$

Where μ_0 - zero bias electron mobility, n – subthresholdslope factor, Vgs - gate to source voltage, V_{ds} – drain-to-source voltage, v_T- thermal voltage, V_t- threshold voltage, C_{ox} –oxide capacitance per unit area,W_{eff} - effective channel width, $L_{eff} - eff$. Due to the exponential relation between $V_t$and I_{sub}, an increase in $V_t$sharply reduces the subthreshold current.

Gate oxide leakage

It is the oxide tunneling current,I1 which is due to reduction in oxide thickness and the consequent increase in electric field across the oxide.

C. Short circuit power dissipation

Power dissipation due to the existence of a direct current path between V_{dd} and ground.

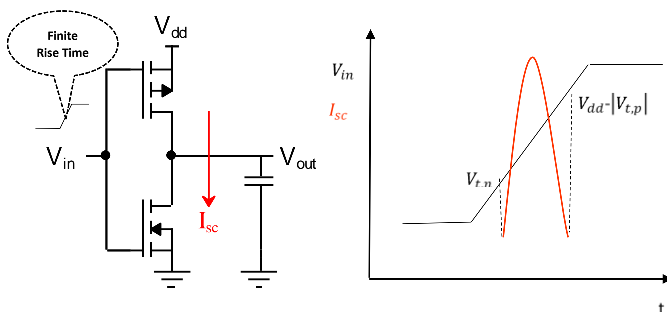

Fig. 1. Short circuit current in short circuit power dissipation

When a CMOS inverter is driven with an input voltage waveform having a finite rise and fall time, both NMOS and PMOS transistors in the circuit may conduct simultaneously for a short period of time($V_{t,n} < V_{in} < |V_{dd} - V_{t,p}|$) , forming a direct current path between $V_{dd}$and ground. The resulting short circuit power dissipation is given by the equation:

$$\mathbf{P_{short\ circuit}= I_{sc} V_{dd}} = \frac{\beta}{12}(V_{dd} - 2V_t)^3 \frac{\tau}{T} \qquad (6)$$

Where I_{sc}- short circuit current, V_{dd}- supply voltage, V_t-threshold voltage, β- gain factor of transistor, T- time period, τ- input transition time.Hence the average power dissipation can be expressed as:

$$P_{avg} = \alpha C_L V_{dd}^2 f + I_{leakage} V_{dd} + \frac{\beta}{12}(V_{dd} - 2V_t)^3 \qquad (7)$$

III. LEVELS OF ABSTRACTION

Power optimization can be achieved at various abstract levels.

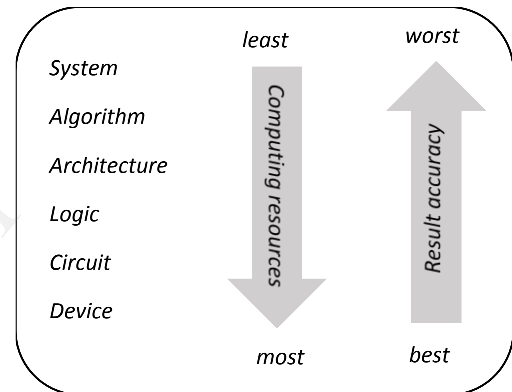

Fig. 4. Abstraction levels for power optimization

The main difference between power optimization at different levels of design abstraction is the trade-off between computing resources and accuracy of results. Even though System/Algorithm/Architecture level power optimization techniques have a large potential for power saving, these techniques tend to saturate as more functionality is integrated on the IC. Hence optimization at logic/circuit/device level is also very important for the miniaturization of IC. This paper focuses on circuit and device level power optimization techniques.

IV. POWER OPTIMIZATION TECHNIQUES

Various power optimization techniques at circuit and device level are discussed in the following section.

A. Dynamic power optimization

$$\mathbf{P_{dynamic} = \alpha C_L V_{dd}^2 f}$$

It is the most dominant component which contributes about 40-70 % of the total power. The viable dynamic power optimization techniques at circuit and device level are detailed below.

1) Supply voltage

Because of its quadratic relationship to power [4],voltage reduction offers the most effective means for minimizing power. Unfortunately, delay in the circuit increases

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drastically as V_{dd} reduces and approaches the threshold voltage ,V_t of the device. This affects the dynamic performance of the gate as given by the equations:

$$\tau_{PHL}=\frac{C_{load}}{k_n\ (V_{dd}-V_{t,n})}\left[\frac{2V_{t,n}}{V_{dd}-V_{t,n}}+\ln\left(\frac{4(V_{dd}-V_{t,n})}{V_{dd}}-1\right)\right] \qquad (8)$$

$$\tau_{PLH}=\frac{C_{load}}{k_p\ (V_{dd}-V_{t,p})}\left[\frac{2V_{t,p}}{V_{dd}-V_{t,p}}+\ln\left(\frac{4(V_{dd}-V_{t,p})}{V_{dd}}-1\right)\right] \qquad (9)$$

Where τ_{PHL}- high to low propagation delay, τ_{PLH}- low to high propagation delay, C_{load}- load capacitance, V_{dd}- supply voltage, $V_{t,n}$-NMOS threshold voltage, $V_{t,p}$- PMOS threshold voltage, k_n- $\mu_n C_{ox}\frac{W}{L}$, k_p- $\mu_p C_{ox}\frac{W}{L}$, μ_n- electron mobility,μ_p- hole mobility, C_{ox}- oxide capacitance, W-width of transistor, L- length of transistor.

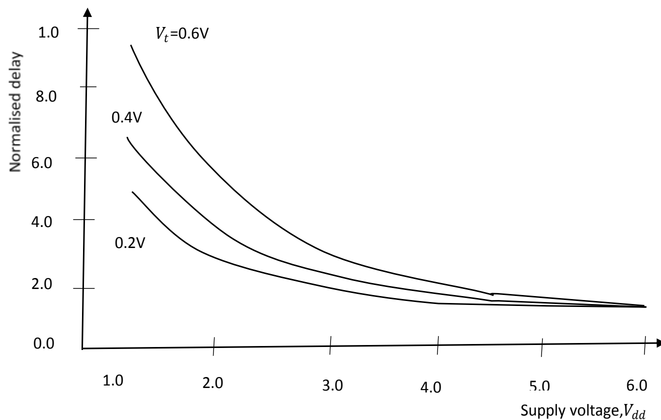

Fig. 5. Dependence Of Delay On Supply Voltage And Threshold Voltage

Creating **Voltage islands** is a solution for the problem. It is the concept of multi-supply voltages being used in different functional blocks of the core for saving power. High V_{dd} supplied to performance critical blocks and a low V_{dd} supplied to performance non critical blocks, creates a perfect balance between power and performance. This is accomplished by using level shifters.

Performance critical Blocks (High V_{dd})	Level shifter	Performance non-critical Blocks (Low V_{dd})

Fig. 6. Multi-supply voltage solution

2) Load Capacitance

Both device and interconnect capacitance contribute to parasitic load capacitance. Device capacitance can be reduced by proper transistor sizing [7]. But as the transistors are downsized, its current drive decreases and the performance is affected. A typical approach to the problem is to compute the **slack time**[13]at each gate in the circuit. Slack time of a gate is the difference between the signal's required time and its arrival time at the output of the gate. The gate sizes are adjusted such that the slack time of each gate is as low as possible without any gate, having a negative slack.Interconnect capacitance can be reduced by proper placement and routing.

3) Switching Activity Factor

In addition to voltage and load capacitance, switching activity also influences dynamic power dissipation. A chip may contain an enormous amount of load capacitance, but if there is no switching in the circuit, then no dynamic power will be consumed. Static logic family has an inherently low activity factor whereas dynamic circuit families have clocked nodes and a high activity factor. **Clock gating**[6]is a widely accepted technique in the industry which disables clock to idle portions of the chip, thereby avoiding power dissipation due to unnecessary charging and discharging of the unused circuit.

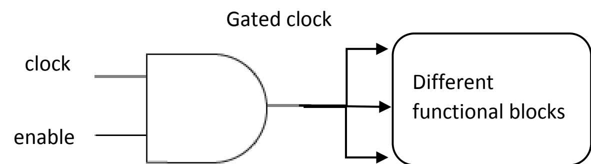

Fig. 7. Clock Gating

In clock gating, clock is selectively stopped for portions of circuit which are idle, by using an 'enable' signal.

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4) Frequency

Frequency [15] can also be traded for power. Frequency of operation can be reduced to reduce dynamic power, wherein the major concern is throughput and not frequency.

B. Static power optimization

$\mathbf{P_{static}= I_{leakage}V_{dd}}$

20-50% of the total power is contributed by this component [14]. The various design time and run time static power optimization techniques at circuit and device level are discussed here.

1) Variable Supply Voltage

Subthreshold leakage current from equation (5) can be reduced by reducing V_{dd}. But reduction in V_{dd} increases the delay as given by the equations (8),(9). V_{dd} reduction can be achieved without compromising performance by reducing V_t. Again from equation (5), $V_t$reduction results in an increase in sub threshold leakage current. Hence low V_{dd} and high V_t is best desirable for static power optimization. Going for variable supply voltage in different functional blocks is a viable option to strike a perfect balance between dynamic power optimization and static power optimization.

2) Variable Threshold Voltage

VTCMOS- Variable Threshold CMOS

In conventional CMOS logic circuits, substrate terminals of all NMOS transistors are connected to ground and that of PMOS are connected toV_{dd} so that threshold voltages of transistors are not influenced by **'body effect'**, as given by the equation :

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$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right) \qquad (10)$$

WhereV_t- threshold voltage, V_{t0}-threshold voltage when the source is at body potential, ϕ_s– surface potential at threshold,V_{sb}- potential difference between source and substrate/bulk.

In conventional approach,V_{sb} remains '0' and henceV_t= V_{t0}.In VTCMOS logic circuits[13], transistors are designed inherently with a low$V_t$and this$V_t$is varied by a substrate bias control circuit .

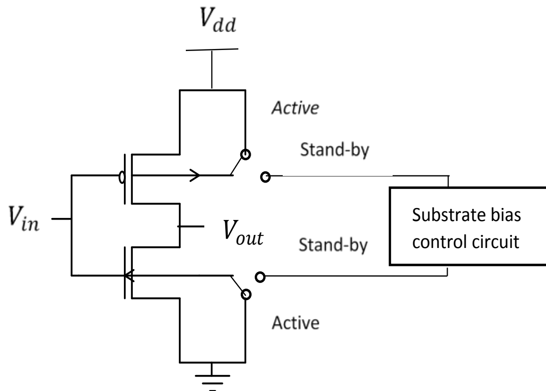

Fig. 8. Variable body biasing

In 'active mode', the above inverter circuit works as a conventional CMOS inverter with lowV_{dd} and lowV_t, thereby benefitting from low dynamic power dissipation and high switching speed. In 'stand-by mode', substrate bias control circuit generates a lower bias voltage for NMOS and a higher bias voltage for PMOS.This increases$V_t$of both the transistors as per the equation(10) and thereby reduces static power dissipation in stand-by mode.

MTCMOS- Multi Threshold CMOS

This technique [3][13] makes use of transistors working with two different threshold voltages in the circuit.

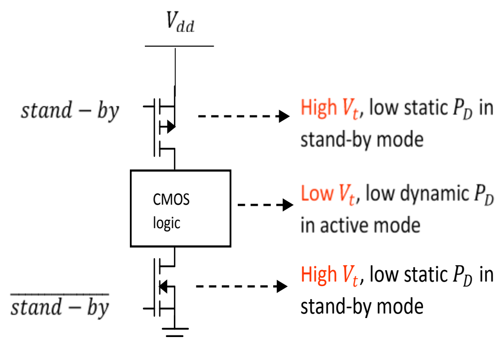

Fig. 9. MTCMOS technique

In the active mode, the high$V_t$transistors are turned onand the CMOS logic with low $V_t$operates with a low dynamic power dissipation and a high switching speed. In the stand-by mode, high$V_t$transistors are turned off and hence the possibility of a sub threshold leakage current from the CMOS logic circuitry is cut off. This brings down static power dissipation.

DTMOS- DynamicThreshold MOS

In DTMOS [16], gate and the body are tied together to dynamically alter the threshold voltage.

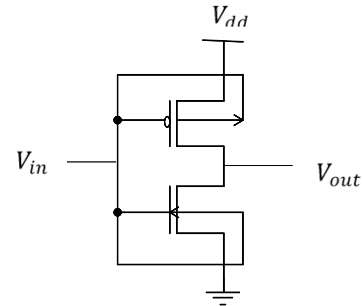

Fig. 10. DTMOS technique

Initially when the gate voltage is zero,$V_t$is maximum. As the gate voltage increases, the reverse voltageV_{sb} in equation(10) decreases and the threshold voltage drops.

3) Leakage prevention

HighC_{ox} is desirable for good transistors since there is an inverse relation betweenC_{ox} andV_t. As the gate oxide thickness approaches 15-20 A,tunneling current increases exponentially .

Hence the only option to maintain a high$C_{ox}$is to use a gate insulator with a high dielectric constant, like oxynitride, N_2O instead of SiO_2.

$$C_{ox} = \varepsilon \frac{A}{d}$$
(11)

WhereC_{ox} – oxide capacitance,ε-permittivity of insulating material, A- area of the junction, d- oxide thickness.

Reverse biased pn-junction leakage can be reduced by proper cooling arrangements since reverse leakage current decreases as the temperature drops.

4) Transistor stacking effect

Subthershold leakage current flowing through a stack ofseries connected transistors reduces when more than one transistor in the stack is turned off. This effect is known as the "**stacking effect**"[11],[10].

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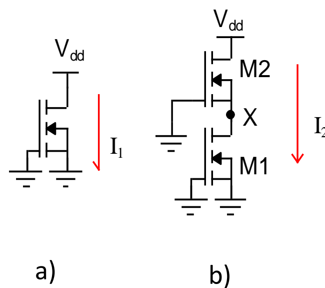

Fig. 11. Transistor stacking

In Fig. 11.a, the NMOS off-transistor has a low Vt because of Drain Induced Barrier Lowering(DIBL) from the high drain voltage. As a result, the subthreshold leakage current I1 is considerably high. In Fig. 11.b, two NMOS off-transistors are in series. Because of the leakage current in M2, point X rises to a small positive potential, much smaller thanV_{dd}. $V_t$of M2 is higher because of the small drain voltage, which decreases sub threshold leakage. M1 is also turned off hardly because of negative V_{gs} and body effect. The net result is that I2 is much smaller than I1.Hence static power dissipation can be reduced considerably by taking advantage of the stack effect, where in gates with series transistors are put into a sleep mode by turning them off.

C. Short circuit power optimization

$$P_{short\ circuit} = I_{sc} V_{dd}$$

5-10% of total power is contributed by short circuit power. Various reduction techniques are discussed below.

1) Keep the input rise/fall time less than or eual to output rise/fall time by proper transistor sizing.

If the load capacitance is very large [16], output fall time of an inverter becomes larger than input rise time and drain-source voltage of the PMOS transistor approximates tozero. This results in a zero short circuit power dissipation. If the load capacitance is very small, output fall time becomes smaller than input rise time and drain-source voltage of the PMOS transistor approximates toV_{dd}.This results in a very large short circuit power dissipation.

2) High threshold voltage

The dependency of short circuit power on V_t is given by the equation (6). Going for high V_t transistors [9] in the non-critical paths reduces the short circuit power dissipation by nearly 40 % without compromising dynamic and static power dissipations.

3) $V_{dd} < V_{t,n} + |V_{t,p}|$

If the supply voltage is reduced to below the sum of the threshold voltages of the transistors, short circuit current can be eliminated since both the transistors cannot be turned ON at the same time for any input voltage.

V. CONCLUSION

1) Design for low-power implies the ability to reduce all the three components of power consumption in CMOScircuits.This paper explains the various components of power dissipation in digital CMOS VLSI. Various power optimization techniques adopted by industry at circuit and device level are reviewed . Different techniques have different tradeoffsand hence their selection is as per the specification requirements. Future challenge in this field is to strike a perfect balance between power management, reduced transistor size and performance.

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