

Power Optimization and Power Reduction in RTL Design Using System Verilog Assertion and UVM Technology

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Abstract - Power dissipation has now turned into the most basic design limitation. In the design of a SoC, power calculation and examination for the most part comes into picture only after the completion of RTL synthesis. In any case, design optimization for low power is most reasonable before synthesis. After synthesis level the design becomes much more complicated which makes dynamic power targets harder to accomplish. Additionally, changes made later in the design for power optimization lead to cost consumption. It is good to pin point the issue or the bug which is related to power at the beginning itself when they can be still fixed. The methodology for power analysis which is used in this project can be implemented at RTL stage itself. The novel methodology is based on System Verilog assertions to optimize the consumed power of RTL designs.

The proposed technique will upgrade the RTL code towards accomplishing low power design. The design will be coded according to the specification and will be integrated into the UVM testbench. The simulation output of UVM testbench shows the mistaken signal, which can be further corrected and power enhancement can be done. The consumed power of the design is significantly reduced as it catches each unused design signal that consumes power.

Key Words: Power Optimization, UVM, System Verilog Assertion, RTL Design, FSM.

1. INTRODUCTION

With the enhanced growth of portable devices like laptops, and the evolution of shrinking technologies, research has inclined towards low power design methods. Recent application demands for low power implementation of the design. Coming up with the design that consumes more power becomes a real issue in the design of SoC chip and its design components. The designs of complex and high performance SoC has witnessed ground breaking revolution over the past two to three decades. Up to this point, designers were essentially worried about improving the presentation of the design and decreasing silicon area to reduce the production costs. In the current SoC chip design, the prime focus is to reduce power consumption. With the increasing growth of personal, wireless, and mobile communications, as well as home electronics:- comes the demand for high-speed computation and complex functionality for competitive reasons. Today's compact products, along with the expectation of exclusively small and light-weight, long battery life has also becomes an additional requirement. Because of these requirements of current day, designers need to think about every design aspect to reduce the leakage power at the Register Transfer Level itself.

The methodology which has been implemented will upgrade the RTL design code in accomplishing the low power design. As per the proposed procedure, a UVM test bench will be coded. For a design code will be written and incorporated into testbench. The simulation of the testbench represents mistakes in the code or bug in the code, which in turn can be utilized to rectify the design code; hence decreasing the power of the RTL design. This methodology helps in analyzing the entire design signals and reflects that this is a design dependent technique. This type of coding strategy decides the specific input and displays the mistakenly seeing signals which may consume additional power.

1.1 UVM Test bench Architecture

The UVM is a standard method for verifying IC (Integrated Circuit) designs. It has a library of classes that helps in designing and implementing modular testbench components and stimulus which enables re-using testbench components and stimulus within the project and across the projects.

The verification process can be improved by using pseudo-random verification instead of direct testing approach. The main question was how to make such transaction effective, and it is by adopting existing methodology that supports pseudo-random verification. It provides consistency and uniformity in the way verification components are developed, used and connected. So for a new learner who joins a team, the ramp up time will be reduced. Code reused – more the usage less bugs can be seen.

2. PROJECT FLOW

The project flow as depicted below describes the inputs from the logic code which refers to the RTL design code and its test bench.

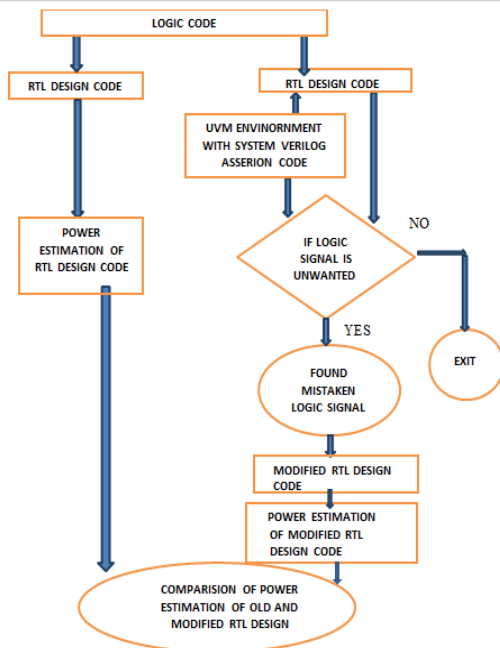


Figure-1: Flow of Methodology

The logic code is the RTL code of any sequential circuit. One part of the flow gives the picture of using UVM environment to the RTL design code, wherein verification is done at this level. The output simulation from UVM verification resultant shows which part of the design or which signal of the design is been affected to the RTL design. Due to mistakenly setting of the signal we can see some bugs in the simulation part. System Verilog assertion must catch these bugs in the logic part of the sequential design. To find the functional bug which is affecting the power consumption of the whole design, a system Verilog assertion is written in UVM environment test bench.

In the next phase of the other part of the project flow, we calculate the power consumption or estimation of the RTL code, before implementing the proposed methodology which is depicted below.

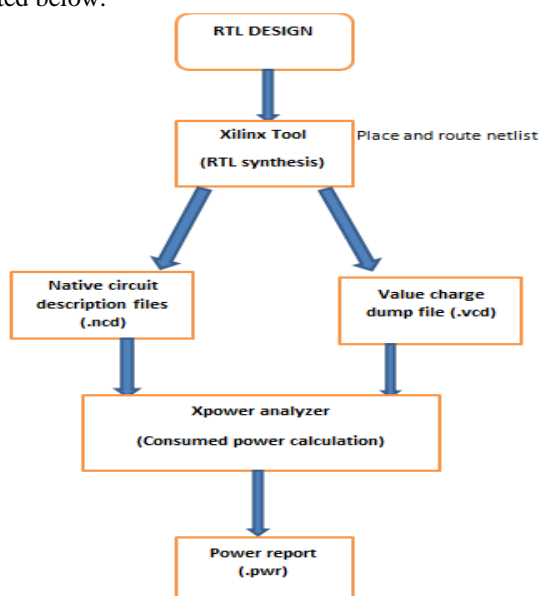


Figure-2: Flow of extracting power report

To estimate the power of RTL code, power report must be generated by using files like NCD and VCD which is generated in the Xilinx tool. NCD file represents the Netlist file which is generated by synthesis and mapping in the Xilinx tool. VCD i.e., the value charge dump file is the file that is obtained by simulating the RTL code. The NCD and VCD files are generated using the RTL design code and test bench. The native description file generated in the Xilinx tool is a fully place and route Netlist file. The value charge dump file is generated from the Xilinx tool which contains series of time ordered value changes for the signals in the given simulation model. To generate the value charge dump file from the Xilinx tool, a testbench will drive the RTL code to insert all other valid input combinations to the design input signals. At last, power calculation will be done using VCD and NCD files and the resulted report is “generated reported file” (.pwr) which is from Xpower analyzer tool.

3. EXPERIMENTS AND RESULTS FOR A CASE

The RTL design is taken from the TCP/IP protocol. The FSM for transmitter is provided in appendix Transmission control protocol and internet protocol is one of the main internet protocol suite for the communication between the devices which gives internet applications. It is parallel communicating protocol which uses 32-bits.

The current design taken is of transmission MAC layer with control path for FSM design of TCP/IP which is a sequential design having a clock signal. On a contrary, clock signal is absent in combinational circuit which does not allow for system Verilog assertion to identify glitches. For this type of RTL design, it is convenient to choose the assertion which can catch the functional bug in the clock signal. The chosen RTL design with the functional bug is shown in the Figure 3

To find the functional bug that is affecting the power consumption of the whole design can be found by writing a system Verilog assertion in the UVM environment test bench. We found glitches in FSM design as depicted in the Figure 3 because as per the specification in the TCP/IP protocol, for one clock cycle only one packet should go HIGH. But in this case few packets or outputs are going HIGH at a time or in the same clock cycle.

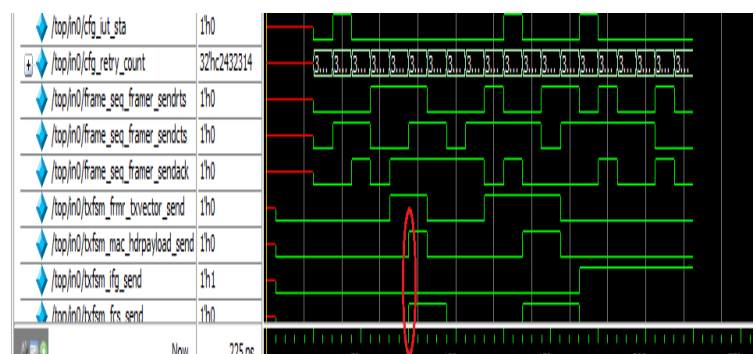


Figure-3: waveform of old RTL design

After getting simulation results the unwanted signal which is effecting the power consumption will be corrected. The depicted Figure 4 is the new bug free modified design

simulation result. As shown none of the output signals are HIGH in the same clock cycle.

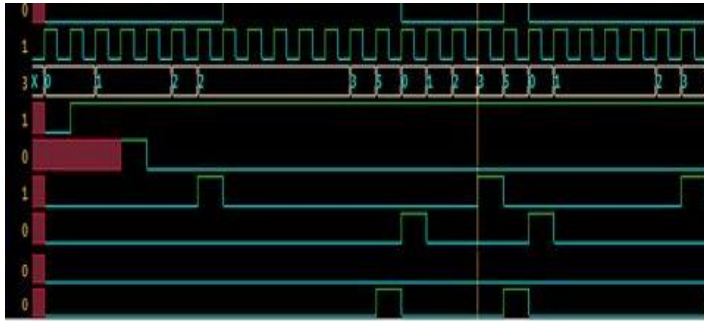


Figure-4: waveform of modified design

To check the difference in the power estimation part, we can use the flow of the power estimation using Xpower analyzer tool.

J	K	L	M	N
Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.000	0.633	0.023	0.610
Vccaux	2.500	0.046	0.001	0.045
Vcco25	2.500	0.016	0.015	0.001
MGTAVcc	1.000	0.303	0.000	0.303
MGTAVtt	1.200	0.213	0.000	0.213
Supply Power (W)		Total 1.345	Dynamic 0.062	Quiescent 1.283

Figure-5: Power estimated report of the old RTL design

Figure 5 is the screenshot of the power calculation of old RTL design, which is calculated using Xpower analyzer tool. The tool settings are: family – virtex6, part – xc6vlx75t, package – ff484, speed grade = -3. The power calculation is done for the frequency of 1 MHz which is added in clock domain. The total power and the dynamic power calculated is shown in fig.. The total power consumed from the old design is 1.345W and the dynamic power is calculated to be 0.062W. Total power includes static power or quiescent power and dynamic power.

J	K	L	M	N
Supply Source	Summary Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.000	0.630	0.021	0.609
Vccaux	2.500	0.045	0.000	0.045
Vcco25	2.500	0.001	0.000	0.001
MGTAVcc	1.000	0.303	0.000	0.303
MGTAVtt	1.200	0.213	0.000	0.213
Supply Power (W)		Total 1.304	Dynamic 0.021	Quiescent 1.283

Figure-6: Power estimated report of the modified RTL design

Figure 6 depicts the power calculation of total power and dynamic power from the modified RTL design. The total power is **1.304W** and Dynamic power is **0.021W**.

The summary of the results are as depicted in table 1

	OLD RTL DESIGN	MODIFIED RTL DESIGN	PERCENTAGE OF DECREASE IN DYNAMIC POWER
DYNAMIC POWER(W)	0.062	0.021	66%
TOTAL POWER(W)	1.345	1.304	

Table-1: Table of Result

Based on the depicted power estimated report, some of the conclusions are given below.

1. **Total power reduction:** Quiescent and dynamic power in old RTL code is 1.345W which is reduced to 1.304W in modified RTL code.
2. **Dynamic power reduction** in old RTL code is 0.062W which is reduced to 0.021W in modified RTL code. Therefore, in the dynamic power, the difference between old and modified RTL code is 0.041W. Therefore the percentage of reduction is 66%.

4. CONCLUSION

This paper suggests a method that uses System Verilog assertions and UVM methodology to enhance power utilization. Using System Verilog assertion and UVM, it is easy to observe the entire design signal whenever required. This technique facilitates in pointing out the mistakes in code while setting the design signals. These mistakes are responsible for consuming extra power. It also reflects in the simulation and the glitches can help in correcting the code at RTL level. Though this methodology is adapted at abstraction level of the Register Transfer Level, the given procedure is a conventional technique which can be used on any Register Transfer Level design code to improve it.

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