Power Gated Circuits with Self Data Retention

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Abstract

The power gating has become one of the most widely used circuit design technologies for reducing leakage current. Different power gating techniques namely Standard Power Gating (PG), Autonomous Power Gating (APG) and Power gating using Tri-modal Switch are presented. In PG and APG, Data retention elements namely flip-flops and isolation circuits are used to preserve the circuit state during standby mode, if the circuit state is required after wake up. An external power management unit is used for controlling the retention elements in PG causing network of control signal implemented with wires and buffers. Retention elements in APG control themselves without explicit control by using a PMOS switch. The power gating using Tri-modal switch implements data retention without the use of retention flip-flops. This technique benefits from a new tri-modal switch design in the form of header or footer, which can operate in three different modes: active, sleep and drowsy. The experiments with 50 nm technology in mentor graphics EDA tool shows that, compared to PG and APG the power gating using Tri-modal switch reduces the power consumption up to 90% by making use of Tri-modal switch.

Keywords: Data retention, drowsy, low power, power gating.

1. Introduction

Leakage power has been growing with every process of generation and is now responsible for a high portion of total power consumption. Power gating [3] is one of the most popular techniques to minimize standby leakage by cutting off the circuit power supply rails during standby mode. Leakage current is present in both active and standby modes of operation. To reduce the standby leakage power consumption, the circuits can be put in power down mode by switching off the power. The transistors switching off the power are called sleep transistors. For switching off the Vdd, pMOS sleep transistors are required between real Vdd and Virtual Vdd of the circuit. Likewise, for switching off the ground, nMOS sleep transistors are required between the real ground and virtual ground. Since the sleep transistors are fairly large nMOS sleep transistors are preferred than the pMOS sleep transistors.

When a sleep transistor or footer is located between a logic block and ground is turned off, the voltage at the virtual ground (Vssv) raises slowly until it reaches a steady state potential, which is usually close to Vdd. Similarly, if a header is used and if it isturned off, the voltage at the virtual Vdd (Vddv) goes down slowly to a steady state potential which is close to Vss. Due to collapse of either Vddv or Vssv during stan dby mode, the circuit states that

are represented by sequential elements and primary outputs has to be captured in advance and preserved. The approach of state retention mainly relies on dedicated circuit elements. A sequential element, especially flip-flop that is capable of retaining a state is called a retention flip-flop; extra circuit that is placed near the output to hold the output value is called isolation circuit.

There are several varying implementations of retention flip-flop and isolation circuit, that require explicit control from an external controller, which is also responsible for controlling header or footer, in addition of being main source of standby leakage. For circuits with many sequential elements and primary outputs, wiring of the control signals for circuit elements can translate into a significant increase to total wire length and buffers, similarly to the overhead of clock network.

2. Standard Power Gating (PG) and Autonomous Power gating (APG)

In both Standard Power Gating and Autonomous Power Gating, the combinational gates are located between Vdd and Vssv as shown in Figure. 1 and Figure. 2, The Vssv is controlled by footer, which is turned on during active mode and turned off during standby mode. The conventional retention flip-flop can preserve the

state of the circuit even when the footer is turned off; this is made possible by connecting a slave latch directly between vdd and Vss. Similarly, the conventional isolation circuits preserve the state of the output when footer is turned off. However, the sleep control input SLEEPBAR is connected to an external power management unit (PMU), thus causing extra wires and buffers between flip-flops and PMU. In APG the retention flip-flop is replaced by Autonomous Retention Flip-flop (ARF) and the conventional isolation circuit by Autonomous Retention Isolation (ARI). However, the Sleep control input SLEEPBAR is connected to local Vssv rather than to an external PMU, thus eliminates wires and buffers between itself and PMU. In APG, when the footer is turned off, Vssv raises towards Vdd but very slowly, for the SLEEPBAR inputs of ARF and ARI, the data cannot be properly captured and preserved; large amount of short-circuit current may flow in ARF and ARI during transition. This can be resolved by adding a large pMOS switch located between Vdd and Vssv, called the Sleep Charge Pump (SCP) as shown in Figure. 2. The SCP is driven by a pulse generator. Once the SLEEPBAR goes high to make transition to standby mode, the pulse generator produces a short pulse that shortly turns on the SCP, which in turn allows the Vssv to rise towards Vdd in a short period of time, thereby the state of the circuit is captured and preserved without and data loss in the standby mode.

The size of the SCP and width of the pulse applied to it are important design considerations [2].

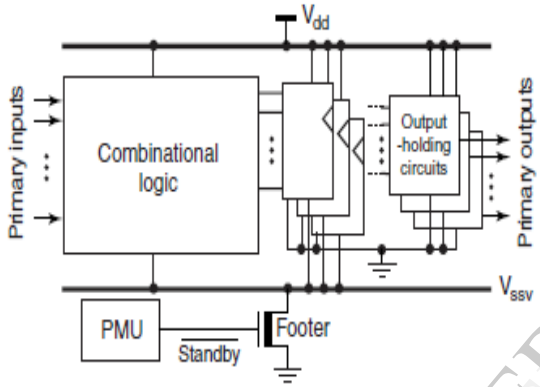

Figure.1 Standard Power Gating.

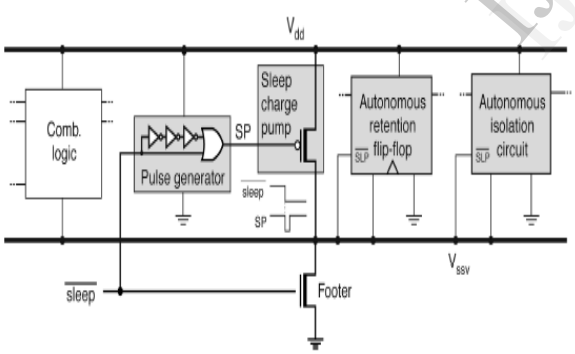

Figure.2 Autonomous Power Gating.

2.1 Circuit elements for PG and APG

The circuit in Figure.3 shows a conventional retention flip-flop which is negative edge triggered. The flip-flop is made of two latches: master and slave. When the clock is high, load master is transparent while the slave latch is disconnected from master latch preserving the previous value of the output. Likewise when the clock goes low during negative edge of the cycle the slave latch is enabled and will update its state. The slave latch

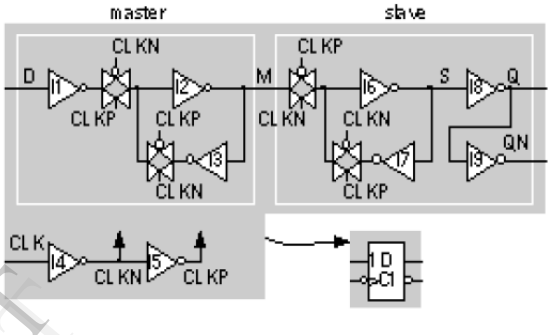

Figure.3 Conventional Retention Flip-flop

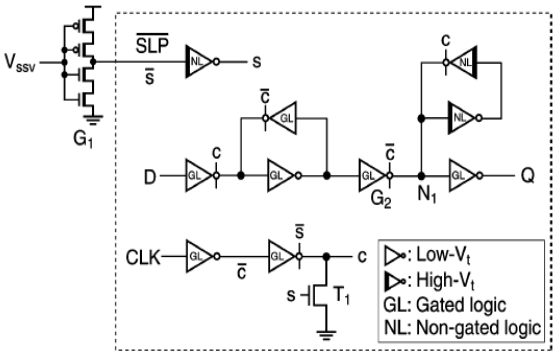

Figure.4 Autonomous Retention Flip-flop (ARF)

will keep the value of the master latch at the output despite the changes at the input.

The circuit within the dotted line of Figure.4 is an example of Autonomous Retention Flip-flop (ARF). The gated marked GL are power gated, and are thus connected between Vdd and Vssv; those marked NL are not power gated and are connected to Vdd and directly to Vss. When SLEEPBAR is high during active mode, nMOS switch T1 is turned off and footer is turned on, which allow the retention flip-flop to function as a normal flip-flop. When the SLEEPBAR is low during standby mode, the footer is turned off, the switch T1 is turned on, which keeps the net c low, which in turn allows the

slave latch to capture and preserve the current data of the flip-flop. The SLEEPBAR signal which is connected to Vssv, which is the power rail and thus can be accessed directly through an inverter G1 as shown in Figure.4. The steady state voltage of Vssv in standby mode is determined by the size of the footer. The footer is sized by the requirement during active mode, specified by the amount of delay increase or by the amount of Vssv that can be tolerated. This slightly keeps Vssv slightly low than Vdd during standby mode. The stacked inverter is employed at G1 in order to avoid the sub threshold leakage of the pMOS device when the footer is turned off during standby mode. The clock is also maintained low in ARF before turning off the footer because it may affect the master latch through G2, thus the clock is usually gated during standby mode.

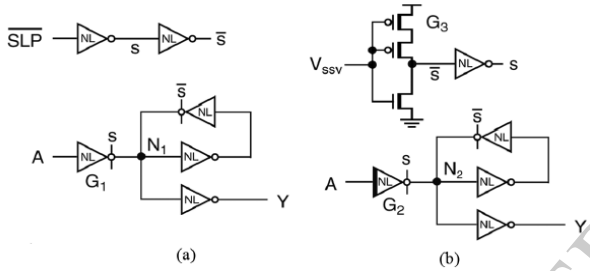

Figure.5 (a) Conventional isolation circuit (b) Autonomous Retention Isolation (ARI)

Figure.5 (a) shows an example of an conventional isolation circuit. When SLEEPBAR signal is high during active mode, the circuit is transparent (i.e.) Y is equal to A. When A is high and SLEEPBAR goes low during standby mode, N1 is decoupled from A due to G1 and is maintained in the latch. When A is low, (A comes from the power gated circuit, and thus logic low implies Vssv) and before power gating starts, N1, which is high, can adversely go low once footer is turned off, since Vssv slowly rises which makes G1 start to discharge. However, since Vssv rises very slowly in PG, once SLEEPBAR goes low, N1 is decoupled from A and preserves the data stored in the latch.

Figure.5 (b) shows AFI. When Vssv is high during active mode, the circuit is transparent. When A is high and the footer is turned off (Vssv will rise towards Vdd Slowly), it is readily seen that N2 can be safely captured in the latch. When A is low and the footer is turned off, however, care needs to be taken to guarantee the integrity of N2. In conventional isolation circuit G1 reaches high impedance before A raises enough to make the latch capture the wrong value, Since SLEEPBAR comes from PMU while A raises very slowly. The control input G2(s) and input (A) both originate from Vssv as shown in Figure.5 (b). In order to ensure that G2 goes to high impedance state before A starts its impact on N2, so that A does not propagate to N2 too early.

3. Power Gating using Tri-modal Switch

This technique implements data retention without requiring retention flip-flops. The tri-modal switch design is in the form of header or footer, which can operate in three different modes namely active, sleep and drowsy. The drowsy mode, an intermediate power saving mode, reduces the leakage current while preserving the contents of the cell.

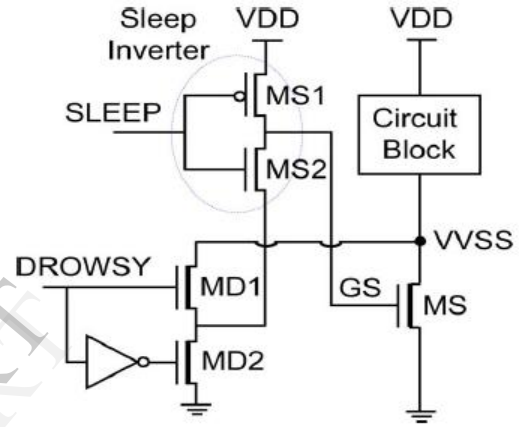

Figure.6 Implementation of tri-modal footer cell

The tri-modal switch has two input signals SLEEP and h. This switch provides three different circuit operation modes namely sleep, drowsy or active, depending upon the value of the control signals as shown in Table 1.

Table.1 Tri-modal Switch Functionality

SLEEP	DROWSY	Switch function
0	X	Active
1	0	Sleep
1	1	Drowsy

When SLEEP goes low, MS1 is ON and the voltage level at GS is Vdd. Thus, independent the value of drowsy input, the MS transistor is on and the circuit operates in active mode. When the SLEEP is high, the tri-modal switch operates in drowsy or sleepy mode depending upon the value of the DROWSY signal. If the DROWSY signal is low, MS2 and MD2 will both be ON, MS is OFF, and the tri-modal switch will operate in sleep mode. If both SLEEP and DROWSY are high, MS2 and MD1 will be ON, creating a negative

feedback between Vssv and GS nodes which puts the circuit block into the drowsy mode.

5. Simulation Results

The operation of various circuit elements in PG, APG and Power gating using tri-modal switch are shown in the form of waveform during active mode and standby mode; Drowsy mode for tri-modal switch. The PG and APG is applied to combinational circuits and their data is retained during standby mode using flip-flops and isolation circuits, whereas in power gating using tri-modal switch the data retention takes place without the use of retention elements.

In PG the combinational gates are located between Vdd and Vssv; Vssv is controlled by footer, which is connected to PMU. The Footer is turned ON during active mode and OFF during standby mode. When the SLEEPBAR signal is high, the flip-flop and isolation circuit act as an ordinary flip-flop and isolation circuit. When the SLEEPBAR signal goes low, the flip-flop and isolation circuit act like state retention circuits and thereby the previous values of the circuit is maintained. The Figure.7 (a) shows the PG for an inverter circuit, and Figure.7 (b) shows the PG for an adder circuit.

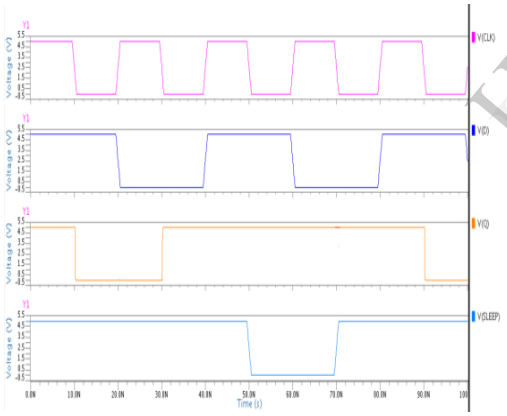

Figure.7 (a) shows the PG for an inverter circuit

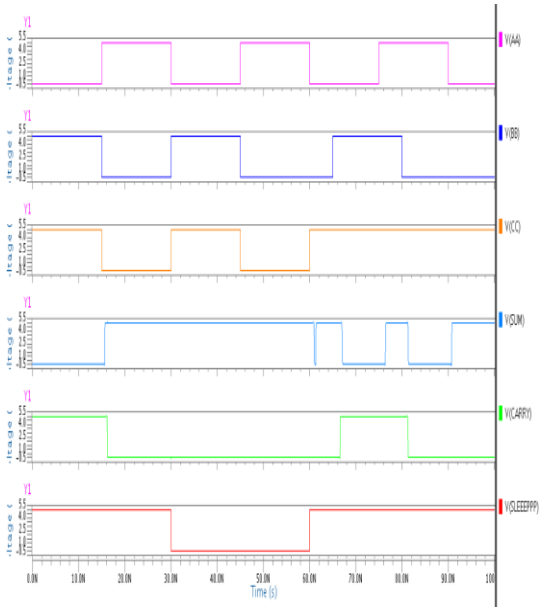

Figure.7 (b) shows the PG for an adder circuit.

In APG the combinational logic block is located between Vdd and Vssv; Vssv is controlled by footer, which in turn is connected to local Vssv rather than PMU. In APG conventional retention flip-flop is replaced by ARF and the isolation circuit is replaced by ARI. When the footer is turned ON the circuit operates in active mode and when the footer is turned OFF, the circuit operates in standby mode. The Figure.8 (a) shows the APG for an inverter circuit and 8 (b) shows the APG applied for an adder circuit. The SLEEPBAR signal is connected to footer itself rather than PMU thereby extra wires and buffers are minimized.

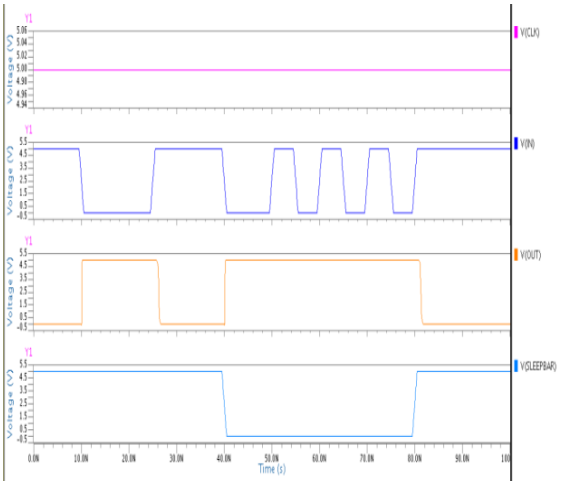

Figure.8 (a) APG for an inverter circuit

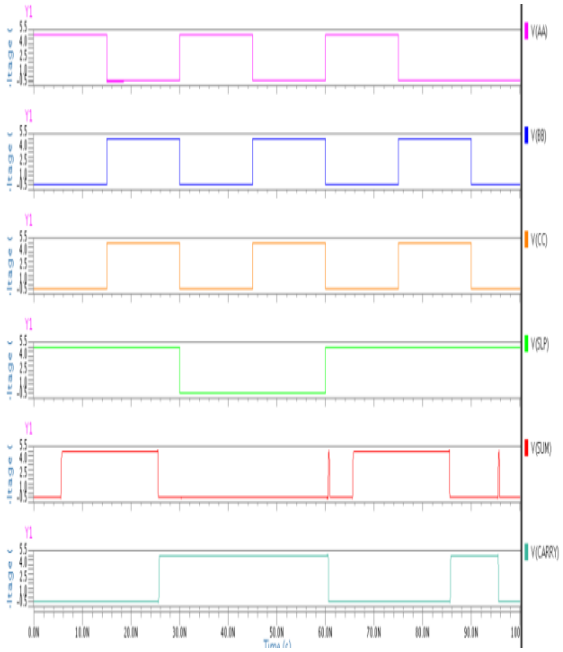

Figure.8 (b) APG for an adder circuit

The tri-modal switch operates in three different modes, when the SLEEP is low and DROWSY state maybe either high or low, the circuit operates in active mode. When the SLEEP is high and DROWSY is low the circuit operates in sleep mode. When the SLEEP and DROWSY signals are high the circuit operates at drowsy mode. The drowsy mode is the intermediate power saving mode, reduces the leakage current while preserving the state of the circuit.

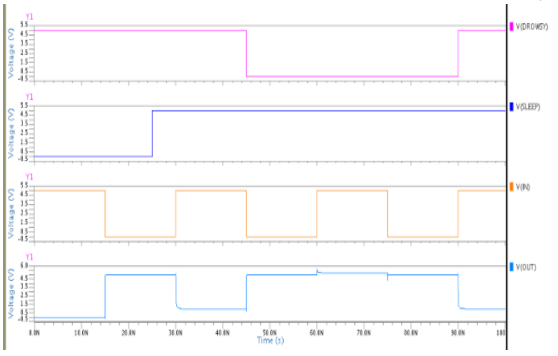

Figure.9 (a) Tri-modal switch in inverter.

Figure.9 (b) Tri-modal switch in full adder.

The power gating can be applied to any combinational circuits and the power dissipation of individual circuit is listed in the form of tabular column. The column shows that the total power consumed by circuit operating using tri-modal switch is very much less when compared to Autonomous Power Gating and Standard Power Gating where the leakage power is also much reduced during the switching from active mode to standby mode or vice versa.

Table.2 Total Power Dissipation of Individual Circuits.

	SPG	APG	Power gating using tri-modal switch
Flip-flop	6.37mW	0.39mW	-
Isolation circuit	4.61mW	0.08mW	-
Power gated inverter	24.1mW	1.16mW	0.29mW
Power gated adder	29.2mW	7.41mW	1.27mW

6. Conclusion

The power gated circuits may have an increase in wire-length, which may significantly impact the route ability of designs. A major portion of this

increase can be attributed to extra signals to control data retention elements specific to power gated circuits. We have proposed a new circuit scheme called power gating using tri-modal switch where the state of the circuit is retained without the use of retention flip-flop, likewise in APG, the retention elements drive their own control by detecting the raising potential of Vssv rails, thereby removing extra control signals. In tri-modal switch operation, the drowsy mode is the intermediate power saving mode and reduces the leakage current while preserving the circuit previous state. Standby mode leakage power is very much reduced.

7. Acknowledgement

The authors thank the Management and Principal of Sri Ramakrishna engineering College, Coimbatore for providing excellent computing facility and encouragement.

8. References

[1] J. Friedrich, B. McCredie, N. James, B. Huott, B. Curran, E. Fluhr, E.Chan, G. Mittal, D. Plass, Y. Chan, S. Chu, H. Le, L. Clark, J. Ripley, S. Taylor, J. Dilullo, and M. Lanzerotti, "Design of the Power6 microprocessor,"in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2007,pp. 96–97.

[2] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOScircuits," Proc. IEEE, vol. 91, no. 2, pp. 305–327, Feb.2003.

[3] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, "A 1-V power supply high-speed digital circuit technology with multithreshold-voltage CMOS," IEEE J. Solid-State Circuits, vol. 30, no. 8, pp. 847–854, Aug. 1995.

[4] K. Usami, N. Kawabe, M. Koizumi, K. Seta, and T. Furusawa, "Automated selective multi-threshold design for ultra-low standby applications," in Proc. Int. Symp. Low Power Electron. Des., Aug. 2002, pp. 202–206.

[5] , S. G. Narendra and A. Chandrakasan, Eds., Leakage in Nanometer CMOS Technologies. New York: Springer, 2005.

[6] M. Keating, D. Flynn, R. Aitken, A. Gibbons, and K. Shi, LowPower Methodology Manual for System-on-Chip Design. New York: Springer, 2007.

[7] S. Shigematsu, S. Mutoh, Y. Matsuya, Y. Tanabe, and J. Yamada, "A 1-V high-speed MTCMOS circuit scheme for power-down application circuits," IEEE J. Solid-State Circuits, vol. 32, no. 6, pp. 861–869, Jun.1997.

[8] J. Kao and A. Chandrakasan, "MTCMOS sequential circuits," in Proc.Eur. Solid-State Circuits Conf., Sep. 2001, pp. 317–320.

[9] V. Zyuban and S. V.Kosonocky, "Lowpower integrated scan-retention mechanism," in Proc. Int. Symp. Low Power Electron. Des., Aug. 2002, pp. 98–102.

[10] H.-S. Won, K.-S. Kim, K.-O. Jeong, K.-T. Park, K.-M. Choi, and J.-T.Kong, "An MTCMOS design methodology and its application to mobile computing," in Proc. Int. Symp. Low Power Electron. Des., Aug. 2003, pp. 110–115.

[11] S. Gururajarao, H. Mair, D. Scott, and U. Ko, "Ultra low area overhead retention flip-flop for power-down applications," U.S. Appl. Pub.20060267654, Nov. 2006.

[12] T. Lueftner, J. Berthold, C. Pacha, G. Georgakos, G. Sauzon, O.Hoemke, J. Beshenar, P. Mahrla, K. Just, P. Hober, S. Henzler, D.S. Landsiedel, A. Yakovleff, A. Klein, R. J. Knight, P. Acharya,

A. Bonnardot, S. Buch, and M. Sauer, "A 90-nm CMOS low-

Power GSM/EDGE multimedia-enhanced baseband processor with 380-MHz ARM926 core and mixed-signal extensions," IEEE J. Solid-State Circuits, vol. 42, no. 1, pp. 134–144, Jan. 2007.

[13] H. Mair, A.Wang, G. Gammie, D. Scott, P. Royannez, S. Gururajarao,M. Chau, R. Lagerquist, L. Ho, M. Basude, N. Culp, A. Sadate, D. Wilson, F. Dahan, J. Song, B. Carlson, and U. Ko, "A 65-nm mobile multimedia applications processor with an adaptive power management scheme to compensate for variations," in Proc. Symp. VLSI Circuits, Jun. 2007, pp. 224–225.

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