Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 8 Issue 08, August-2019

Power-Efficient Voltage Level Shifter for Dual-Supply Applications

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***Abstract*—Reduction of power consumption has always been major design goal in energy harvesting digital devices. One effective way for low power design use of multiple voltages depends on their speed. This paper presents a fast and power efficient voltage level shifting circuit capable of converting extremely low levels of input voltages into high output voltage levels. This efficiency of the implemented circuit is due to the fact that not only strength of pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull down is also increased using a low power auxiliary circuit. Postlayout simulation results of the implemented circuit in a 180-nm technology consumes a total energy of 1.175 uJ, for an input frequency of 10 MHz, low supply voltage of 400 mV, high supply voltage of 1.8 V consuming average power of 128nW for a propagation delay of 4 ns.**

***Index Terms*—Level converter, low power, subthreshold operation, voltage level shifter.**

I. INTRODUCTION

The important aspects in very large-scale industry (VLSI) is power, delay, area . The power dissipation is one the most important factor that has to be considered while designing the circuits. Power dissipation is plays important role in portable devices. The energy consumption has not been a major concern until now, because the heat generated was dissipated by large packages, cooling fins, and fans. Sub threshold and near threshold voltage circuits consumes very less amount of power and energy. Because the supply voltage of sub-VTH and near-VTH circuits is close to or lower than the threshold voltage (VTH) of a MOS transistor and those of the peripheral circuits are still high signal communications between each circuit have become difficult when conventional LSs are used. Level Shifters are required when the chips are operating in multi-voltage domains.In this way, elaboration tasks that require substantially different performance capabilities are effectively managed [2]. Aggressive voltage scaling into the sub/near-threshold region for sections operating at $V_{DD}L$ would provide a better use of the available energy budget [2]. One of the main challenges in the design of effective MSV SoCs is the minimization of delay and energy for level conversion between different voltage domains [2]. This issue becomes particularly critical when the number of power domains and/or the bus data width in the SoC increase. Several level shifter (LS) circuits were recently proposed [4-8] to allow voltage conversion from the deep subthreshold regime up to the nominal supply voltage

level. The LS proposed in [5] is based on the Wilson current mirror configuration. This circuit results to be fast at the expense of large standby power consumption Hence, in this brief, a fast and power efficient voltage level shifter is implemented, which is able to convert extremely low values of the input voltages. Voltage level translation is needed is shown in Fig.1. when two devices have differing supply voltage nodes. Two possible conditions exist. A higher-voltage device may be needed to drive a low-voltage device. A lower-voltage device may be needed to drive a high-voltage device. If the low voltage device is the driver, the circuit typically cannot function properly without the use of a translation device.

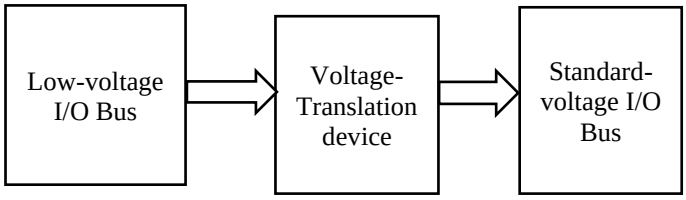

Fig. 1. voltage level shifter functioning

One of the conventional level-shifting architectures is shown in Fig. 2(a). The operation of this circuit is as follows, when the input signal IN is "High = V_{DDL}," M_{N1} and M_{N2} are ON and OFF, respectively. Therefore, M_{N1} tries to pull the node Q_1 down. Consequently, M_{P2} is gradually turned on to pull the node Q_2 up to V_{DDH} and to turn M_{P1} off. Similarly, when the input signal is changed to "Low = V_{SS}," the operation is forced to reverse states. It is noticeable that, in this structure, there is a contention at the nodes Q_1 and Q_2 between the pull-up devices (i.e., M_{P1} and M_{P2}) driven with V_{DDH} and the pull-down devices (i.e., M_{N1} and M_{N2}) driven with V_{DDL}. As a result, when the voltage difference between V_{DDL} and V_{DDH} is high and particularly when the input voltage is in subthreshold range,

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
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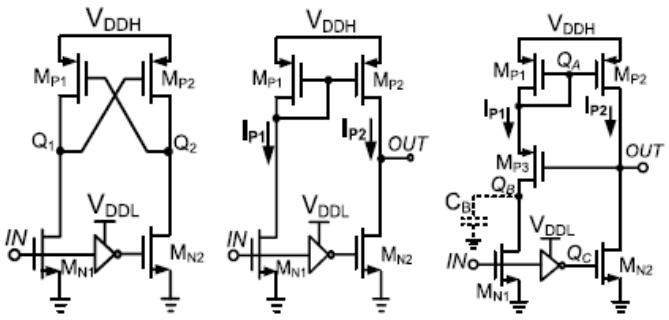
this circuit will no longer be able to convert the voltage levels. This is because the currents of the pull-down transistors are smaller than those of the pull-up devices.

To solve this problem, several attempts have been reported. One approach is to exploit technology-based strategies, e.g., employing strong pull-down devices using low-V_{th} transistors and/or weak pullup networks by using high-V_{th} transistors [4]. Another approach is to use strong pull-down devices by enlarging their width, leading to an increase in both the delay and the power consumption. The last solution is to reduce the strength of the pull-up device when the pulldown device is pulling down the output node [5]–[8]. The structure illustrated in Fig. 2(b) uses a semi static current mirror to limit the current and therefore the strength of the pull-up device (i.e., M_{P2}) when the pull-down device is pulling down the output node.



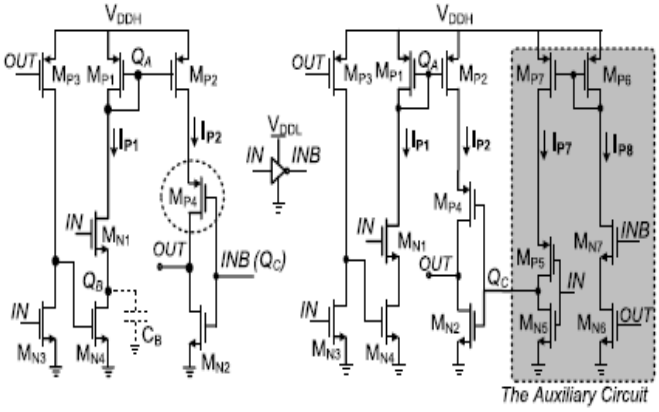
(a) (b) (c)

Fig. 2. Schematic of the (a) conventional level shifter, (b) level shifter with a semi-static current mirror, and (c) level shifter with a dynamic current mirror (Wilson current mirror) [5].

However, this structure suffers from the static current flowing through M_{N1} and M_{P1} during the "High" logic levels of the input signal. In order to decrease the static power consumption, a dynamic current generator, which turns on only during the transition times, can be used [5]–[8]. The structure shown in Fig. 2(c) employs a dynamic current generator implemented by MP3 [5]. In this circuit, when the input signal IN goes from "Low" to "High," M_{N2} turns off and M_{N1} turns on and pulls the node Q_B down. Since the node OUT had been "Low" (before the transition), during the time interval in which OUT is not corresponding to the logic level of the input signal IN, M_{P3} will be turned on. Therefore, a transition current flows through M_{N1}, M_{P3}, and M_{P1}. This current is mirrored to M_{P2} (i.e., I_{P2}) leading to pull the node OUT up. Finally, when OUT is pulled up to V_{DDH}, M_{P3} is turned off and therefore no static current flows through M_{N1}, M_{P3}, and M_{P1}. On the other hand, when the input signal IN is changed from "High" to "Low," M_{N1} turns off and M_{N2} turns on trying to pull the node OUT down. As the node OUT is gradually pulled down, M_{P3} is turned on trying to charge the node Q_B, which is already discharged to the ground, meaning that a transition current (i.e., I_{P1}) flows through M_{P1} and M_{P3} to charge node Q_B. This current is mirrored to M_{P2} (i.e., I_{P2}) and therefore tries to pull the node OUT up, while M_{N2} is trying to pull this node down. This means that there is still a contention between the pull-up and the pull-down devices in the high-to-low transition of the input signal, leading to increase in the delay and consequently the power consumption of the circuit, especially the power of the next stage.

The rest of this paper is organized as follows. The implemented circuit is introduced in Section II. Section III explains about multi supply design. Section IV presents the simulation results of the designed circuit verifying the efficiency of the implemented structure. Finally, the brief is concluded in Section V.

II. IMPLEMENTED VOLTAGE LEVEL SHIFTER



(a) (b)

Fig. 3. (a) Principle of the implemented level shifter. (b) Schematic of the implemented level shifter.

Contention is still found in Fig. 2(c) when the input signal transitions from high to low as M_{P3} is turned on which tries to charge the capacitance C_B at node Q_B. As a result, new voltage level shifter is implemented in Fig. 3 which works by suppressing the current I_{P1} and therefore I_{P2} during high to low transition of the output. In the implemented circuit. The principle operation of the implemented circuit is based on using M_{N4} to stop the static current when output is at the same logic level of the input, instead of using M_{P3} as in Fig .2(c). During "High" to "Low" transition of input signal, M_{N1} is turned on while M_{N4} is still turned off as output is still at high logic corresponding to previous state of the input. As a result output is pulled down through M_{N2} and M_{P3} is turned on charging the node Q_B to V_{DDH}. Similarly during "Low" to "High" transition of the input signal M_{N1} is turned on also M_{N4} is still turned on, even though M_{N3} is turned on, because the overdrive voltage of M_{P3} (i.e., V_{DDH}) is larger than that of M_{N3}(i.e., V_{DDL}). Therefore, a transition current flows through M_{N4}, M_{N1} and M_{P1} (i.e., I_{P1}). This current is mirrored into M_{P2} (i.e., I_{P2}) and output node is pulled up to V_{DDH}. Once the output is pulled high M_{P3} is turned off as a result gate of M_{N4} is pulled down by M_{N3}, as a result M_{N4} is turned off which results in no static current flow through M_{P1}, M_{N1} and M_{N4}. As a result in contrast to the structure shown in Fig. 2(c), roughly no transition current flows through MP1. However, when no static current is flowing through M_{P1}, M_{N1} and M_{N4} the node Q_A is just pulled up just to $V_{DDH} - |V_{th}|$, where V_{th} is the threshold voltage of M_{P1}. This means that the current of M_{P2} (i.e., I_{P2}) is still not completely close to zero but a weak subthreshold current still exists consequently a weak contention still exists between M_{P2} and M_{N2}. In order to further reduce the value of I_{P2}, another device,

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 8 Issue 08, August-2019

i.e., M_{P4} in Fig. 3(a) is used. Now during "High" to "Low" transition when M_{N2} is pulling down the output node, the gate of M_{P4} is "High" with the value of V_{DDL} and therefore the drain–source voltage of M_{P2} is decreased. As a result both power and the propagation delay
during high to low transition of input signal is reduced therefore the. If however the gates of M_{N2} and M_{P4} are driven with a voltage higher than V_{DDL}, not only the current of the pull-up device (i.e., I_{P2}) is drastically reduced, but also the strength of the pull-down device (i.e., M_{N2}) is increased. Thus, the contention and therefore the delay and the power are significantly reduced. Moreover, the level shifter will be able to properly even for subthreshold input voltages. In order to apply this technique to the implemented structure, as shown in Fig. 3(b), an auxiliary circuit (i.e., M_{P5}, M_{P6}, M_{P7}, M_{N5}, M_{N6}, and M_{N7}) is used. This auxiliary circuit turns on only in the high-to-low transition of the input signal to pull up the node Q_C to a value larger than V_{DDL}. The operation of this part of the circuit is as follows. When IN changes from "High" to "Low" and OUT is not still corresponding to the input logic level, M_{N6}, M_{N7}, and M_{P6} are turned on and MN5 is turned off. Therefore, a transition current flows through M_{N6}, M_{N7}, M_{P6}, and mirrors to M_{P7} (i.e., IP7) pulling up the node Q_C. This means that MP4 is turned off and M_{N2} is turned on with a voltage higher than V_{DDL}, as shown in Fig. 3(b), leading to a significant reduction in the aforementioned contention. Finally, when OUT is pulled down, M_{N6} is turned off and consequently no current flows through M_{N6}, M_{N7}, andM_{P6} meaning that the auxiliary circuit is turned on only during the high-to-low transition of the input signal. It can be concluded that the working of the implemented circuit is based on reducing the strength of the pull-up device when the pull-down device is pulling down the output node, also the strength of the pull-down device is also increased in the circuit using an auxiliary circuit. Finally, during "Low" to "High" transition of input signal when the output is at "Low" level a short circuit flows through M_{P3} and M_{N3} so in order to reduce the short-circuit current, instead of the output signal, the input is used to drive the gate of M_{N3}. In other words, in the conventional inverter, both low-to-high and high-to-low short-circuit currents exist whereas in the implemented structure, only a small current at the low to-high transition exists. Moreover, this current is reduced due to the fact that the gate of M_{N3} is driven by V_{DDL} not V_{DDH}.

III MULTI SUPPLY DESIGN

In order to verify the functionality of the proposed level shifter, it is implemented in Dual supply design. This application is consists of three blocks- Half-adder, voltage level shifter and D-latch.

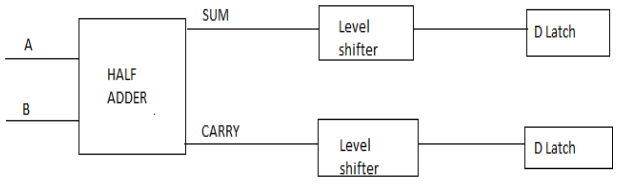


Fig.4. Block diagram of multi supply design

1.Half adder

HA is a combinational circuit that performs addition. It consist of two inputs and two outputs. It consists of one XOR gate and one AND gate. The inputs to Half adder are A and B respectively and outputs to half adder are SUM and CARRY.

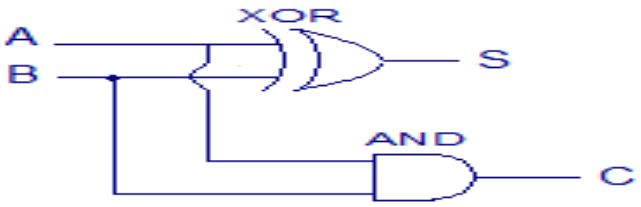


Fig.5.Half-adder circuit

2.*Voltage level shifter*

The SUM of half adder is applied as input to one level shifter and CARRY of half adder is applied to another level shifter. The input of 1 V is applied to level shifter and converts this voltage to 3 V.

3. *D-latch*

The D-latch is designed using a combination of four NAND gates and inverter .It has D input, Enable input and Output Q and Q b

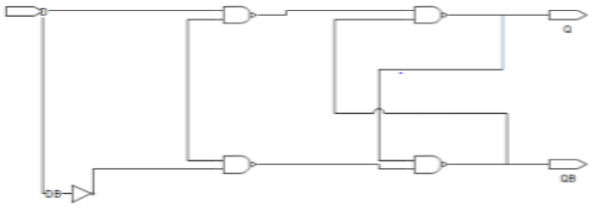


Fig.6. D-latch implementation by using NAND gates

IV SIMULATION RESULTS

Fig. 7 shows the implemented voltage level shifter using 180 nm technology in cadence virtuoso. Then the transient response due to input signal is obtained as shown in Fig. 8.

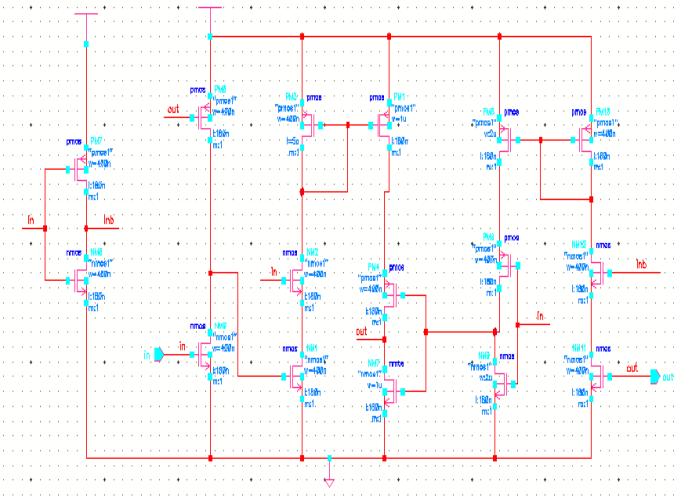


Fig. 7.Voltage Level Shifter with Auxiliary Circuit

International Journal of Engineering Research & Technology (IJERT)
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The power consumption of voltage level shifter can be classified in two static power consumption and dynamic power consumption. Static power dissipation is found more in this design during high to low transition of output signal. This is higher than dynamic power dissipation, which arises due to charging and discharging of load capacitance.

The implemented level shifter with auxiliary circuit was further modified to optimize the delay and power delay product by trying to increase the V_{th} of the switching transistor thereby reducing the dynamic power dissipation.

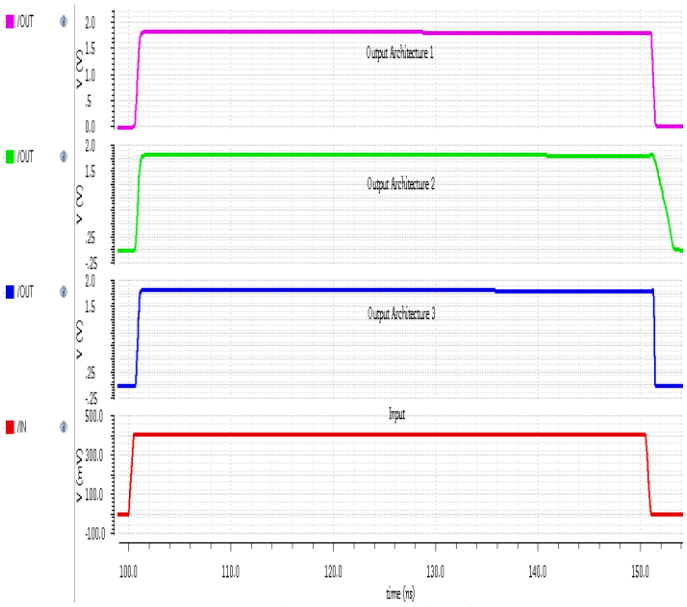

Fig. 8. Transient response of all the level shifters for the input signal.

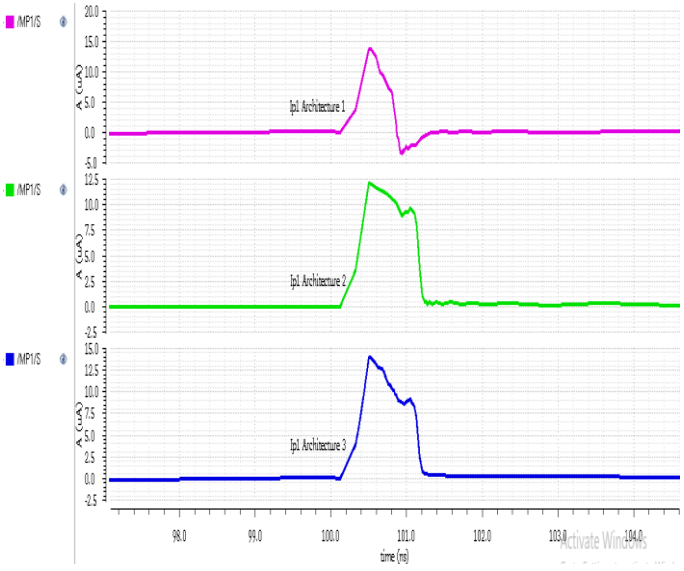

Fig. 9. Current IP1 during low to high transition of the input signal.

Current flowing through the MP1 during low to high transition of the input signal is shown in Fig. 8.

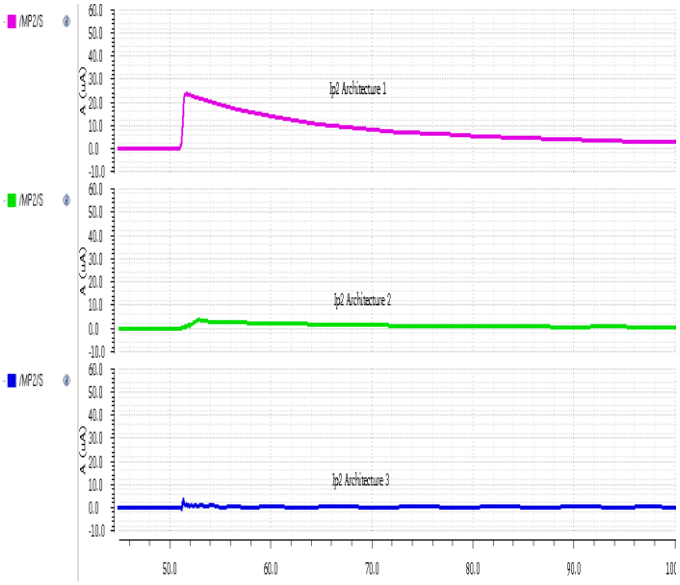

Fig. 10. Current flowing through the output branch during high to low transition of the input signal

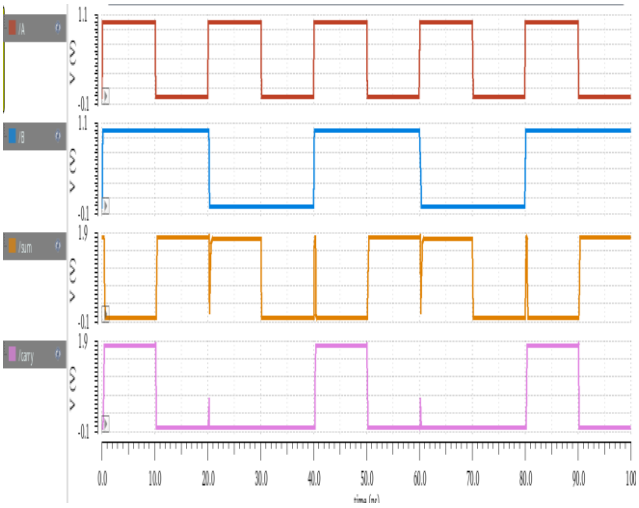

Fig. 11. simulated waveforms of half adder

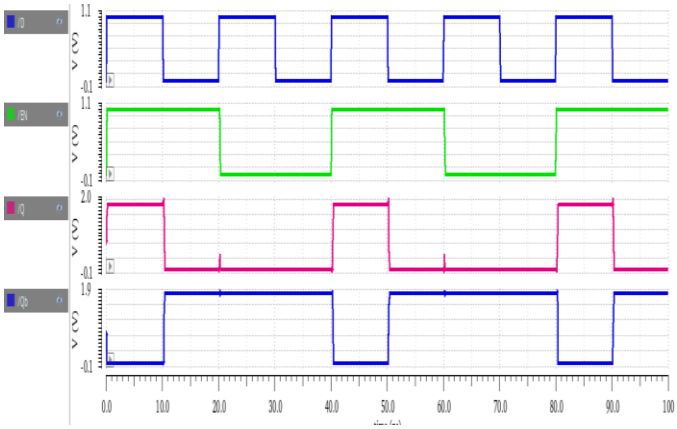

Fig.12.simulated waveforms of d-latch

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ISSN: 2278-0181
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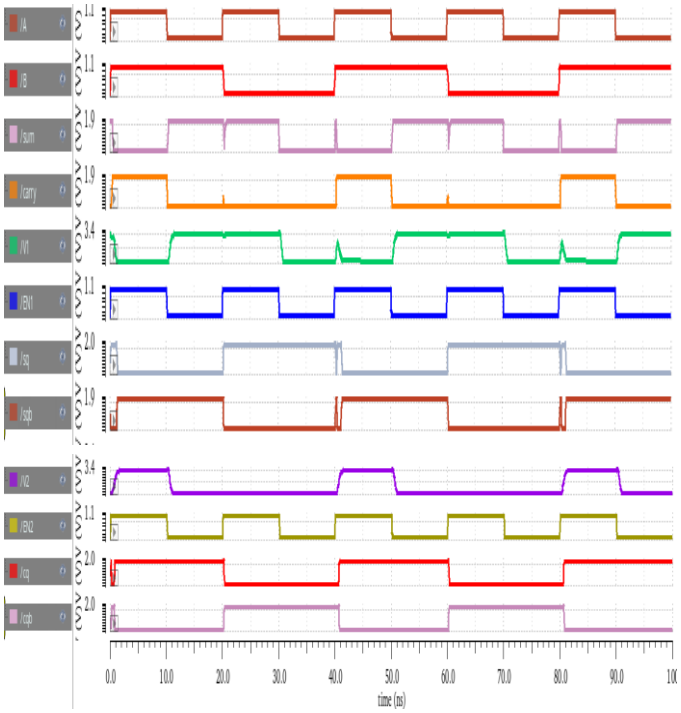

Fig.12.simulated waveforms of multi-supply design

Table 1 Comparison Results of Voltage Level shifters

Architecture	Average Power (nW)	Delay(ns)	Power Delay Product(nW.nS)
1	4761	5.2	4639.8
2	766.9	8.07	6188.2
3	117.7	6.3	741
4	128	4.6	588

V CONCLUSION

Power Dissipation is one of the major factors that is to be considered in designing of circuits. Different techniques are considered to attain the low power dissipation circuits. In this brief, a fast and low-power voltage level-shifting architecture was proposed which is able to convert extremely low-input voltages. The efficiency of the proposed circuit is due to the fact that not only the current of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased

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