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# Power-Efficient STC-DET with SAPON in CMOS Circuits

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***Abstract*- Flip-flops have evolved as power-rigorous elements inside processors in a modern age that is driven by Artificial Intelligence (AI) along with Graphics Processing Units (GPUs). To take care of this issue concerned with power usage, a novel solution has been proposed, employing a Single-Transistor Clocked Buffer (STCB) alongside a 1-phase clock Dual-Edge-Triggering (DET) flip flop. The deployed STCB has a single-clocked transistor in the information sampling route, which eliminates redundant transitions (RTs) as well as intrinsic RTs associated with the clock, which is usually encountered in other DET layouts. According to the findings of the simulation (after design) across 22 nm fully depleted silicon on insulator (FD-SOI) CMOS, a novel configuration being devised outperforms contemporary cutting-edge reduced-power DETs in terms of efficacy of power, enhancing the least Power-Delay-Product (PDP) amongst its competitors. Design of True Single-Phase Clock (TSPC) Single Transistor Clock Dual Edge Triggering (STCDET) can be further enhanced with the prospects offered by the following: altered gating of clock, gate technique, Sub-threshold Leakage Attenuation through P- and N-type transistors (SAPON), and Transmission Gate. Thus, it becomes possible to cut down certain variables like power, delay, etc., which is validated further.**

***Keywords*: Dynamic power, Dual-Edge-Triggering, True Single-Phase Clock, flip flop, and SAPON.**

## I. INTRODUCTION

One of many critical challenges in present-day electronics is the power effectiveness of devices [1-3]. The problem grows increasingly serious once faced with electronic circuits that are combined [4]. Memory cells and microprocessors are not exceptions to suffer due to these problems. Flip flops are a fundamental memory component [5, 6]. The widespread usage of flip flops in pipelining procedures demonstrates the significance of the power effectiveness of equipment [7, 8]. Flip flops, as fundamental elements, constitute a significant portion of the power in digital devices [9-11]. As a result, decreasing the power usage of the flip flops may dramatically lower the total power usage associated with digital devices [9].

With reference many literature's like [1, 12-16], the flip flops could be categorized into 3 major types, which are as follows:

- Master Slave-flip flops
- Transmission Gate-flip flops
- Pulse Triggered-flip flops

Given the ability of flip flops to synchronize data flow and enable local data storage, they are among the most crucial circuit components in contemporary digital circuit design [17]. A common processor uses a high number of flip flops, generally several thousands, since this kind of synchronization needs to be carried out across the whole clock realm [11]. Flip-flops are so many that they take up a significant amount of space in the circuitry architecture, both by means of physical region and power consumption. For this reason, reducing the power usage of flip flops considerably affects system-level efficacy of energy, particularly for IoT applications with limited energy [17].

Employing the falling or rising clock edge as the trigger origin for the process of latching is the most often used method for building a flip-flop. Because of its straightforward construction and convenient temporal characterization, this type of flip-flop is regarded as a Single-Edge-Triggered flip-flop (SET-FF) and is used extensively [18-22]. Conversely, Dual-Edge-Triggered flip-flops (DET-FFs) leverage the edge of clock that is not utilized by SET-FFs; that is, the latching process is initiated at both the dropping and rising edges of clocks. By allowing double the data flow across SET-FFs containing the similar clock frequency, using both clock edges possibly results in higher energy efficiency. To reduce power consumption in comparison to SET-FFs, DET-FFs have been suggested as an alternate orderly circuitry constituent [23].

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1) Background

Digital circuits may be designed using efficient flip-flops or latches by using the TSPC (i.e., Transmission-Free True Single-Phase Clock), which is a sequential logic circuit design method. Applications requiring little power and fast speed frequently utilize it.

To transfer data during the clock phase, conventional flip-flops and latches need transmission gates or pass transistors. Unfortunately, there are extra delays and power losses due to these transmission gates. These problems are resolved by Transmission-Free TSPC, which reduces power consumption and improves performance by doing away with the requirement for transmission gates.

The flip-flop in Transmission-Free TSPC is split into the three steps listed below. This is a short summary of the process:

- Pre charge Phase
- Evaluation Phase
- Latching

There are numerous advantages in using the transmission-free TSPC such as swift processing of operations, easier circuit design and minimized usage of power than using the traditional flip flops. Instead of using the transmission gates for controlling the state of the internal nodes, complementary logic signals are used for functioning without transmission.

However, it's important to take into account the transmission-free TSPC's drawbacks, which include a larger operational region and a higher vulnerability to noise or clock faults. Therefore, the technique's applicability is implied by its drawbacks and the specifications of the digital circuits that were implemented.

2) Problem statement

The effectiveness and the performance of the clock signal in digital circuits can be improved by the usage of the STCDET (i.e., Single Transistor Clock Dual Edge Triggering) technique. Here, the rising and falling edges of the clock signals are utilized for initiating the circuit activities which in turn result in two times increasing of the effective clock frequency.

The actions of conventional digital circuits are timed to the clock signal's rising edge. Nevertheless, this restricts how quickly tasks may be completed. By exploiting the rising and falling edges of the clock signal as discussed earlier, STCDET overcomes the above-mentioned restriction. Digital circuits function faster and better as a result, while the underlying circuitry is not much altered.

The fundamental concept underlying STCDET is the generation of two clock signals that are non-overlapping in nature. One clock signal is for the rising edge and the other clock signal is for the falling edge. These signals are generated through the usage of a single transistor. To do this, a capacitor's discharge is controlled by use of a transistor which also functions as a switch. The capacitor starts to charge when the transistor is in the active status and it starts to discharge when the transistor is switched off and provides the falling edge clock signal.

Applications for STCDETs may be found in different kinds of digital circuits like the high-speed CPUs, memory interfaces and data transmission systems. In all these applications, the clock frequency is optimized for efficient functioning.

3) Major contributions

The following are the major contributions of this work:

- Then, the designed DET layout is validated (with STCB) with 22 nanometer fully depleted silicon on insulator (FD-SOI) Complementary Metal-Oxide-Semiconductor (CMOS).
- We shall modify the clock gating, Sub-threshold Leakage Attenuation through P- and N-type transistors (SAPON), Transmission Gate, and gate approach for refining the TSPC Single Transistor Clock Dual Edge Triggering (STCDET) layout and corresponding parameters.

4) Paper Organization

The forthcoming sections of the paper have been organized as follows:

Section II will be presenting a novel and enhanced architecture proposed in this work; Section III will be presenting performance-oriented analysis with the common performance measures of power usage criteria; Section IV will be presenting the concluding remarks of our research and comment on its performance.

## II. PROPOSED DESIGN

At the center of CMOS circuitry, increasing voltage (threshold) to accomplish voltage decrease unavoidably boosts sub-threshold current leakage, resulting in a rise in constant power consumption. To tackle this issue, we describe a new strategy for CMOS gate layout that combines altered Clock Gating along with the SAPON approaches, significantly reducing current leakage with no increase in loss of dynamic power. Two types of transistors p-type and n-type leakage control transistors are included into the logic gate as part of the SAPON technology. Most importantly, one leakage control transistor (LCT) is always "near its cutoff voltage" for any combination of inputs because the gate terminals of each LCT are closely connected to each other's sources. Because of this tactical configuration, leakage currents are significantly reduced when the resistance increases significantly from V/sub dd/ to ground.

To create a leakage-controlled circuit, the gate-level netlist of the circuit must be converted into a static CMOS complex gate. This is done by adding LCTs. One of the most important aspects of SAPON and Modified Clock Gating is that they are more successful in reducing leakage than other approaches, both in the active and idle stages of the circuit.

When the threshold voltage is lowered in CMOS circuits, voltage scaling causes sub-threshold leakage current to increase, which in turn causes increased dissipation of static-typed power. In this innovative approach, altered Clock Gating along with Sub-threshold Leakage Attenuation through P- and N-type transistors (indicated as SAPON, develops an effective CMOS gate that can greatly lessen current leakage with no increase in loss of dynamic power. Two types of transistors p-type and one n-type leakage control transistors are included in the logic gate as the fundamental component of SAPON (shown in figure 1). Crucially, each LCT's gate terminal is connected to its source in a complex way, guaranteeing that one LCT always remains "near its cutoff voltage" for every combination of inputs. This configuration, then, reduces leakage currents significantly by increasing resistance along the route from V/sub dd/ to

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ground. To create a leakage-controlled circuit, the gate-level netlist of the designated circuit must be transformed into a static CMOS complex gate. This is done by adding LCTs. One of SAPON's outstanding qualities is that it is more effective at reducing leakage than alternative methods, whether or not the circuit is active and idle.

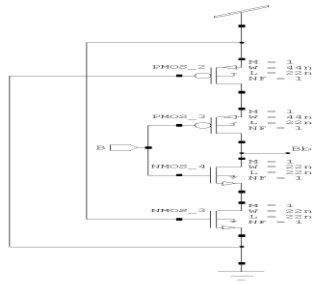

**Figure 1: Pictorial representation of SAPON**

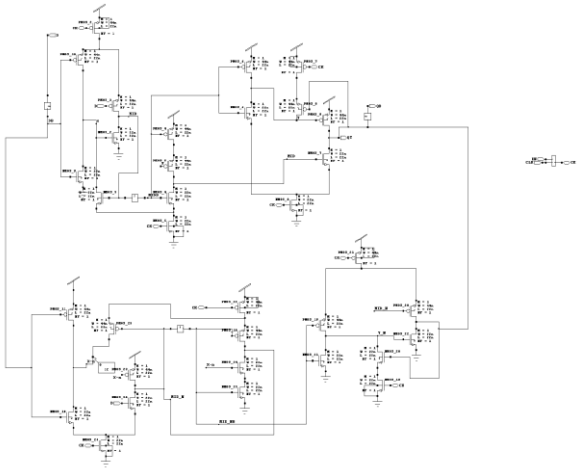

**Figure 2 :Pictorial representation of TSPC-typed STCDET with SAPON**

A. Working of the Top flip flop in DET with STCB

As shown in figure 2, Transistors (P2, N2) become equal to a virtual inverter when C L K = 0. The timed PMOS P3 of the top master latch activates when C L K = 0, shifting node X to D ″. On the other hand, node Y will not be zero in the top slave latch, meaning that PMOS P8 is off and clocked NMOS N4 is off due to C L K = 0. Next, the input passes via M I D in the upper master latch. The inability of VDD and QT to connect or GND indicates that the QT of the upper FF is floating.

Transistors N1, N2, P1, P2, and P3 make up a negative-triggered STCB. The signal sampling channel is provided by the single timed transistor P3. The RT that occurs between a clocking PMOS and a clocking NMOS is absent from STCDET, in contrast to FN_C DET and FS-TSPC. Additionally, there is no dispute. While it is used in the keeper instead of the data sampling path, the second clock-driven NMOS transistor (N3) is included in the top master latch. Like transistor P3, it is clocked similarly. An arrow has been used to indicate the location of the four transistors on the data sampling path that are clocking together. In the upper FF, transistors N4, N7, N8, P7, and P8 construct a second positive triggered STCB.

Clocked PMOS P3 is off when C L K = 1, which also means that the routes linked to P1 and subsequently N2 in the top master latch are off. Consequently, the keeper (N3, N15, P14, P15) keeps M I D's logic state operational. If X's logic state is 0, pull-down keeper (N14, N3) will preserve it. Y becomes M I D″, or almost M I D, when the timed NMOS, N4, activates at the top slave latch. Because of transistors (N8, P8) functioning as a virtual inverter, the signal from M I D, which is right before the clock rising edge, goes to QT. Consequently, at the clock positive edge, the top FF is turned on.

5) Working of the Bottom flip flop in DET with STCB

When C L K = 0 in the bottom FF, the clock NMOS, N5, in the bottom master latch activates. Therefore, the keeper (N16, N17, P5, P17) keeps the logic state of M I D_n intact, and the routes that link to N9 and P10 are rendered inactive. Keeper (P16, P5) will preserve the logic state of X_n if it is 1. On the other hand, in the bottom slave latch, Y _n becomes M I D_n ″, or M I D_n, when C L K = 0. This is because the timed PMOS P6 in the top switches on. Consequently, the signal of M I D_n arises, and P12 and N12 function as a virtual inverter. I D_n is at this point, right before the clock falling edge goes to QT. This causes the bottom FF to engage on the negative edge of the clock.

## III. RESULT AND ANALYSIS

In this section, we indicate the results obtained from the TSPC DET in the STCDET structure making use of the novel technique.

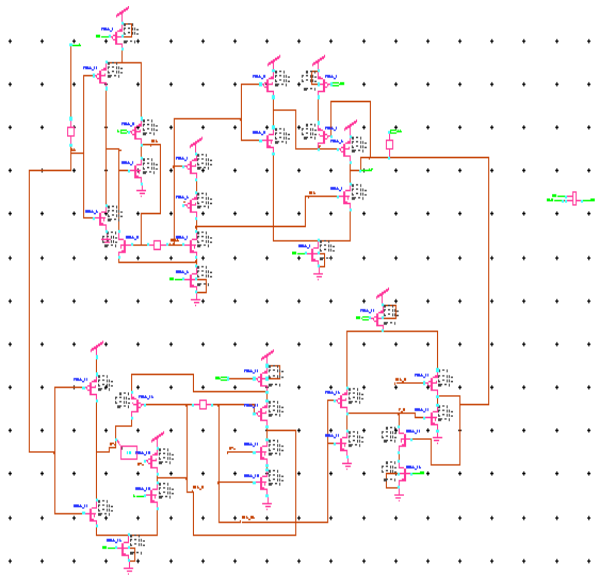

**Figure 3 Diagrammatic depiction of STCDET**

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The above figure 3 shows the diagrammatic depiction of STCDET, denoting an appreciable lowering in parameters.

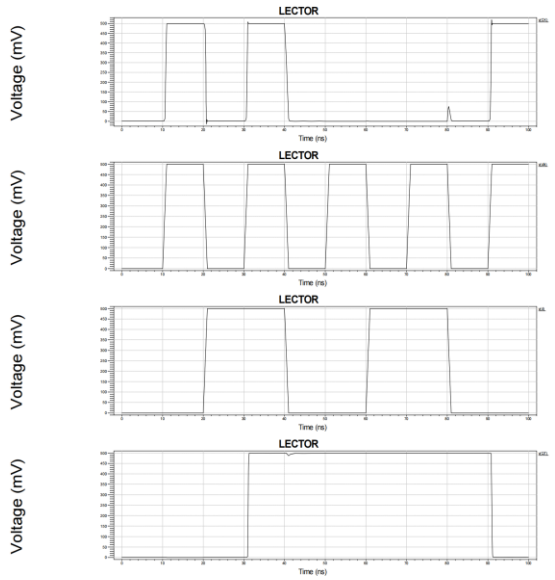


**Figure 4 : Representation of STCDET Waveform**

The above shown Figure 4 presents simulation of the waveforms, summarizing the performance offered by STCDET.
The below figure 5 exhibits the spatial range of devised circuitry, especially the TSPC in the STCDET through the area calculation.

```
*    Device and node counts:
*                  MOSFETs - 58
*                     BJTs - 0
*                  MESFETs - 0
```

**Figure 5 :Calculation of Area**

```
Power Results
vl from time 0 to 1e-007
Average power consumed -> 2.12643le-007 watts
Max power 6.935537e-006 at time 9.10585e-008
Min power 9.986249e-009 at time 2.16546e-008
```

**Figure 6 : Calculation of Power Magnitude**

The above shown Figure 6 provides perception into the power usage measures of design such as average, minimum, and maximum power consumption. Thus, a detailed summary of power magnitudes related to the implementation can be presented through this.

```
delay = 2.7012e-010
    Trigger = 3.0783e-008
    Target  = 3.1053e-008
```

**Figure 7: Calculation of Delay Value**

The above Figure 7 gives the values of delay, trigger, and target.

**Table 1: Comparison of parameters**

| | **Existing** | **Proposed** |
|---|---|---|
| **Delay** | 0.0205µs | 0.02701µs |
| **Power** | 0.2298µW | 0.2126431µW |
| **Area** | 50 | 58 |

The above table 1 provides the comparative study of system and the extension technique by means of the calculated delay, power, and area values.

## IV. CONCLUSION

A unique transition-redundant-free and reduced-power DET flip-flops (with STCB), both new and power-saving in architecture, are presented. This distinctive architecture used STCB to successfully remove RTs in DET flip flops. The negative-activated and positive-activated STC buffers in the architecture, with each having a single-timed transistor in the circuitry responsible for the sampling of information. This arrangement eliminated every clock redundant element, shift, and internal redundant shift that existed in prior DET solutions that utilized 2-clocked transistors. Importantly, the DET with STCB was not only RT-free, but it also had no power loss issues. Additionally, in a complete study of different processing conditions and voltage situations for switching action, the suggested DET with STCB was able to beat all other DET layouts by expending the smallest amount of power. Finally, among the cutting-edge DET flip flops, the recommended DET with STCB had the smallest power usage in the mean switching action spectrum.

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