International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 3 Issue 3, March - 2014

Power Efficient CMOS Full Adders with Reduced Transistor Count

Jyotshna Kamath. B, Neetu Bani
Sahyadri College , Mangalore, India

***Abstract* - In this Paper, a CMOS Full Adder is designed using Tanner EDA Tool based on 0.25µm CMOS Technology. Using Tanner software tools, schematic and simulations of CMOS full adder are designed and presented, which helps to obtain design constraints. As part of this we have performed the simulation of CMOS full adder using T-SPICE of Tanner EDA. This paper also proposes a new 3T-XOR gate with significant area and power savings. A new eight transistors one bit full adder based on 3T-XOR gate is presented. Simulations results utilizing standard 0.25µm CMOS technology illustrate a significant improvement in terms of number of transistors, chip area and propagation delay.**

Keywords- Full adder, XOR, low power CMOS, VLSI, Tanner.

I. INTRODUCTION

In VLSI design methodologies power minimization is one of the primary concerns because a long battery life is required for mobiles and portable devices, Power dissipation is increasing due increasing rate of transistors on a single chip. Adder is one of the most critical components of a processor, as it is used in the arithmetic logic unit (ALU), in the floating point unit, and for address generation in case of cache or memory access [2]. Increasing demand for mobile electronic devices such as cellular phones,

PDA's and laptop computers require the use of power efficient VLSI circuits.

There are three types of power consumption in VLSI circuits namely short circuit power, static power and dynamic power. The short circuit power dissipation is due to the short circuit current generated when both NMOS and PMOS transistors are simultaneously active for a small duration. The static power dissipation varies with process technology. The dominant dynamic power due to charging and discharging of load capacitance is given by the following equation (1),

$$\text{Dynamic Power} = \alpha (VDD)^2 f CL \text{ --- (1)}$$

Where α is the switching activity, VDD is the supply voltage, f is the switching frequency CL is the load capacitance. Lower the voltage is, the smaller the power consumption. However, using a lower VDD increases the delay. The alternate way of decreasing the power is by reducing the number of switching transistors. The power consumption of a CMOS digital circuit can be represented as

$$P=fCV_{dd}^{\ 2}+fI_{short}V_{dd}+I_{leak}V_{dd} \text{..... (2)}$$

Where f is the clock frequency, C is the average switched Capacitance per clock cycle, VDD is the supply voltage, J short is the short circuit current, and J leak is the off current .In a well-optimized low power VLSI circuit, the 1st term of Equation (2) is by far the dominant. The stand-by power Consumption is accounted for by the 3rd term. Using a lower VDD is an effective way to reduce them dynamic power consumption since the 1st term is proportional to the square of VDD [3]. For full adder the Boolean expressions for some and carry is given bellow:

$$\text{Sum}=A \oplus B \oplus C$$
$$\text{Carry}=AB + BC + CA \text{..... (3)}$$

Where A, B, C are the inputs [2].

The early designs of XOR gate was based on either eight transistors or six transistors [1] that are conventionally used in most designs.

In this paper, we have reported the design and comparison, performance of two full-adder cells implemented with an alternative internal logic structure, depends upon the multiplexing of the Boolean functions XOR/XNOR and AND/OR, to obtain balanced delays in SUM and CARRY outputs, severally, and pass-transistor powerless/groundless logic styles, in order to reduce power consumption. This paper proposes a new design technique for a 3TXOR gate [2] circuit based on static CMOS inverter logic and Pass transistor logic (PTL). The rest of the paper is organized as follows, in Section 2, a review of full adders in previous works is presented. In Section 3, the proposed work on XOR gate and full adder circuit is presented, which is followed by the schematic design of TG full adder simulation results and conclusions in Sections 4, 5 and6, respectively.

II. REVIEW OF FULL ADDER TOPOLOGIES

Most of the Full adder structures make use of XOR and XNOR logic gates. Conventional CMOS [3] full adder with 28 transistors are a high power and robust full adder.

This design is based on complementary pull up and pull down topologies. It has high noise margin and reliability. The CMOS full adder suffers from large power consumption and high delay. New 14T full adder [4] based on simultaneous XOR-XNOR signals is an improvement from 14T full adder. However, it suffers from high delay. The feedback transistors need special attention, when sizing is done that increases the layout complexity. The TGA full adder [5] using 20 transistors is based on CMOS transmission gates and CMOS inverters. It provides full output voltage swing. In TFA [5], the design was

improved with 16 transistors and maintains full output voltage swing operation. Complementary pass transistor logic (CPL) full adder [3] provides high speed and full swing operation. The presence of many internal nodes and inverters results in large power dissipation.

The Hybrid pass logic (HPSC) full adders [5] with 22 transistors have poor PDP. For low supply voltages, the PDP rises drastically making them unsuitable for low-voltage operation. The hybrid CMOS style full adder [6] with 24 transistors has

better noise immunity and performs well with low voltages. The proposed 8T full adder shows better results in terms of power, delay and PDP. It occupies less area in terms of transistor counts, more suitable for supply voltage scaling and under different load conditions.

28 transistors conventional full adder is given in Fig.1 [5].In this adder design PMOS network is same as NMOS network.

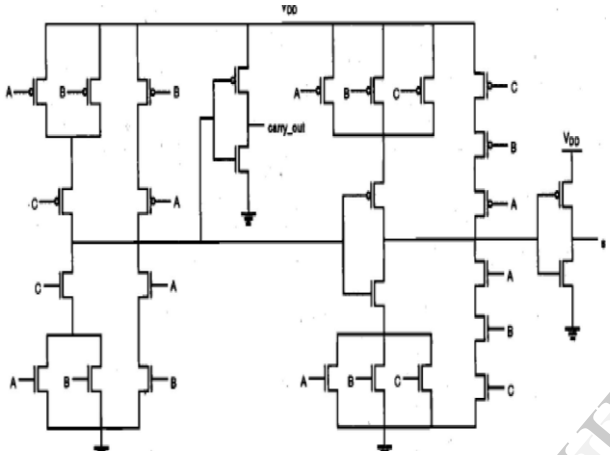


Fig.1 -The conventional design of CMOS Full Adder [5]

Conventional CMOS [3] full adder with 28 transistors are a high power and robust full adder.

III. TRANSISTOR COUNT OPTIMIZATION XOR CIRCUIT

The proposed new design of XOR logic gate using three transistors is shown in Figure-2. The design is based on modified CMOS inverter and PMOS pass transistor logic. When the input Y is at logic one, the inverter on the left functions as a normal CMOS inverter. Therefore the output is the complement of input X. When the input Y

is at logic zero, the CMOS inverter output is at high impedance. However, the PMOS pass transistor M3 is turned ON and the output gets the same logic value as input X. The operation of the whole circuit could be given as a 2 input XOR gate as given in Table-1.

Exact output logic levels are obtained for all the input combinations without any voltage degradation. However, when X=0 and Y=0,voltage degradation due to threshold drop occurs across the PMOS pass transistor M3 while passing the output logic zero and consequently the output is degraded with respect to the input.

The voltage degradation due to threshold drop can be considerably minimized by increasing the W/L ratio of transistor M3 [9]. The equation (4) relates the threshold voltage of a MOS transistor to its channel length and width.

$$V_t = V_{t0}+g(\sqrt{v_{SB}+\emptyset_0})-\alpha\frac{t_{ox}}{L}(V_{SB}+\emptyset_0)-\alpha V\frac{t_{ox}}{L}V_{ds}+\alpha w\frac{t_{ox}}{L}((V_{SB}+\emptyset_0) \quad ---(4)$$

Where V_{t0} is the zero bias threshold voltage, g is bulk threshold coefficient, ϕ_0 is ϕ_f , where ϕ_f is the Fermi potential, t_{ox} is the thickness of the oxide layer and α1, α v and α w are process dependent parameters. From equation (4) it is obvious that by increasing the width W of transistor M3, keeping the length constant it is possible to reduce the voltage degradation due to the threshold voltage. Typical values of transistor widths Wp =5.0µm for PMOS M1, Wn=2.5µm for NMOS M2, and Wp =5.0µm for PMOS M3 have been taken. The length for all the transistors have been taken constantly as L= 0.25 µm (250 nm).

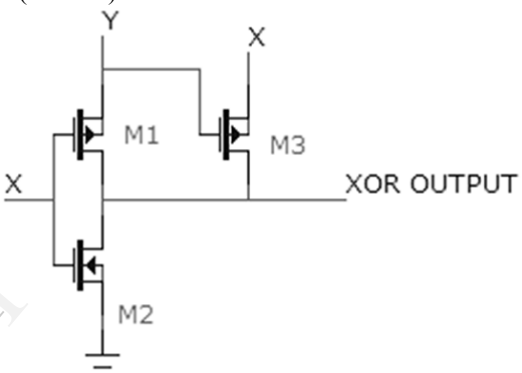


Fig-2. 3-Transistor based XOR

TABLE 1 - LOGIC TABLE OF 3T XOR GATE

Input-A	Input-B	Output = X'Y+XY'
0	0	X/0
0	1	X'/1
1	0	X/ 1
1	1	X'/0

IV. SCHEMATIC DESIGN OF TG FULL ADDER

Full adder block diagram by using by using 27 transistors is shown in Fig 3. Area and power consumed by this circuit is less as compared to full adder circuit made by XOR circuit in Fig 4.

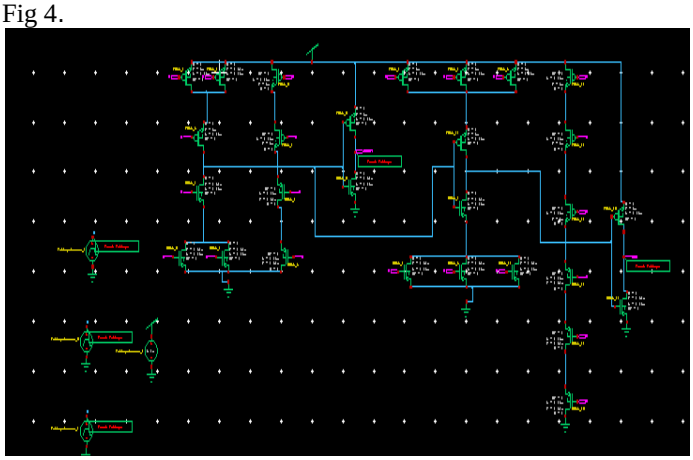


Fig3 -Full Adder by using 27 transistors

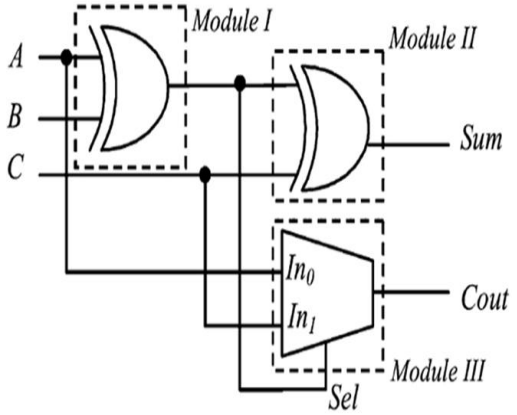
Proposed TG full adder by using 2xl MUX:

The TG full adder circuit is implemented in Tanner EDA by building following two modules:

A. One 2: 1 MUX

B. Two 2 input XOR gate.

Fig-4 shows a two-input multiplexor circuit consisting of two CMOS transmission gates. The operation of the multiplexor can be understood quite easily: If the control input S is logic-high, then the bottom TG will conduct and the output will be equal to the input B. If the control signal is low, the bottom TG will turn off and the top TG will connect the input A to the output node.



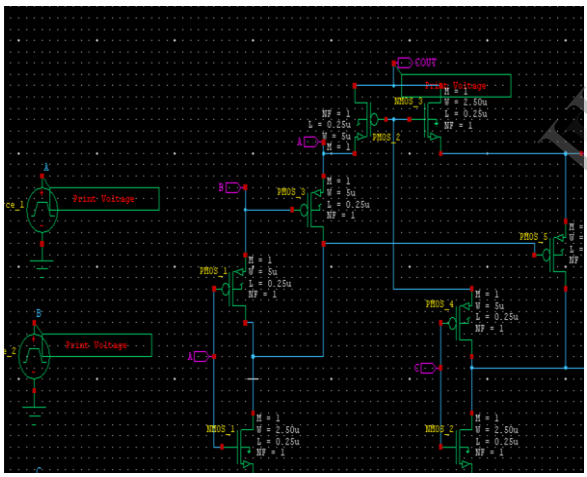


Fig 4. Full adder using two XOR gates and multiplexer (a) Block diagram
(b) Circuit diagram

The full adder operation can be given as follows: Given the three 1-bit inputs A, B, and C, it is desired to calculate the two 1-bit outputs Sum and Carry, where Sum=A$\oplus B \oplus C$,
Carry=AB + BC+ CA,
Cout=A.B+C(A$\oplus B$)

Full adder circuit can be implemented with different combinations of XOR, XNOR and 2x1 multiplexer blocks. The goal of this paper is to design a high performance and low power full adder module with 8T.

Having each transistor a lower interconnection capacitance, the power consumption is reduced to a great extent. The proposed 8T full adder is based on XOR/XOR logic constructed using two

3T XOR cells and one multiplexer as shown in block diagram of Figure-2(a). Two XOR gates generate the sum and 2T multiplexer block generate Cout. The 1-bit full adder with eight transistors has been implemented and shown in Figure-2(b).The typical values of width (Wn & WP) 2.5µm & 5µm have been taken for NMOS and PMOS transistors respectively in the multiplexer block with gate length of 0.25µm.

V. SIMULATION RESULT

Reduction of power consumption provides a great improvement to an adder circuit. Power consumption issues can lead to over consumption of resources when devices are cascaded. This reduction in power would come at the expense of overall speed and increased delay.

On the basis of Tanner EDA designing tool we make the performance comparison between of area and power of CMOS full adder by 27T and TG full adder design with 2xl MUX which consist 8 transistors.

In order to compare the results of the proposed full adder circuits with the existing full adders, a wide range of experiments was carried out. Schematics are designed for all the circuits using Tanner EDA for 0.25µm technology.

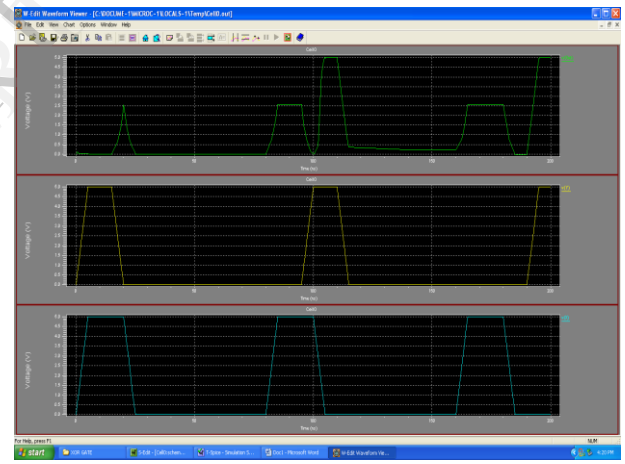


Fig5 (a) shows input results for XOR cell.

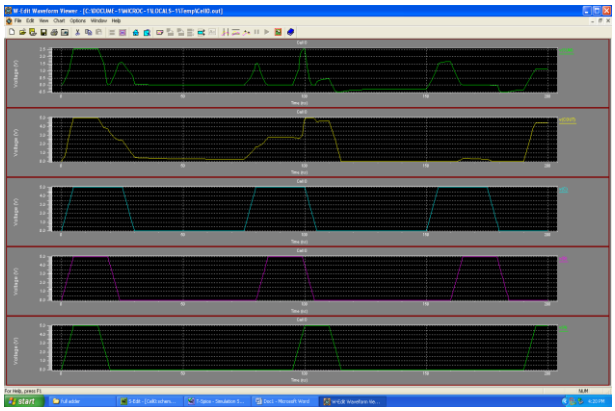
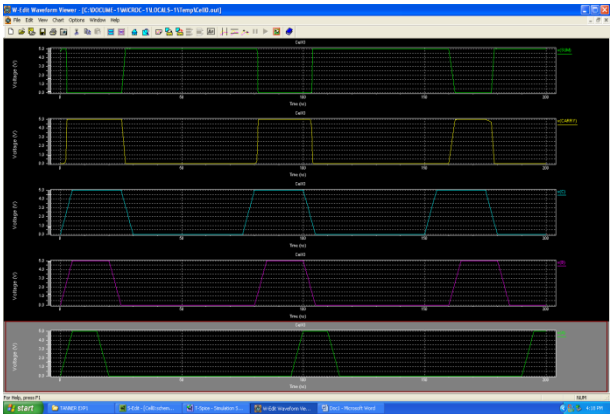


Fig5 (b) shows input and output waveform results for 8 transistor full adder

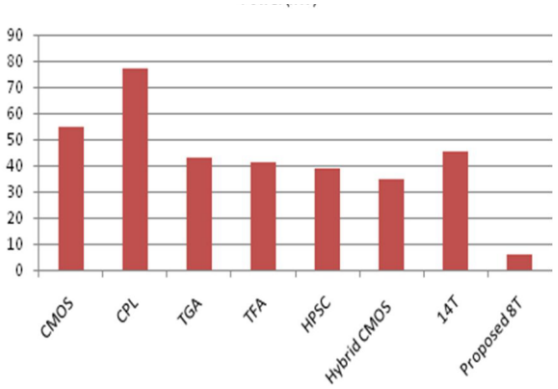


Fig(c) shows input and output waveform for Full Adder by using 27 transistors.

The XOR and full adder circuits provide full swing output voltage with respect to sizing of transistors for threshold voltage degradation. Short circuit currents are also quite low in the XOR circuit as direct path from supply to ground is eliminated. Full adder circuit have been simulated and comparisons have been presented in Table2.

Adder	No. Of Transistors	Power(μW)
CMOS	27	32.093
Proposed 8T	8	5.87

During the Tanner EDA simulation, for all the existing adders transistor width was taken as Wn = 2.5μm & Wp = 5μm with input voltage = 5V and transistor length L=0.25μm.
Graph drawn in Fig-6 shows comparison of power and delay of proposed adder circuit with other adder circuits. It has been shown that proposed adder circuit show less power consumption and delay than previously reported adders. Proposed full adder has less internal capacitance as number of transistors is reduced and gives reduced power consumption.



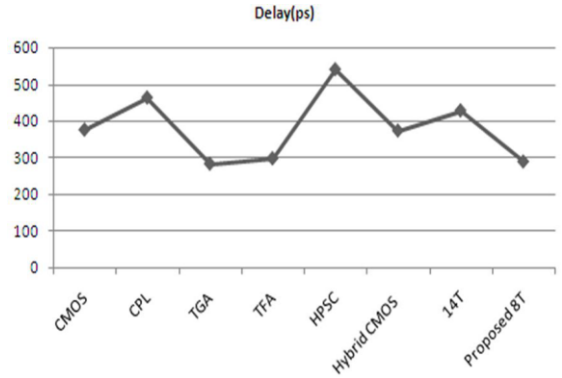


Fig-6 Comparison of (a) Power and (b) Delay for various Full adders

VI. CONCLUSION

In this paper we have represent the design and implementation of CMOS full adder using only eight transistors based on new XOR cell using fully static logic design style which is most suitable for low-energy applications. The proposed approach resulted in low power consumption and high speed compared to the existing full adder architectures. Also the realization of CMOS full adder gives even better calculation of Power Delay Product.

REFERENCES

[1]. A. M. Shams and M. Bayoumi, "Performance evaluation of 1-bit CMOS adder cells," in *Proc. IEEE ISCAS*, Orlando, FL, May 1999,vol. 1, pp. 27–30.
[2] R. Shalem, E. John, And L. K. John, "A Novel Low Power Energy Recovery Full Adder Cell," in Proc. IEEE Great Lakes VLSI Symp.,Feb. 1999, pp. 380-383.
[3] R. Zimmermann and W. Fichtner, "Low-power logic styles:CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.
[4] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," IEE Proc. Circuits Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001.
[5] N.Weste and K. Eshraghian, "Principles of CMOS VLSI design," in A System Perspective. Reading, MA: Addison-Wesley, 1993.
[6] M. Zhang, J. Gu, and C. H. Chang, "A novel hybrid pass logic with static CMOS output drive full-adder cell," in Proc. IEEE Int. Symp.Circuits Syst., May 2003, pp. 317–320.
[7] S. Goel, A. Kumar, and M. Bayoumi, "Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1320, Dec. 2006.
[8] Y.Tsividis, Mixed Analog-Digital VLSI devices andTechnology, Singapore: McGraw Hill, 1996.