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Power Efficient 4-bit Flash ADC using Cadence Virtuoso

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Abstract—Analog-to-Digital Converters (ADCs) are useful building blocks in many applications like a biomedical, data storage read channel and an optical receiver because they represent the interface between the important world analog signal and therefore the digital signal processors. During this paper, an attempt is formed to style Power efficient 4-bit Flash Analog to Digital Converter [ADC] for Biomedical applications. Moreover, this paper describes the study of sample and hold circuit, comparator and encoder in 4-bit Flash Analog to Digital Converter (ADC) to get a power efficient ADC. During this paper, R-2R ladder is replaced with sample and hold circuit to reduce the power consumption, the traditional comparator is replaced with a simple comparator and therefore the priority encoder is employed as the alternative for the traditional encoder. It's implemented using 0.18µm CMOS technology. Generally, the CADENCE VIRTUOSO tools are used for drawing the schematics and to do the simulations. The simulation results include 1.8V analog input range at a frequency of 33.20MHz.

Index Terms— Flash ADC, CADENCE VIRTUOSO, gpdk180, Resolution.

I. INTRODUCTION

In today's era due to technological advancement, there are various applications of ADC which include the range from Biomedical application to RF and Wireless communication. It is required to use analog to digital converters (ADCs) for interfacing the real-world analogue signal to the digital system. Different ADCs have been developed by altering the architecture of ADCs like pipelined, integrating, binary search, delta sigma, successive approximation and flash ADC [1]. In almost every practical application it requires to convert analog signal into digital for more precise output so, ADC plays an important role for various applications include wireless communication and digital signal processing. Moreover, various types of ADC are present including successive approximation, Flash and sigma-delta. Flash ADC's are used in various applications ranging from radar receivers, digital sampling, and LAN interface [2]. Analog to digital conversion is an electronic process that converts a voltage that varies among an infinite number of the values to a defined level [3].

Moreover, in applications such as on chip direct digitization of a wideband RF signal and digital receivers, flash architectures are often preferred [4]. Mixed-signal applications such as partial response maximum-likelihood (PRML) read channels and Gigabit Ethernet require high-speed low-resolution ADCs

which are usually implemented with the flash architecture. By their nature, these applications rely heavily on DSP, which performs best when implemented on the finest geometry CMOS process [5]. Furthermore, the precision of output plays a vital role as analog signal has more amount of noise and interference of side band signal and also it is difficult to process and analysis. Moreover, design and verification plays an important role in the output, where analog circuits are most difficult to do there compare to digital. Basically, a typical biomedical application work on 100KHz up to 5.8 GHz frequency range with SNR of 24.92 dB and SFDR of 28.42 dB with the resolution of 4-bit. The maximum power consumption is 592 µW. As an application example, the authors have proposed a bio implant to measure arterial blood pressure for patients suffering from Peripheral Artery Disease (PAD) [6]. Here, Flash ADC is used which is having a block of sample and hold circuit for converting analog input into discrete output with the help of capacitor, resistor and amplifier. The output of the comparators is like a thermometer code: the higher the input value, more comparators have their outputs high from bottom to top. A dedicated component known as "Priority Encoder" translates this code into a binary code, which corresponds to the position of the last comparator with high output, counting from the bottom to up. As the advantage is that it is very fast and it converts the code instantly.

II. DIFFERENT BLOCKS OF ADC

The analog signal is first applied to the 'sample' block where it's sampled at a selected frequency. The sample amplitude value is maintained and held within the 'hold' block. It's an analog value. The hold sample is quantized into discrete value by the 'quantize' block. At last, the 'encoder' converts the discrete amplitude into a binary number.

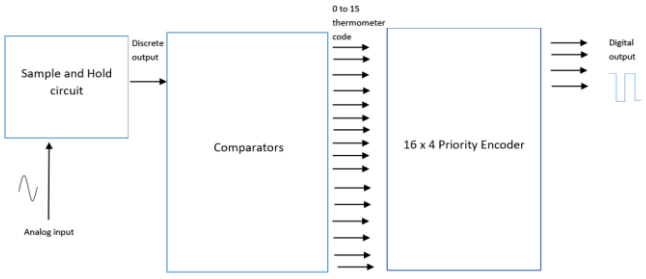

Fig. 1. Block Diagram of ADC [7]

1) Sample and Hold

During the sampling phase when the clock goes high, the input signal is sampled and the capacitor is charged to input level. During hold mode when the clock is low the sampled signal is held to constant and the capacitor discharged through same path.
So, if clk is high MOS gets on => Vout can track Vin.

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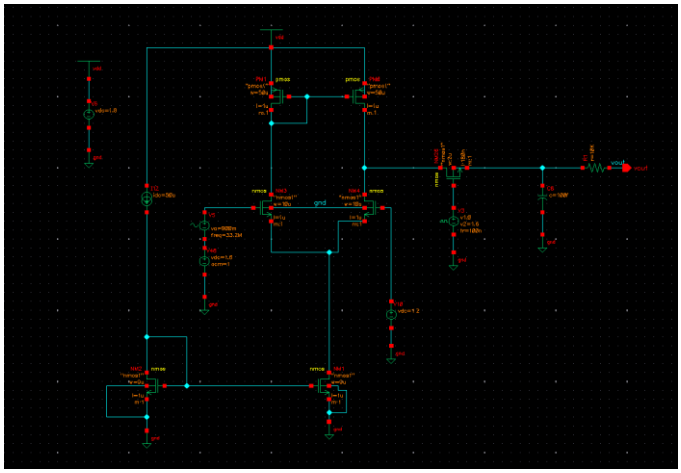

Fig. 2. Sample and Hold circuit with Amplifier

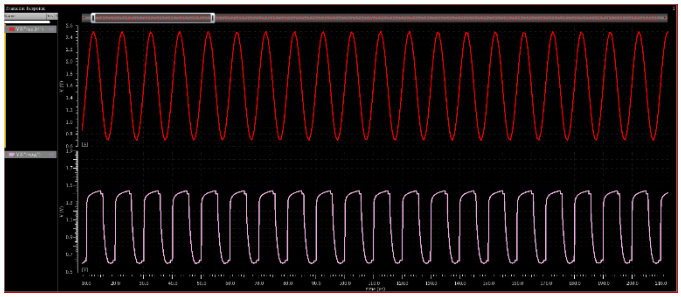

Fig. 3. Output of Sample and Hold Circuit

2) Discrete Comparator

A comparator is normally used in applications where some varying signal level is compared to a fixed voltage level (usually a voltage reference). Since it is, in effect, a 1-bit analog-to-digital converter (ADC), the comparator is a basic element in all ADCs.

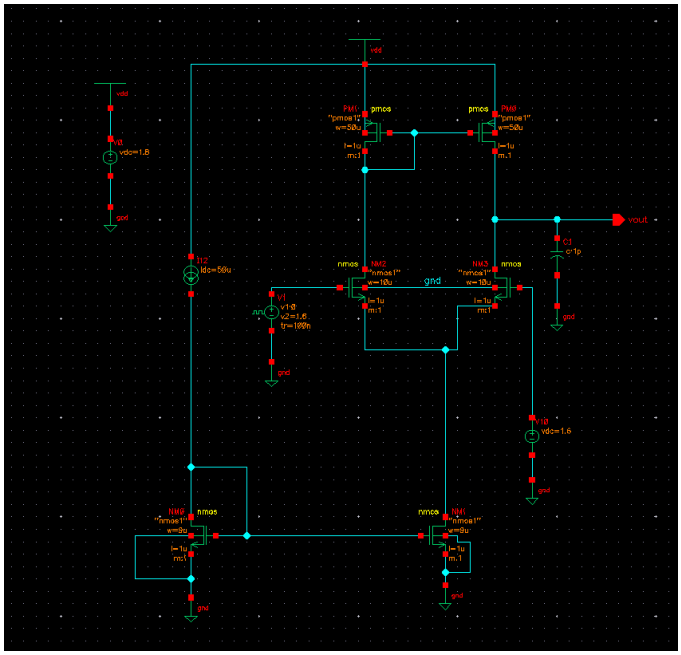

Fig. 4. Discrete Comparator

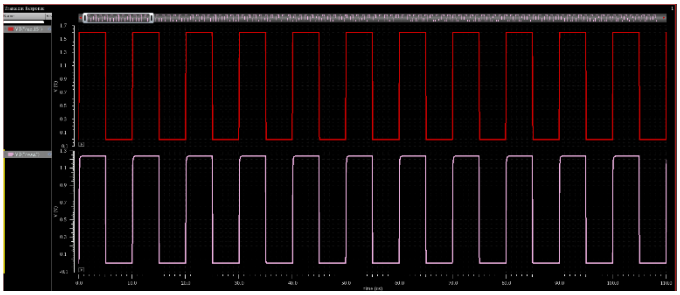

Fig. 5. Output waveform of Discrete Comparator

3) Priority Encoder

The next stage of the comparator is an encoder. At the output of the comparator stage, the produced thermometer code is converted to a binary code using the thermometer to a binary encoder. The Thermometer code generated by the TIQ (Threshold Inverting Quantization) is the unary code that represents a natural number n, with n followed by zero or (n-1) ones followed by a zero.
So, for 16 to 4 priority encoder the output equations are:

O1= D1+D3+D5+D7+D9+D11+D13+D15.
O2=D2+D3+D6+D7+D10+D11+D14+D15.
O3= D4+D5+D6+D7+D12+D113+D14+D15.
O4= D8+D9+D10+D11+D12+D13+D14+D15.

Where O1, O2, O3, O4 are the output pins and D1, D2, ..., D15 are the input pins.

The priority encoder consists of 8 input OR Gate:

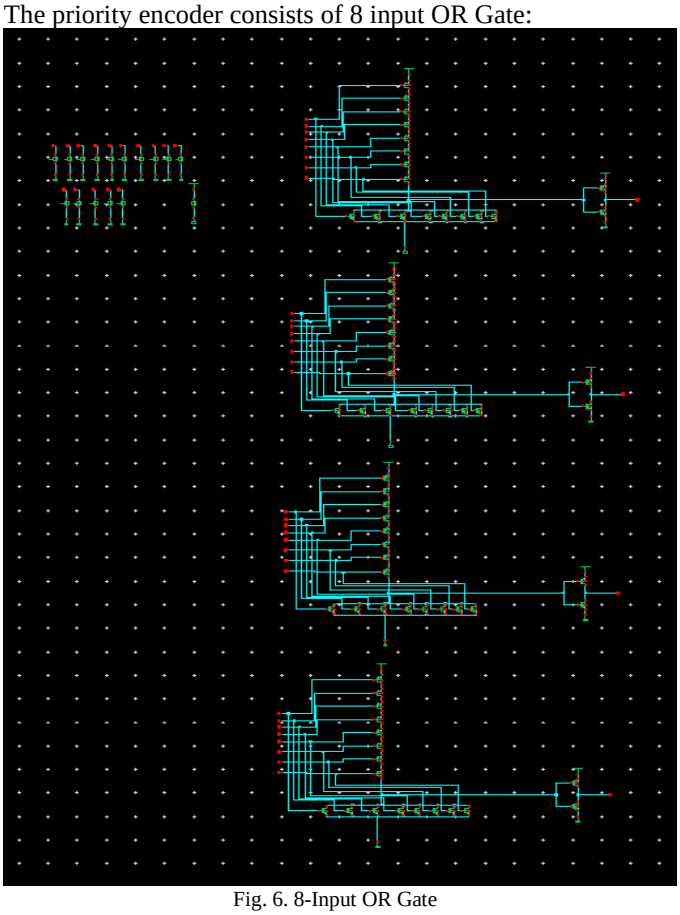

Fig. 6. 8-Input OR Gate

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III. PARAMETERS

1) Power dissipation

The process in which an electric or electronic device produces heat or other waste energy as an unwanted byproduct of its primary action.

Measured by doing DC analysis and then multiplying the output Voltage and Current we will get the amount of power which is dissipated.

2) Delay

The propagation delay of a signal path is the time taken between the change in input and the change in output for that signal. If it is not managed properly, propagation delays can result in logic circuits that run too slowly to meet their requirements, or that fail altogether.

Measured by doing Transient analysis.

3) SNR (Signal to Noise Ratio)

It is signal to noise ratio

Signal-to-Noise Ratio. This figure characterizes the ratio of the fundamental signal to the noise spectrum. The noise spectrum includes all non-fundamental spectral components in the Nyquist frequency range (sampling frequency / 2) without the DC component, the fundamental itself and the harmonics:

$$SNR = 20 * \log([Fundamental]/\sqrt{(SUM(SQR[Noise]))})$$

Also, SNR= 6.02N + 1.76 db.

By doing theoretical calculation as to put the value of N in above equation we will get the value of SNR. Moreover, by doing transient analysis and then FFT one can calculate the value of SNR.

4) SNDR (Signal to Noise + Distortion Ratio)

Signal-to-noise-and-distortion ratio (S/N+D, SINAD, or SNDR) is the ratio of the input signal amplitude to the rms sum of all other spectral components. The SNDR is dependent on the input-signal frequency and amplitude, degrading at high frequency and power.

Measured results are often presented in plots of SNDR versus frequency for a constant-amplitude input, or SNDR versus amplitude for a constant-frequency input.

5) SFDR (Spurious Free Dynamic Range)

Spurious Free Dynamic Range. The figure for spurious free dynamic range (sometimes also called only dynamic range) characterizes the ratio between the fundamental signal and the highest spurious in the spectrum [15]

Also, SFDR= 6.02* N, N is the no. of bits.

Dynamic range is calculated theoretically as well as practically by applying a sine wave input for many periods and perform an FFT analysis of the output stream. The SFDR is the difference between the signal level and the highest harmonic you see in waveform (fig. 7). The more periods you simulate the more accurate results you can have.

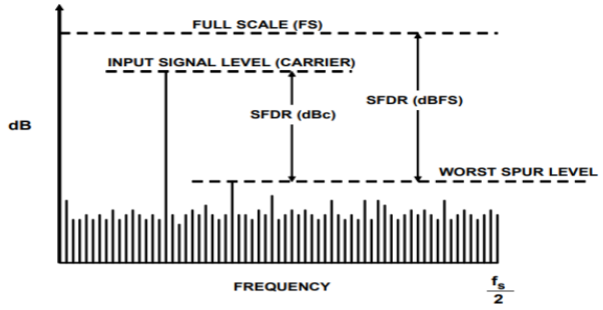

Fig. 7. SFDR waveform [15]

6) *Gain Error*

Defines as the difference of the slope of the actual output values and the ideal output values. Expressed as a percentage. Total system gain error includes any gain errors from preamplifiers, attenuators, or signal transducers.

Gain error (%) = (actual value – ideal value) %

Here, gain error = 1.8-1.6 = 0.2% error is present over here.

7) *INL (Integral Non-Linearity)*

DNL errors accumulate to produce a total Integral Non-Linearity (INL). It is defined as the maximum deviation from the ideal slope of the ADC and is measured from the center of the step. It is expressed as counts. INL is a function of each ADC's particular architecture. It is not possible to remove its effects with calibration [15].

8) *DNL (Differential Non-Linearity)*

For an ideal ADC the output is divided into 2 power in uniform steps each with the width. Any deviation from the ideal step width is the Differential Non-Linearity (DNL). It is expressed as counts. DNL is a function of each ADC's particular architecture. It is not possible to remove its effects with calibration [15].

For INL and DNL first LSB is being find:

For finding LSB:

1 LSB = Vref/(2^N). here, Vref = 1.6 and N= 4. Therefore, 1 LSB = 0.075. so, INL = amount of input in transient analysis divided by the amount of LSB.

Therefore, INL = 10m/0.075 = 0.133.

So INL = +/- 0.133 LSB.

IV. IMPLEMENTED DESIGN

In the proposed ADC design, the 4-bit low power consumption Flash ADC structure is proposed. Here, the design is working at the frequency of 33.20MHz and 1.8V input with a sample and hold circuit at the beginning to overcome the problem of power dissipation by R-2R ladder furthermore it is connected to a discrete comparator which is giving discrete output and this output is given to priority encoder as an input. Basically, the design of priority encoder is formed with OR gates instead of MUX using XOR gates to reduce the complexity and to overcome the problem of power dissipation. Along with this circuit a Low-Pass Filter is added as a low-pass filter (LPF) attenuates content above a cutoff frequency, allowing lower frequencies to pass through the filter. Moreover, an amplifier is kept at the beginning to amplify the signal or to strengthen

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the signal so that the amount of noise reduces and then this AC signal is passed to S/H circuit for further process.

As, n-bit ADC requires (2^n)-1 comparators; 4-bit ADC requires 15 comparators whose input is the output of sample and hold circuit and the output is given to 8 input OR gate for getting the digital output from the discrete input.

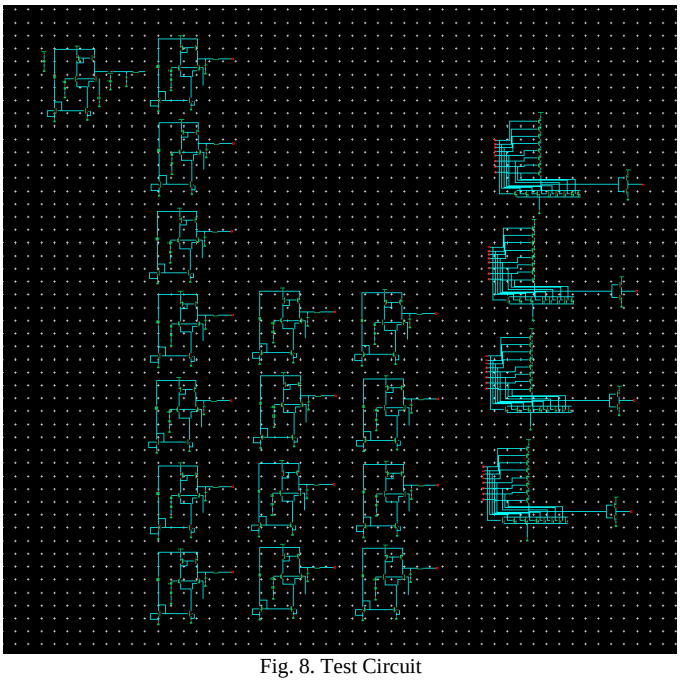

Fig. 8. Test Circuit

V. RESULT AND DISCUSSION

Here, 4-bit ADC is being prepared with an input voltage of 1.8V, moreover frequency is taken as 33.20MHz which will fulfill the aspect of Biomedical application. The power dissipation is quite low compared to [1] & [8] that is 2.88mW due to the usage of sample and hold circuit instead of R-2R ladder and also using OR gate instead rather than MUX in Encoder. SNR, SNDR, SFDR has the values 25.846 dB, 25.842 dB, 24.08 dB respectively. The value of SNR and SNDR are high compared to [1] & [8] as a low pass filter is used in this prepared circuit instead of a normal circuit so the signal has less distortion and we had greater values whereas, SFDR required less value so here also it is fulfilling the aspect as the harmonics are less due to low pass filter and OR gates in the circuit noise is very less. But at the cost of speed, because for maintaining other aspects delay increases over here with 12.9ns. Furthermore, taking each block into consideration the power dissipation of S/H circuit, Comparator and Priority encoder is 2.78mW, 90uW and 124.9pW respectively. The INL and DNL are +/- 0.133LSB each with the gain error of 0.2%.

TABLE I. Comparison of results

Parameters	This work	[1]	[8]
Frequency(Hz)	**33.20M**	33.20M	970M
Technology	180nm	180nm	180nm
Vdd(V)	1.8	1.8	1.8
Resolution	4-bit	4-bit	4-bit
Power dissipation(W)	**2.88 m**	4.51 m	42 m
Delay(ns)	12.9	4.83	24.266
P.D.P	3.71 * 10^ (-11)	-	-
SNR(dB)	**25.846**	25.2	-
SNDR(dB)	**25.842**	23.3	25.3
SFDR(dB)	**24.08**	30.1	37.3
Gain Error(%)	**0.2**	-	-
INL(LSB)	**+/- 0.133**	+/- 0.6	+/- 0.06
DNL(LSB)	**+/- 0.133**	+/- 0.25	+/- 0.04
P.D (sample and hold)	**2.78mW**	0.85mW	37.5mW
P.D (Comparator)	**9 * 10^ (-5) W**	2.88mW	2.5mW
P.D (Encoder)	**1.249 * 10^ (-10)**	0.78 mW	2mW

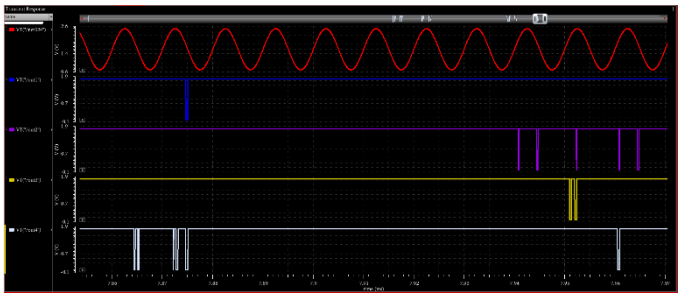

Fig. 9. Output Waveform

POWER DISSIPATION

In [1] & [8] R-2R ladder is used which is the main caused of power dissipation. R-2R ladder is replaced with the sample and hold circuit which is used here because due of R-2R ladder power consumption is more and delay increases; to overcome that problem sample and hold circuit is used. So, here instead of R-2R ladder sample and hold circuit is used. Moreover, by using complex priority encoder in the paper [1] with MUX and gates, here simple OR gates are used which also plays a major role for reduction of power consumption.

SNR (Signal to Noise Ratio)

A higher SNR value means that the signal strength is stronger in relation to the noise levels, which allows higher data rates and fewer retransmissions – all of which offers better throughput. Higher numbers generally mean a better specification, since there is more useful information (the signal) than there is unwanted data (the noise).

Here, the SNR value is higher due to structure of the circuit as low-pass filter is added, moreover it will strengthen the signal and decrease the value of Noise. So, in this paper instead of using simple circuit, by adding low-pass filter SNR value is more than the [1] & [8].

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SNDR (Signal to Noise and Distortion Ratio)

Similar to SNR, there is another indicator called SNDR. It indicates the ratio of Total energy (Wanted + Unwanted) and Unwanted power. Since the numerator is the total power in the definition, the value in dB is always positive.
As according to SNR, low pass filter is used to strengthen the signal: wanted component has higher ratio compared to unwanted components.
So, here in this paper instead of using simple circuit in reference paper, by adding low-pass filter SNDR value is more than the compared [1] & [8].

SFDR (Spurious Free Dynamic Range)

Dynamic range (dB) = 20 * log(VLSB/Vrange) = 20 * log(2^n)

OR

SFDR= 6.02* N, N is the no. of bits.

Spurious-free dynamic range (SFDR) is the strength ratio of the fundamental signal to the strongest spurious signal in the output.
SFDR is defined as the ratio of the RMS value of the carrier wave (maximum signal component) at the input of the ADC to the RMS value of the next largest noise or harmonic distortion component which is referred to as "spurious" at its output. SFDR is usually measured in dBc (i.e. with respect to the carrier signal amplitude).
Here, as the harmonics are not high compared to the reference paper we are getting low SFDR, again with the help of low pass filter and using simple or gates the harmonics are very less so SFDR is low compared to [1] & [8].

CONCLUSION

The proposed work presents a highly digital 4-bit flash ADC whose major parts are synthesizable, reducing the design efforts, time-to-market and power requirement, it's scalable with the technology. Having an application of Biomedical aspect whose range is from 100KHz to 5.8GHz. Here, the frequency is taken as 33.2MHz because it comes under the specific range of biomedical application, this particular ADC is employed for that application. The SNDR, SNR and SFDR are capable 25.842 dB, 25.246 dB and 24.08 dB, respectively. The DNL of this 4-bit flash ADC is ± 0.133 LSB and INL is ± 0.133 LSB. The sample and hold circuit, comparator and Thermometer to code converter is meant and simulated in CADENCE virtuoso tool using 180 nm CMOS technologies. The varied analysis like DC and transient analysis are performed for above said functional blocks with the assistance of CADENCE tool. The proposed circuit has the entire propagation delay of 12.9ns and with power dissipation of 2.88mW. Moreover, the Gain Error is 0.2%, whereas the power dissipation of every block i.e. of Sample and Hold circuit, Comparator, Priority Encoder is 2.78mW, 90uW, 1.249*10^ (-10) W, respectively. The flash ADC is functioning as per the specifications. Moreover, various techniques of comparator like TIQ comparator based ADC can be used to further analysis.
Furthermore, another solution is to perform digital signal processing on the output of ADC to correct offset, gain and linearity of output. In flash ADC there is a thermometer code-to-binary code encoder, one can even use another technique known as quantum voltage (QV). With the help of some above mentioned techniques ADC can be implemented again for better results.

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