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Power and Delay Optimization of 8-Bit ALU using Various Techniques

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Abstract: **The Arithmetic Logic Unit (ALU) is used in many applications such as Digital image processing, microprocessors and Digital Signal Processing. In this paper we designed the 8-bit ALU by using various Techniques like CMOS, TG (Transmission Gate), GDI (Gate Diffusion Input), M-GDI (Modified Gate Diffusion Input), FS- GDI (Full Swing Gate Diffusion Input) Techniques and compare the power, delay and power delay product of 8-bit ALU by using the mentor graphics tool with 90nm CMOS technology with the minimum supply voltage of 1.2V and frequency of 125Mhz.**

Keywords: CMOS, Transmission gates (TG), Gate Diffusion Input (GDI), Modified Gate Diffusion Input (M-GDI), Full Swing Gate Diffusion Input (FS-GDI).

I. INTRODUCTION

An Arithmetic Logic Unit (ALU) is brain of the Central Processing Unit (CPU), which accomplish Arithmetic functions like addition, subtraction, multiplication, division and logical functions like AND, OR, XOR etc. To design an ALU full adder plays an important role which performs arithmetic operations. If there is any change in full adder then there is automatic improvement in the ALU. Power consumption and Delay are the major issues in electronics industry which triggered research efforts to reduce the Power consumption and Delay of the VLSI circuits, there is only a limited amount of power available for portable electronic devices widely used on daily basis, these electronic devices are high speed low power VLSI circuits works simultaneously. Gate Diffusion Input Techniques (GDI, M-GDI, and FS-GDI) was introduced a promising alternative to static CMOS logic and Transmission Gate logic. GDI Techniques reduces transistors count, Power and Delay issues of VLSI circuits.

II. LITERATURE SURVEY

A large body of investigation has been performed to expand and advance conventional Complementary Metal Oxide Semiconductor (CMOS) techniques for the fabrication of ULTRA low power integrated circuits (ICs). The purpose of this study is to expand a faster, lower power, and reduced area substitute to standard CMOS logic circuits. M-GDI technique is one such new technique for minimization of powerconsumption in the digital circuit design field.

Power dissipation becomes most important restriction in high performance applications. Optimizations for basic logic gates are fundamental constraint in order to get better the performance of a variety of low power and high-performance devices. Morgenshtein et al. investigated a high-speed and multipurpose logic style for low power electronics design, known as Gate Diffusion Input (GDI), with reduced area and power necessities, and proficient of implementing a broad variety of logic functions.

The arithmetic logic unit (ALU) is the core of a CPU in a computer. The adder cell is the elementary unit of an ALU. The constraints the adder has to satisfy are area, power and speed requirements. Some of the conventional types of adders are ripple- carry adder, carry-look ahead adder, carry-skip adder and Manchester carry chain adder.

III. EXISTING TECHNIQUES

1.1 CMOS Logic

CMOS or Complementary Metal Oxide Semiconductor is a combination of NMOS and PMOS transistors that operates under the applied electrical field. The structure of CMOS was initially developed for high density and low power logic gates. The NMOS and PMOS are the types of Metal Oxide Semiconductor Field Effect Transistors (MOSFET). The CMOS transistors are used in various applications, such as amplifiers, switching circuits, logic circuits, Integrated circuit chips, microprocessors, etc. The importance of CMOS in semiconductor technology is its low power dissipation and low operating currents. Its manufacturing requires fewer steps as compared to the Bipolar Junction transistors.

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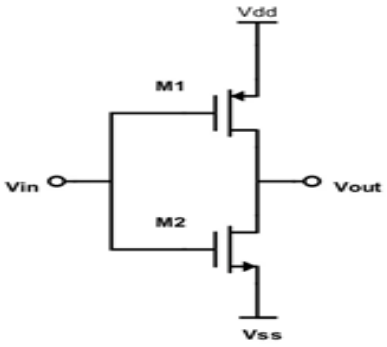

Fig. 1: CMOS Cell

1.2 Transmission Gate Logic

Transmission gate (TG) is a complementary switch constructed by CMOS pair. CMOS pair serves as a switch in case of transmission gates. There are two types of transistors in TG. They are NMOS transistor and PMOS transistor connected back-to-back. Both the PMOS as well as the NMOS transistors becomes switched on or off concurrently. The N-type MOS transistor gives a terrific active low signal "0" but a poor active high signal "1". Similarly, the P- type MOS transistor provides an excessive active high "1" but a bad active low signal "0" (Priyadharshini Shanmuga Sundaram et al. 2011 and Michael H. Schulz et al. 1989).

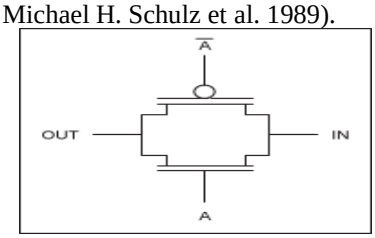

Fig. 2: Schematic representation of a Transmission Gate

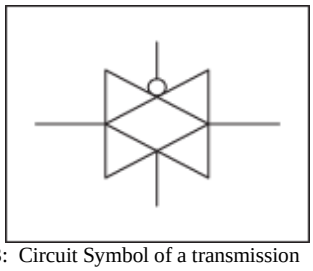

Fig. 3: Circuit Symbol of a transmission gate

1.3 GDI Logic

Gate diffusion input is a new Technique of reducing power dissipation, area and delay and achieving high speed and high performance. The combinational circuits also implemented by using this technique. So that, the total circuit area reduction and power reduction is achieved. GDI Technique is a two-transistor designing technique, using which the complex logic and arithmetic functions can be determined. In first look GDI cell similar to CMOS inverter but GDI cell consists of 3 inputs – G (common gate input of PMOS and NMOS), P (input to drain/source of PMOS) and N (input to drain/source of NMOS). Bulks of both PMOS and NMOS are attached to their diffusion P, N to reduce bulk effect [8]. GDI cell decreases both gate leakage current and subthreshold leakage current as compared to traditional CMOS but its performance depreciates when used in and below 90nm technology. Fabrication of basic GDI cell is not possible in traditional p well progression. When substrate attached to drain, threshold voltage is increased and when the substrate is attached to source, body effect is destroyed.

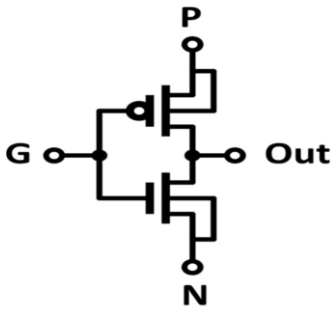

Fig. 4: GDI Cell

1.4 M-GDI Logic

MGDI is a new technique for designing low power digital circuits. This technique is adopted from GDI technique. MGDI technique is used to reduce power dissipation, transistor count and area of digital circuits. MGDI also consists of three input terminals - G, (input of both PMOS and NMOS) P, (input to drain/source of PMOS) and N (input to drain /source of NMOS) except the bulks of PMOS (SP) and NMOS (SN) are constantly coupled to VDD and GND, MGDI overcomes the drawbacks of GDI cell [9]. With technology scaling, the influence of source body voltage on transistor threshold voltage gets exceeding a bridged i.e., the linearized body coefficient. On varying the values of G, P, N, SP and SN in MGDI cell, SP and SN will remain constantly coupled to VDD and GND CMOS it requires 6 transistors.

The main advantage of MGDI technique is that it reduces transistor counts and area on chip that's cause of low power consumptions. So, it is easy to design complex circuits using MGDI technique. The basic primitive of GDI cell consists of NMOS and PMOS containing four terminals G (common gate input of NMOS and PMOS transistors), P (the outer diffusion node of PMOS transistor), N (the outer diffusion node of MOS transistor), and D (common diffusion node of both transistors).In this work a modified primitive GDI logic gates have been implemented in 0.250µm technology and it is compared with existing GDI and CMOS logic. Fig 1 shows the construction of modified GDI basic gates of AND, OR, NOR, NAND, XOR, XNOR and MUX The modified GDI primitive cells are constructed and its significant variation between CMOS and conventional GDI are compared..

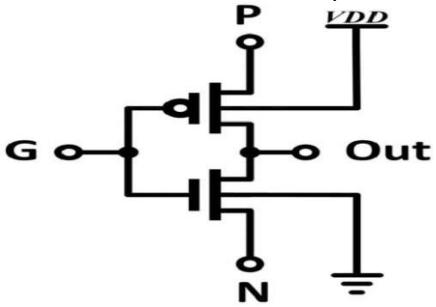

Fig. 5: Basic M-GDI cell

IV. PROPOSED DESIGN

Full swing GDI (FS-GDI) technique is utilized to reduce power consumption and delay. Full swing GDI technique gives better speed of operation as compared to CMOS technique.

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While keeping these parameters at best GDI maintains low complexity of design [10]. Full-swing GDI cells proposed to improve the output swing of GDI gates as an alternative for swing restoration buffers, a swing restoration transistor used to improve the output swing of F1 and F2 gates. F1 and F2 are universal gates similar to NAND and NOR gates as shown in Fig. 3. Using this technique full swing output can be achieved at the expense of increasing transistor count compared tomodified-GDI gates, but when compared to CMOS and PTL implementations FS gates uses fewer transistors hence power consumption and area of VLSI circuits are reduced.

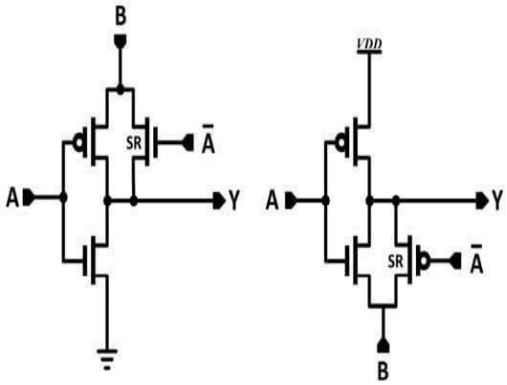

Fig. 6: Basic FS-GDI cell

V. IMPLEMENTATION

In this the Full-Swing GDI technique is used to realize the circuits required todesign the ALU as follows:

A. 2x1 Multiplexer

A multiplexer is a digital switch chooses the output form several inputs basedon a select signal, shown in figure. 2x1 multiplexer consists of 6 transistors.

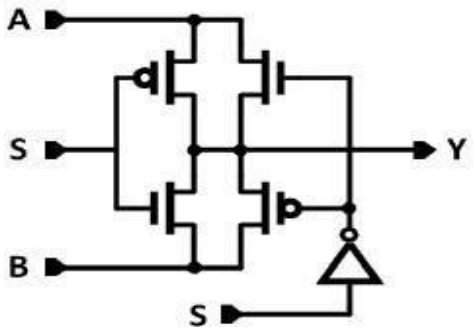

Fig. 7: FS-GDI Based 2X1 MUX

B. 4x1 Multiplexer

Using the previously discussed 2x1 multiplexer a 4x1 multiplexer realized as shown in Fig. consists only of 16 transistors.

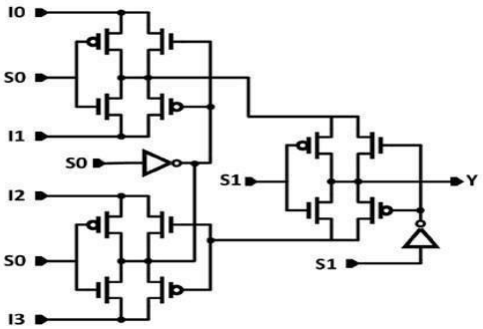

Fig. 8: FS-GDI Based 4X1 MUX

C. Full Adder

A full adder is a combinational circuit that performs the arithmetic sum of three input bits. It consists of three inputs and two outputs. The adder cell used in this design realized using full-swing AND, OR, and XOR gates. This design was chosen among 3 designs to maintain low power operation, it has the lowest delay among the three designs, and with some modifications it performs the logic operations as well, these modifications will save large area of the ALU design.

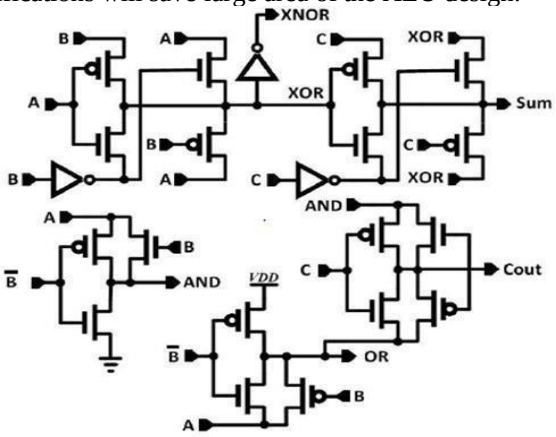

Fig. 9: FS-GDI Based Full Adder

D. Arithmetic Logic Unit

An ALU is a key component in the Central Processing Unit (CPU) of any computer; even the simplest microprocessors contain one. It performs arithmetic operations such as addition, subtraction, increment, decrement and logic operations such as AND, OR, XOR and XNOR. The proposed design of the 4-Bit ALU consists of 4 stages, each stage is an 1-Bit ALU realized using the previously discussed circuitsas follows. Each 1-Bit ALU stage consists of two 2x1 multiplexers, two 4x1 multiplexers and one full adder cell, this design requires 48 transistors as depicted in Fig. Any desired operation can be performed based on the selection line S0, S1, S2 code; Table II summarizes the truth table of the proposed ALU.

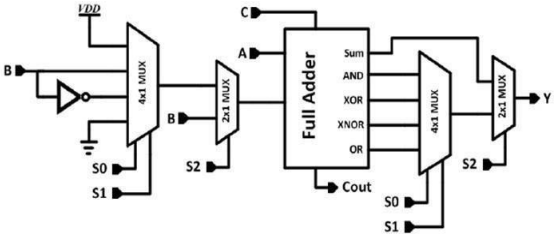

Fig. 10: FS-GDI Based 1-Bit ALU

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VI. SIMULATION RESULT

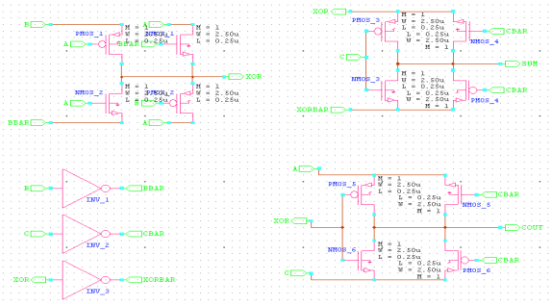

Fig. 11: Schematic for FS-GDI based FULL ADDER

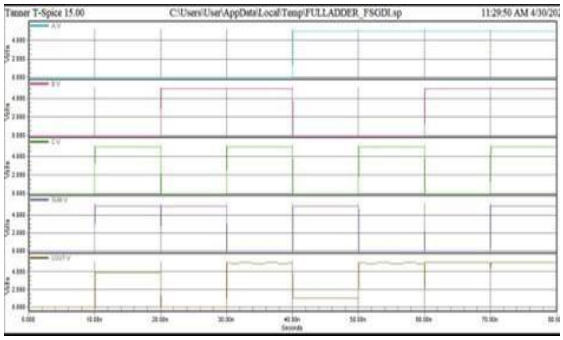

Fig. 12: FS-GDI based FULL ADDER Output Waveform

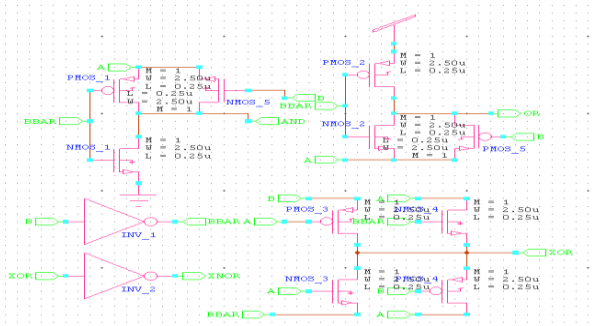

Fig. 13: Schematic for FS-GDI based LOGIC BLOCKS

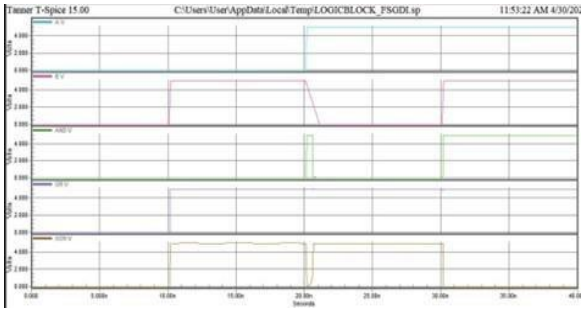

Fig. 14: FS-GDI based LOGIC BLOCKS Output Waveform

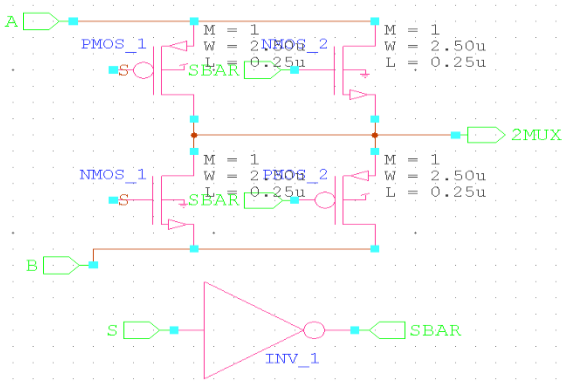

Fig. 15: Schematic for FS-GDI based 2X1 MULTIPLEXER

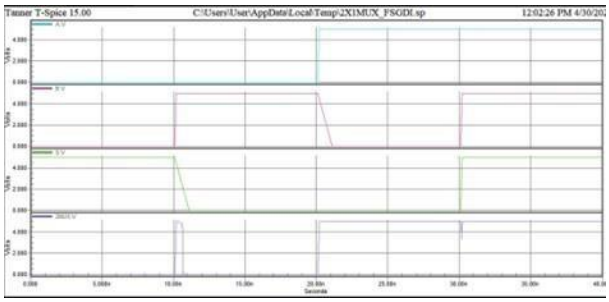

Fig. 16: FS-GDI based 2X1 MULTIPLEXER Output Waveform

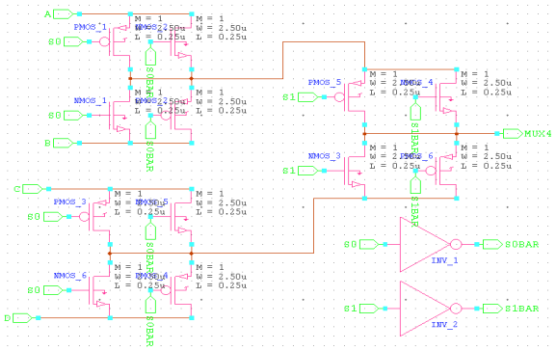

Fig. 17: Schematic for FS-GDI based 4X1 MULTIPLEXER

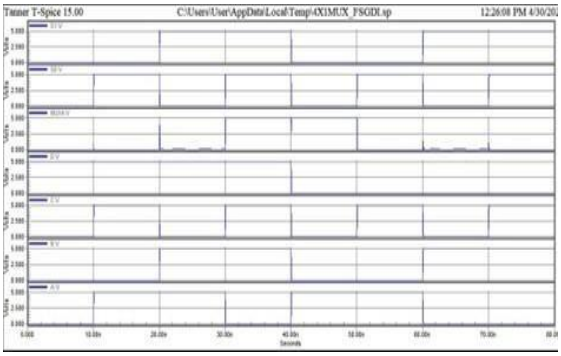

Fig. 18: FS-GDI based 4X1 MULTIPLEXER Output Waveform

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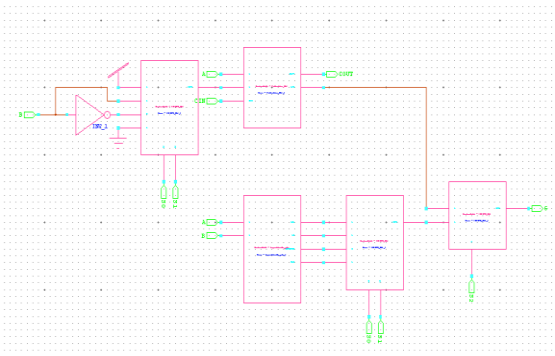

Fig. 19: Schematic for FS-GDI based 1 BIT ALU

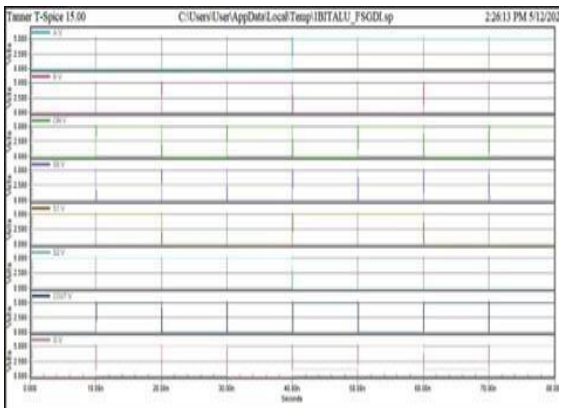

Fig. 20:FS-GDI based 1 BIT ALU Output Waveform

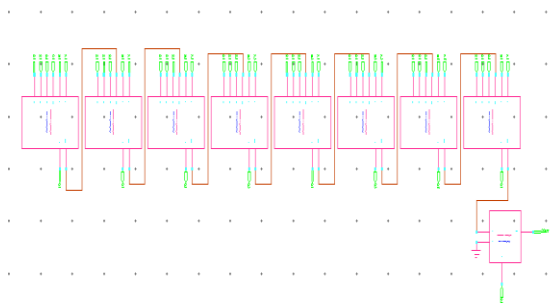

Fig. 21: Schematic for FS-GDI based 8 BIT ALU

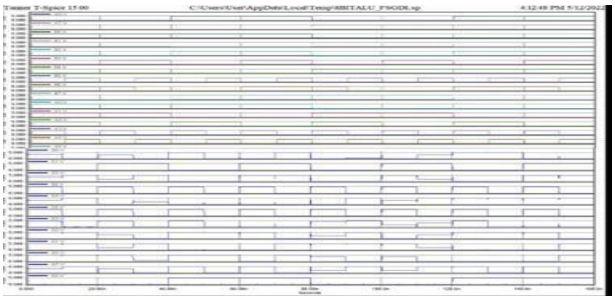

Fig. 22: FS-GDI based 8 BIT ALU Output Waveform

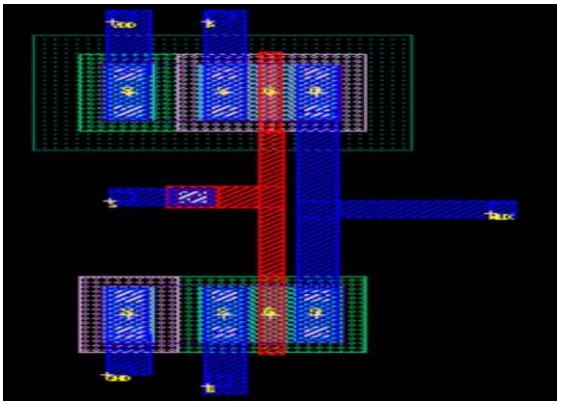

Fig. 23: Layout for FS-GDI based 2X1 MULTIPLEXER

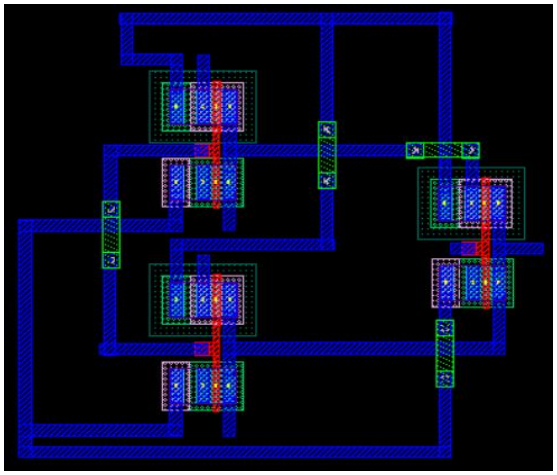

Fig. 24: Layout for FS-GDI based 4X1 MULTIPLEXER

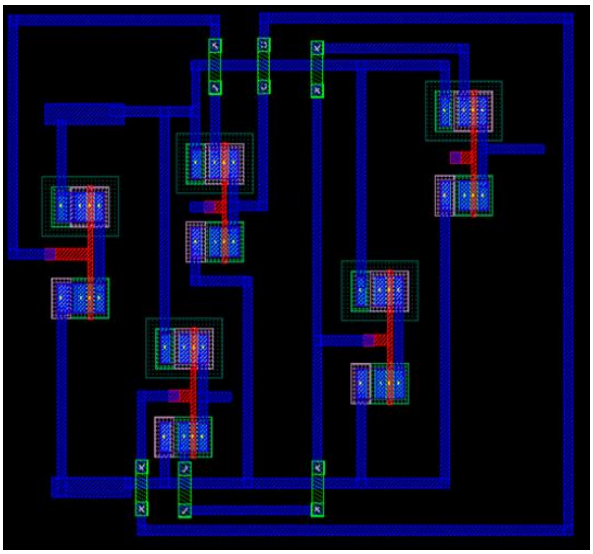

Fig. 25: Layout for FS-GDI based FULL ADDER

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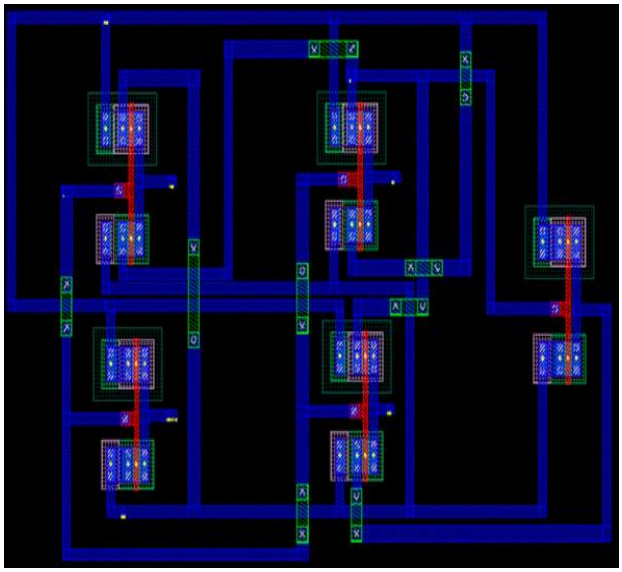

Fig. 26: Layout for FS-GDI based LOGIC BLOCKS

Table 1: Comparison of Different Techniques 250nm Technology

Technology	Number of transistors	Power consumption	Delay	Power delay product
CMOS LOGIC	648	95.511×10^{-6}	120.25×10^{-12}	0.0114×10^{-6}
TG LOGIC	400	50.158×10^{-6}	106.28×10^{-12}	0.0531×10^{-6}
GDI LOGIC	372	48.153×10^{-6}	185.36×10^{-12}	8.9083×10^{-6}
M-GDI LOGIC	288	30.001×10^{-6}	0.04638×10^{-12}	1.3890×10^{-6}
FS-GDI LOGIC	448	46.916×10^{-6}	0.03383×10^{-12}	0.0154×10^{-6}

Table 2: Comparison of Different Techniques for 90nm Technology

Technology	Number of transistors	Power consumption	Delay	Power delay product
CMOS LOGIC	648	67.62×10^{-6}	94.42×10^{-12}	0.0635×10^{-6}
TG LOGIC	400	34.86×10^{-6}	82.35×10^{-12}	0.0285×10^{-6}
GDI LOGIC	372	32.45×10^{-6}	110.58×10^{-12}	3.5695×10^{-6}
MGDI LOGIC	288	16.51×10^{-6}	0.0083×10^{-12}	0.0013×10^{-6}
FSGDI LOGIC	448	12.23×10^{-6}	0.0054×10^{-12}	0.0066×10^{-6}

VII. CONCLUSION

This work presents an 8-Bit ALU designed in TSMC 90nm CMOS process using the GDI, Modified GDI, Full-Swing GDI technique, Transmission Gate technique and simulated using the Tanner EDA tool. Simulation results showed an advantage of the proposed ALU design in terms of power consumption and transistor count, while maintaining Full-Swing Operation and as well as Transmission Gate. The proposed FS-GDI provide better results compare to existing techniques. It consists of 448 transistors and operates under 5V supply voltage.

REFERENCES

[1] Vivechana Dubey, Ravimohan Sairam, “An Arithmetic and Logic Unit Optimized for Area and power” IEEE Fourth International Conference on Advanced Computing & Communication Technologies.,pp.330-334, 2014.

[2] G. Sree Reddy, K. V. KoteswaraRao,“32-Bit Arithmetic and Logic Unit Design With Optimized Area and Less Power Consumption By Using GDI Technique” International Journal of Research In Computer Applications and Robotics, Vol.3 Issue.4, pp. 51-66, April 2015.

[3] Hee-sup Song, Jin-Ku Kang, “A CMOS adiabatic logic for low power circuit design”,Proceedings of 2004 IEEE Asia-Pacific Conference on Advanced System Integrated Circuits 2004., pp.348,351, 4-5 Aug. 2004. doi: 10.1109/APASIC.2004.1349493.

[4] Vojin G. Oklobdßzija, Fellow, IEEE, Dragan Maksimovi´c, Member, IEEE, andFengcheng Lin” Pass-Transistor Adiabatic Logic Using Single Power-Clock Supply” Ieee transactions on circuits and systems-II:analog and digital signal processing,vol.44,no.10,October 1997

[5] Junyoung Park, Sung Je Hong, Jong Kim, “Energy-saving design technique achieved by latched pass-transistor adiabatic logic”, IEEE International Symposium in Circuits and Systems, 2005. ISCAS 2005., Vol. 5, pp.4693-4696 23-26 May 2005. doi: 10.1109/ISCAS.2005.1465680.

[6] Robert C. Chang, Po-Chung Hung, Hsin-Lei Lin, “Low Power Energy Recovery Complementary Pass-Transistor Logic”, Journal of Circuits, Systems, and Computers Vol. 15, No. 4, pp.491–504, 2006.

[7] A. Morgenshtein, I. Shwartz, and A. Fish, “Gate Diffusion Input (GDI) logic in standard CMOS Nanoscale process”, 2010 IEEE 26th Convention of Electrical and Electronics Engineers in Israel, 2010.

[8] A. Morgenshtein, A. Fish, and I. Wagner, “Gate-diffusion input (GDI): a power- efficient method for digital combinatorial circuits”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems IEEE Trans. VLSI Syst., vol. 10, no. 5, pp. 566–581, 2002.

[9] Shubham Sarkar, Hijal Chatterjee, PritamSaha, Manoj Biswas proposed “8- Bit ALU Designusing m-GDI Technique”, Proceedings of the Fourth International Conference on Trends in Electronics and Informatics (ICOEI 2020) IEEE Xplore Part Number: CFP20J32-ART; ISBN: 978-1-7281-5518-0, 978-1-7281-5518- 0/20 2020 IEEE.

[10] A. Morgenshtein, V. Yuzhaninov, A. Kovshilovsky, and A. Fish, "Fullswing gate diffusion input logic—Case-study of low-power CLA adder design", Integration, the VLSI Journal, vol. 47, no. 1, pp. 62–70, Jan. 2014.

[11] Mahmoud Aymen Ahmed1 , M. A. Mohamed El-Bendary2 , Fathy Z. Amer3 , Said M. Singy4 “Delay Optimization of 4-Bit ALU Designed in FS-GDI Technique”, 2019 International Conference on Innovative Trends in Computer Engineering (ITCE’2019), Aswan, Egypt, 2-4 February 2019, 978-1-5386-5261- 9/19 2019 IEEE.

[12] Robert C. Chang, Po-Chung Hung, Hsin-Lei Lin, “Low Power Energy Recovery Complementary Pass-Transistor Logic”, Journal of Circuits, Systems, and Computers Vol. 15, No. 4, pp.491–504, 2006.

[13] Mahmoud Aymen Ahmed,M. A. Abdelghany proposed “Low Power 4-Bit Arithmetic Logic Unit Using Full-Swing GDI Technique”, 2018 International Conference on Innovative Trends in Computer Engineering (ITCE 2018), Aswan University, Egypt, 978-1-5386-0879-1/18 2018 IEEE.

[14] M. Shoba, R. Nakkeeran, "GDI based full adders for energy efficient arithmetic applications", Engineering Science and Technology, an International Journal, vol.19, no. 1, pp. 485–496, Mar. 2016.

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