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Photovoltaic Integrated Switched-Capacitor Seven level Inverter with Minimal Switch Configuration

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***Abstract* - Increasing the voltage of low-voltage energy sources such as photovoltaic (PV) systems, fuel cells, and battery storage units is a critical requirement in modern power conversion systems, particularly for grid-connected and high-power applications. Multilevel inverters with voltage-boosting capability offer an effective solution by improving output voltage quality while reducing filter size and harmonic distortion. In this work, a new single-phase seven-level switched-capacitor (SC) inverter topology is presented, which achieves voltage boosting with a reduced number of power semiconductor devices and simplified control. The proposed inverter utilizes a single PV DC source and only eight switches to generate a seven-level AC output with a voltage boost gain of three. By employing a switched-capacitor configuration, the inverter is capable of charging and discharging the capacitors in a controlled manner, enabling inherent self-voltage balancing without the need for additional sensors, balancing circuits, or complex control algorithms. Unlike conventional multilevel inverters, the proposed topology does not require a back-end H-bridge in which switches are subjected to the full peak output voltage. As a result, the voltage stress across all switches is limited to less than half of the peak load voltage, improving device reliability and allowing the use of lower rated switches.**

Furthermore, the reduced switch count and elimination of auxiliary balancing circuits lead to lower conduction and switching losses, improved overall efficiency, and reduced system cost. The operating principle and performance of the proposed inverter are verified through detailed simulations carried out in the MATLAB/Simulink environment. Simulation results confirm the capability of the inverter to produce a stable seven-level output voltage with effective voltage boosting and balanced capacitor voltages, demonstrating its suitability for PV and other renewable energy applications

Keywords - PV, Switched Capacitor, Single carrier Sinusoidal pulse width Modulation, Multilevel Inverter, Total Harmonic Distortion

I. INTRODUCTION

Multilevel inverters (MLIs) are widely used for power conversion in renewable energy systems such as photovoltaic (PV) arrays, wind turbines, and fuel cells due to their high voltage capability, reduced switch voltage stress, lower dv/dt, and improved output voltage quality with low harmonic distortion. Conventional MLI topologies include neutral-point-clamped (NPC), flying-capacitor (FC), and cascaded H-bridge (CHB) inverters. However, increasing the number of output voltage levels in these structures significantly increases the number of clamping diodes, flying capacitors, or isolated DC sources, resulting in higher cost, larger size, and complex control. In particular, NPC and FC inverters require additional balancing circuits and sophisticated control methods to maintain capacitor voltage balance. To achieve higher AC output voltage, conventional MLIs often employ front-end DC DC converters or bulky transformers, which further increase system complexity and cost. Switched-capacitor-based multilevel inverters (SCMLIs) have emerged as an effective alternative to overcome these drawbacks. SCMLIs use capacitors to boost the input voltage and generate multiple voltage levels without inductors or transformers, while offering inherent capacitor voltage self balancing and improved efficiency.

Despite these benefits, existing SCMLIs still face limitations such as the need for multiple DC sources, the use of back-end H-bridges with high voltage stress on switches, or increased switch and capacitor count as voltage levels increase. In addition, many reported SCMLIs provide limited voltage boost or require higher rated switches. These challenges emphasize the need for a compact SCMLI topology that delivers higher voltage gain with fewer components and reduced voltage stress. The growing demand for efficient and compact power conversion systems in renewable energy applications has led to increased interest in multilevel inverter (MLI) topologies. Among these, the seven-level boost inverter has emerged as an attractive solution for photovoltaic (PV) based power generation systems due to its ability to achieve voltage boosting and high-quality output with reduced component count. Since PV sources inherently produce low and variable DC voltage, conventional systems often require an additional DC–DC boost converter, which increases system complexity, cost, and losses.

A PV-sourced seven-level boost inverter overcomes these limitations by integrating voltage boosting and DC–AC conversion within a single power stage using switched capacitor or hybrid boosting techniques. By appropriately charging and discharging capacitors during different switching states, the inverter generates multiple voltage levels with an output voltage significantly higher than the PV input. This eliminates the need for bulky transformers or separate boost converters, improving overall efficiency and power density.

Figure 1 The block diagram illustrates a multifunctional power conversion system based on a proposed 7-level switched-capacitor multilevel inverter (SC-MLI) used to interface multiple energy sources and loads. Renewable and storage

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sources such as solar PV, battery storage, and fuel cell are connected to the input of the SC-MLI. The inverter efficiently combines these DC sources and performs voltage boosting and multilevel AC generation without requiring an additional DC–DC converter.

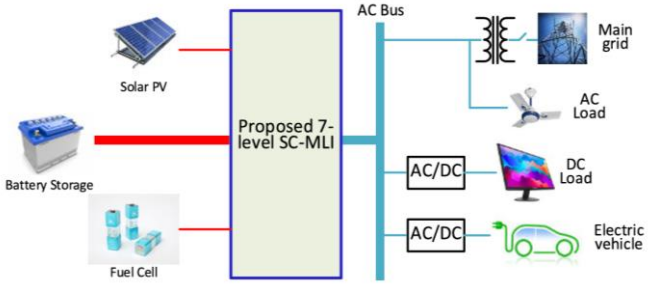

Figure 1: The block diagram of the proposed SC-MLI is used to interface various sources and loads.

II. PROPOSED TOPOLOGY

A. Description of the Proposed SC Based 7-Level MLI

The Figure 2 shows proposed block diagram represents a PV-fed multilevel inverter system with MPPT control. The PV source generates DC power, and its voltage (Vpv) and current (Ipv) are continuously sensed. These signals are fed to the Perturb and Observe (P&O) based MPPT block, which determines the reference voltage (Vref) corresponding to the maximum power point under varying irradiance conditions. The Vref is sent to the switching circuit, which generates appropriate gate pulses for the multilevel inverter switches.

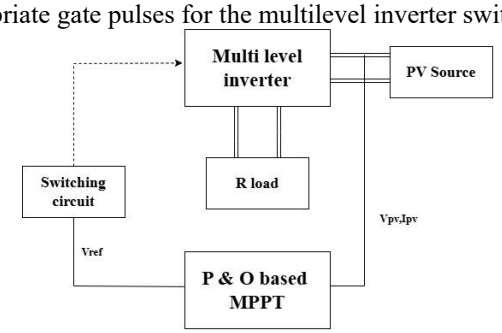

Figure 2. Proposed system Block diagram

In this, PV source is connected to the proposed multi-level inverter along with the two capacitors. The gate pulses for the inverter switches are provided from the switching circuit according to the switching table. The Figure 3 is the proposed circuit consisting of 8 switches (S1–S8), two capacitors (C1-C2), single diode (D) and PV supply (Vin). All the switches have an antiparallel diode connected across it. The circuit produces a 7-level output (0, ±Vdc, ±2Vdc, ±3Vdc) without using an H-bridge for changing the polarity. The 7LSCI topology can generate up to 7 voltage levels, and the number of output levels can be further expanded by connecting multiple (N) modules in series. The proposed topology has no back-end H-bridge and the peak inverse voltage (PIV) of all switches is limited to less than half of the output load voltage, making it suitable for high-voltage applications. Also, the switches S6 performs charging while S4 and S5 can perform discharging of capacitors contributing to reducing the number of switches. Moreover, without using a heavy and bulky transformer or inductor, only two capacitors C1 and C2 are used to generate an output voltage three times higher than the input voltage, which can increase the power density of the inverter system.

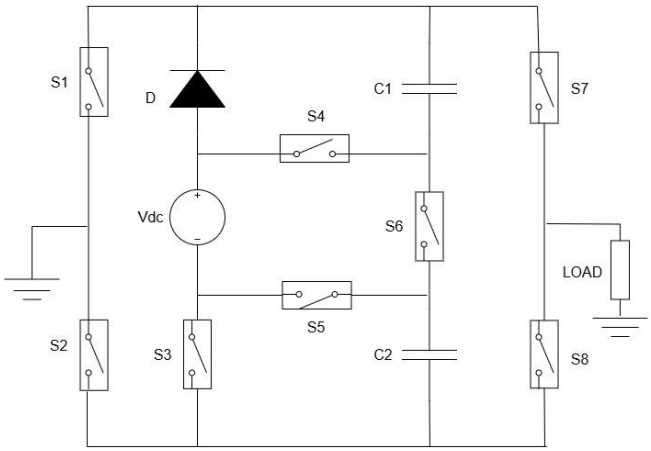

Figure 3. Proposed Circuit Diagram of seven level inverter

B. Operation of the Proposed SC Based 7-Level MLI

In the all the modes of operation Vin values is always represents the Vdc, in which Vdc is the source voltage fed from the photo voltaic block which is monitored by the P & O based MPPT controller. The inverter receives the 120V of voltage from PV array, which provide source to operate the proposed inverter.

Mode 1: Figure 4 is the +1Vdc voltage state of the proposed seven level inverter, where the capacitor C1 and C2 are in parallel with DC source Vin and charged to Vin. And also, the total amplitude of Vin is generated across the load. The Voltage flow is as follows Vdc, D,S1,Load,S8,S3and Vdc. The Charging path of the capacitors Vdc,D,C1,S6,C2, S3 and Vdc.

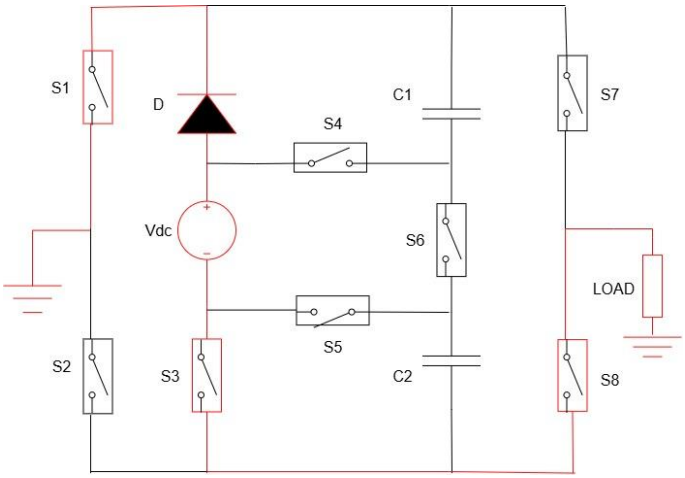

Figure 4. +1Vdc voltage state of proposed inverter

Mode 2:Figure 5 is the +2Vdc voltage state of the proposed seven level inverter, where the capacitor C2 is in series with the PV source voltage and discharged when S5 is turned on and generating the total amplitude of 2Vin across the load. The Voltage flow is as follows Vdc,D,S1,Load,C2,S5 and

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Vdc; whereas the capacitor C1 charges Vdc, D, C1, S6 and Vdc.

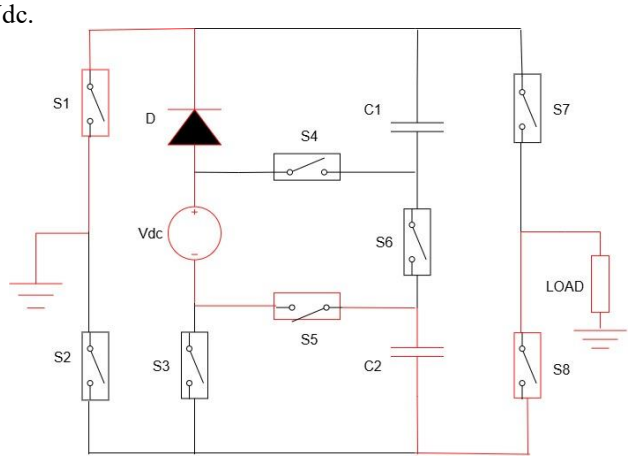

Figure 5 +2Vdc voltage state of proposed inverter

Mode 3: Figure 6 is the +3Vdc voltage state of the proposed seven level inverter, where the Vin, C1, and C2 are connected in series when both S4 and S5 are turned on, so that 3Vin is delivered to the load.

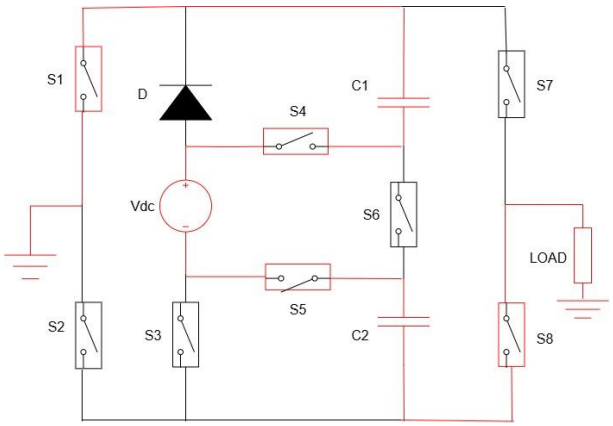

Figure 6. +3Vdc voltage state of proposed inverter

Mode 4: Figure 7 is the zero voltage state of the proposed seven level inverter, where the 0Vin is delivered to load.

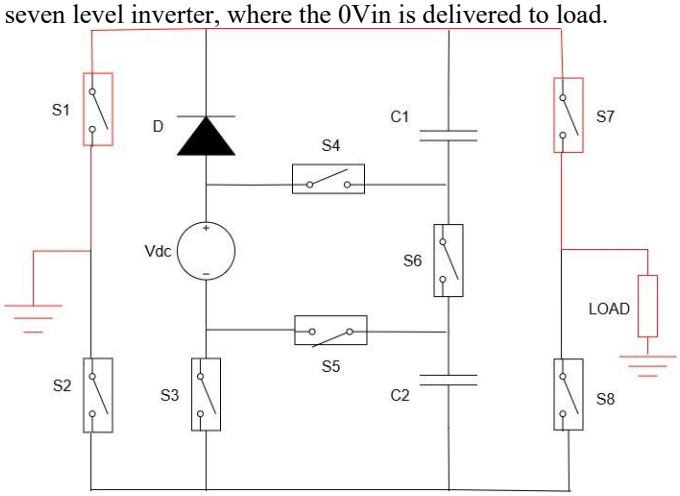

Figure 7. Zero voltage state of proposed inverter

Mode 5: Figure 8 is the -1Vdc voltage state of the proposed seven level inverter, where the Vin is in parallel with C1 and C2 but due to S7 and S2 being turned ON, -Vin is delivered to the load.

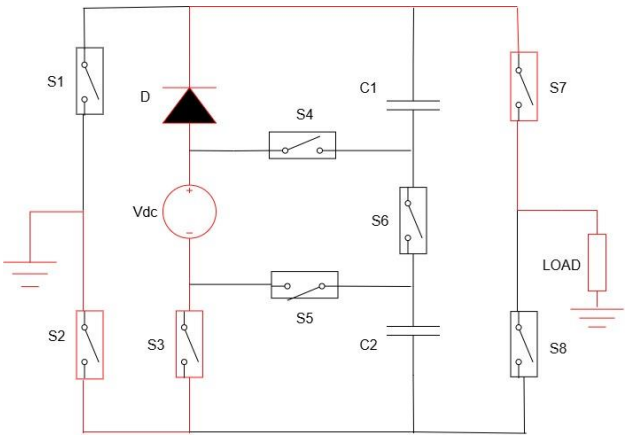

Figure 8. -1Vdc voltage state of proposed inverter

Mode 6: Figure 9 is the -2Vdc voltage state of the proposed seven level inverter, where the Vin and C1are connected in series, which results in the generation of -2Vin.

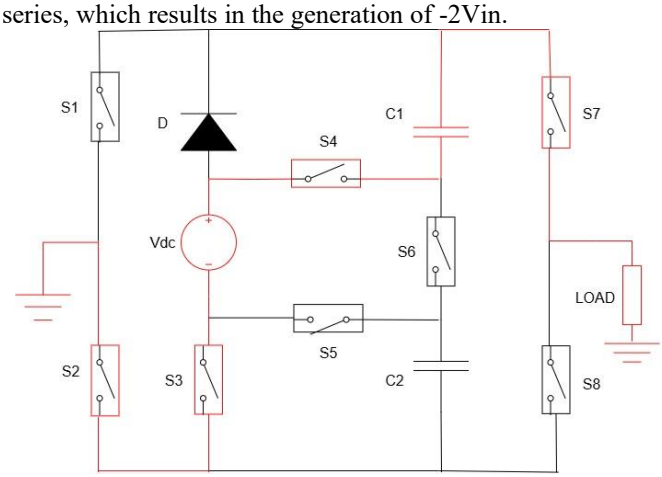

Figure 9. -2Vdc voltage state of proposed inverter

Mode 7: Finally, Figure 10 is the -3Vdc voltage state of the proposed seven level inverter, where the C1 and C2 are discharged and in series with Vin and provides the load voltage of -3Vin.

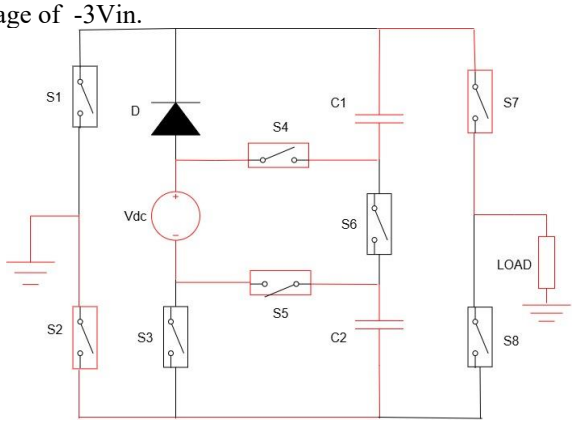

Figure 10. -3Vdc voltage state of proposed inverter

TABLE I represents the switching states of the proposed 7-level switched-capacitor inverter along with the corresponding output voltage levels is shown in the below table. The inverter operates in seven distinct states during one fundamental cycle, enabling the generation of positive, negative, and zero voltage levels. Each state is defined by a specific combination of ON

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switches, which determines both the output voltage magnitude of the seven-level inverter.

TABLE I. Switching states of the proposed inverter

S1	S2	S3	S4	S5	S6	S7	S8	**Vo**
ON	OFF	ON	OFF	OFF	ON	OFF	ON	**Vdc**
ON	OFF	OFF	OFF	ON	ON	OFF	ON	**2Vdc**
ON	OFF	OFF	ON	ON	OFF	OFF	ON	**3Vdc**
ON	OFF	ON	OFF	OFF	ON	ON	OFF	**zero**
OFF	ON	ON	OFF	OFF	ON	ON	OFF	**-1Vdc**
OFF	ON	ON	ON	OFF	ON	ON	OFF	**-2Vdc**
OFF	ON	OFF	ON	ON	OFF	ON	OFF	**-3Vdc**

C. MODELING OF PV ARRAY

An initial understanding of the performance of a solar cell may be obtained by considering it as a diode in which the light energy, in form of photons with the appropriate energy level, falls on the cell and generates electron-hole pairs. The electrons and holes are separated by the electric field established at the junction of the diode and are then driven around an external circuit by this junction potential. There are losses associated with the series and shunt resistance of the cell as well as leakage of some of the current back across the p-n junction. This leads to the equivalent circuit figure 11 as given below:

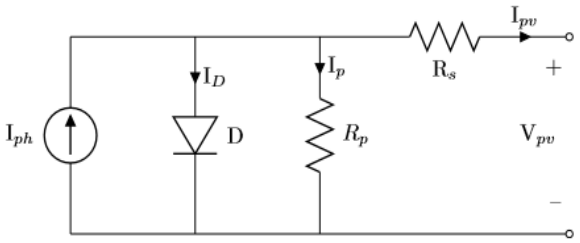

Figure 11. Equivalent Circuit diagram for Modeling of PV array

The PV cell can be modeled as a diode in parallel with a constant current source and a shunt resistor. These three components are in series with the series resistor. The output-terminal current I is equal to the light-generated current I_{ph}, less than the diode current I_D and the shunt-leakage current I_p.The series resistance R_s represents the internal resistance to the current flow, and depends on the p-n junction depth, the impurities and the contact resistance. The shunt resistance R_{sh} is inversely related to the leakage current to the ground. In an ideal PV cell, R_s = 0 (no series loss), and R_p =1(no leakage to ground). The PV cell conversion efficiency is sensitive to small variations in R_s , but is insensitive to variations in R_p. A small increase in R_s can decrease the PV output significantly. In the equivalent circuit, the current delivered to the external load equals the current I_{ph} generated by the illumination, less than the diode current I_D and the ground-shunt currentI_{sh}. The fundamental equation of PV cell can be derived from the theory of Shockley diode equation and semiconductor theory. The fundamental equations needed to design a PV cell are given below:

Using KCL we get

$$I_{pv} = I_{ph} - I_D - I_p \tag{1}$$

As we know Shockley diode equation

$$I_D = I_0 - \exp\left(\frac{e(V_p + R_s I)}{nK_b T}\right) - 1 \tag{2}$$

Now putting this value into equation (2.1) we get

$$I_{pv} = I_{ph} - I_0\left[\exp\left(\frac{e(V_p + R_s I)}{nK_b T}\right)\right] - I_p \tag{3}$$

Finally, putting the value of $I_p$in equation (3) from figure 11

$$I_{pv} = I_{ph} - I_0\left[\exp\left(\frac{e(V_p + R_s I)}{nK_b T}\right)\right] - \frac{V_p + R_s I}{R_p} \tag{4}$$

Now the output current at the standard test conditions (STC) is given as :

$$I_{pv} = I_{ph,ref} - I_{0,ref}\left[\exp\left(\frac{V_p}{a_{ref}}\right) - 1\right] \tag{5}$$

If we consider short circuit condition, V=0 we get

$$I_{pv} = I_{ph,ref} - I_{0,ref}\left[\exp\left(\frac{0}{a_{ref}}\right) - 1\right] = I_{ph,ref} \tag{6}$$

But photo current depends on light intensity and temperature. Therefore, equation of photocurrent may be defined as

$$I_{ph} = \frac{G}{G_{ref}}\left(I_{ph,ref} + \mu_{sc}.\Delta T\right) \tag{7}$$

Where,

G=Irradiance, G_{ref} = Irradiance at STC, $\Delta T = T_c - T_{ref}$,

T_{ref}= Cell temperature at STC = 25 + 273 =298,

μ_{sc} is the Coefficient temperature of short circuit current(A/K), provided by the manufacturer, $I_{ph,ref}$ is the Photocurrent (A) at STC.

Finally, by simplification we get reverse saturation current

$$I_0 = I_{0,ref}\left(\frac{T_c}{T_{ref}}\right)^3 \exp\left[\frac{-q\sum_g}{AK}\right]\left(\frac{1}{T_c} - \frac{1}{T_{ref}}\right) \tag{8}$$

D. MAXIMUM POWER POINT TRACKING

P&O algorithm is used to track and extract the maximum power from the PV system. In the figure 12 showcasing P&O algorithm the operating voltage of the PV array is perturbed by a small increment, and the resulting change in power (ΔP), is measured. If ΔP is positive, then the perturbation of the operating voltage moved the PV array's operating point closer to the MPP. Thus, further voltage perturbations in the same direction (that is, with the same algebraic sign) should move the operating point toward the MPP. If ΔP is negative, the system operating point has moved away from the MPP, and the algebraic sign of the perturbation should be reverse to move back toward the MPP. The advantages of P&O algorithm are simplicity and ease of implementation. The P&O MPPT algorithm is shown in the following figure has

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been implemented in MALAB to track maximum power from the solar PV module.

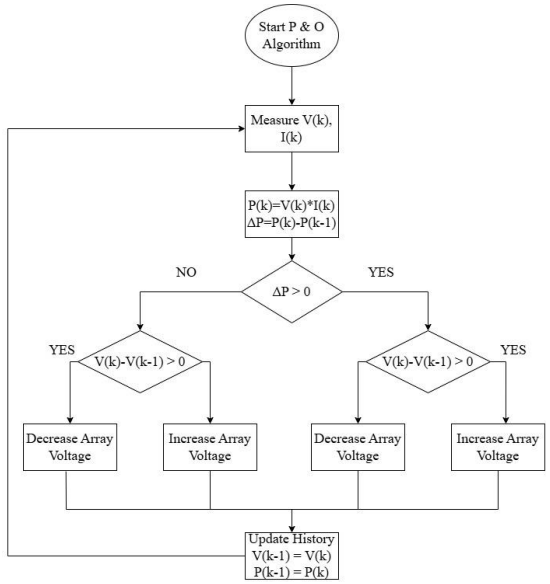

Figure 12. Flowchart for P&O algorithm of MPPT

If $\Delta P/\Delta V > 0$, ΔD is +ve (9)

If $\Delta P/\Delta V < 0$, ΔD is –ve (10)

E. MODULATION TECHNIQUE

Single-carrier sinusoidal pulse width modulation (SC-SPWM) is used to reduce the computational complexity associated with multi-carrier modulation methods and avoid the requirement for synchronization between numerous triangle signals. The final pulses achieved by comparing a single triangular carrier signal with a sinusoidal modulating signal. The fundamental idea behind the suggested switching technique is to compare the triangle carrier signal at the intended switching frequency with the reshaped reference signal, which has been sinusoidally corrected to fit inside the single triangular carrier range. The modulating signal, following reshaping, has an amplitude of (Aref), whereas the triangular carrier has a peak amplitude of (Atri). Figure 13 illustrates the evolution of the comparison zone on both the positive and negative sides of the sinusoidal reference. The modulation index Ma is mathematically defined as

$$Ma = \frac{Aref}{Atri} \quad (11)$$

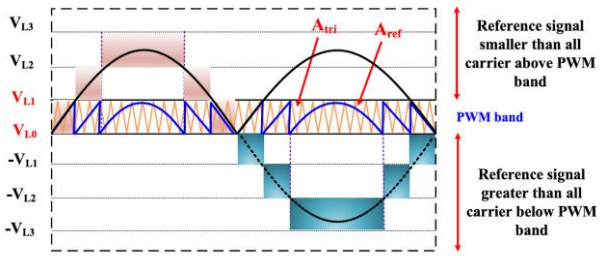

Figure 13. SC SPWM Modulation scheme

In SC-SPWM, a single high-frequency triangular carrier Vtri(t) is continuously compared with a low-frequency sinusoidal reference Vref(t). Switching signals are generated whenever Vref(t) $\geq$ Vtri(t) and turned OFF otherwise.

III. SIMULATION RESULTS

The proposed system is implemented in MATLAB/Simulink using the Simscape Electrical toolbox. A solar PV block is modelled as the DC source and connected to the power conversion stage. The simulation is set in discrete mode using the *powergui* block with a sampling time of 1e-6 s. Voltage and current measurement blocks are used at the PV output, and RMS blocks compute effective values for performance analysis. These signals are processed through mathematical and control blocks to generate reference signals. The multilevel inverter (MLI) subsystem is modelled using controlled switches and connected to the load through measurement ports. Proper gating pulses are applied to the inverter switches to obtain the desired multilevel output waveform, and scopes are used to observe voltage and current responses.

The interpretation drawn after completion of the full-fledged project is that it's a multilevel inverter used for many purposes. We have done simulation in MATLAB Simulink platform for various R load and RL load. Based on total harmonic distortion factor (THD)the circuit is modified in such way to get a minimal THD factor.

The simulation circuit for the proposed inverter is provided below:

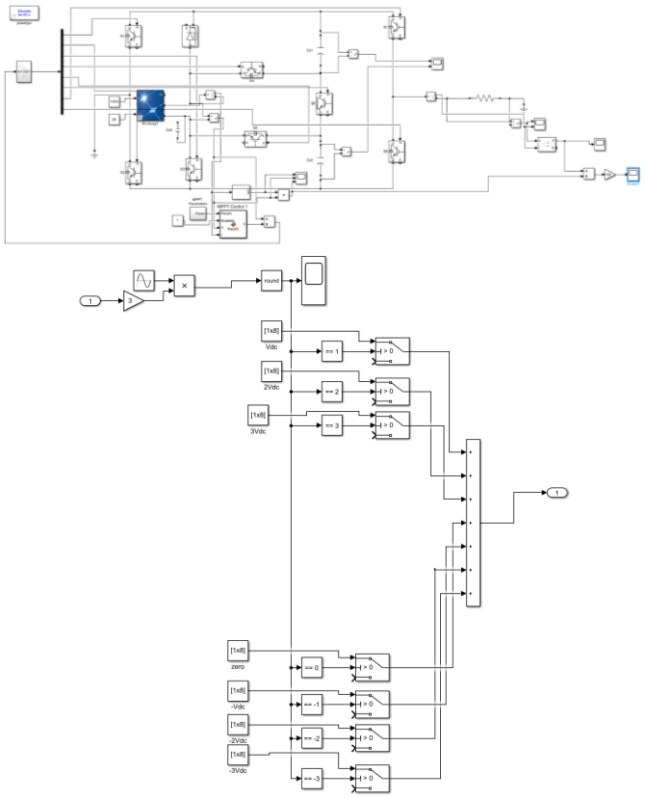

Figure 14. simulation circuit for the proposed inverter

Figure 14 illustrates the simulation circuit of the proposed PV fed seven level inverter consists of eight power electronic switches, two capacitors, and a photovoltaic (PV) voltage source connected to a 20 Ω resistive load. The PV array operates at an irradiation level of 1000 W/m² and a

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temperature of 25 °C, while the system is simulated with a sampling time of 1e-6 s to ensure accurate and high-resolution performance analysis.
The parameters used in the simulation is provided below:

Table II. Design Specification of the system

Parameters	Values
DC Voltage (Vin)	120V
Inverter output frequency (f)	50Hz
Inverter output Voltage (Vo)	360V
R Load Value	20Ω
RL Load Value	40mH
Capacitor Values (C1, C2)	6700µF
Capacitor Voltage (C1, C2)	120V and 120V
Switching frequency	50Hz
No. of switches used	8 - IGBT
Gate Control Method	SC SPWM

Table II summarizes the key simulation parameters used to evaluate the performance of the proposed 7-level switched-capacitor multilevel inverter.

The PV voltage, current and power is provided below:

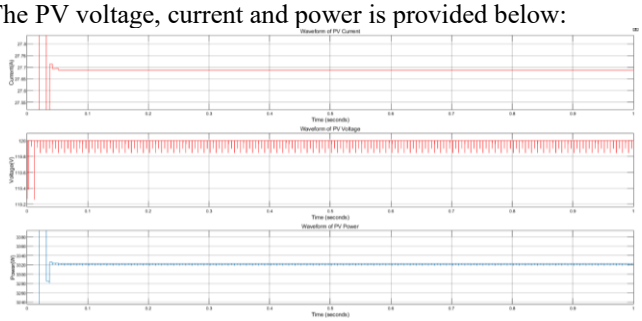

Figure 15. Waveform of PV voltage, current and power.

Figure 15 illustrates the PV current is around 27.7A and voltage of 120V and the power is 3320W, in which the three plots are represented as waveforms showing the PV system's electrical behaviour over time. The current waveform initially exhibits a transient response and then settles at approximately 27.7 A, indicating stable operation. The voltage waveform reaches and maintains around 120 V with small high-frequency ripples caused by converter switching. The power waveform rises rapidly during startup and stabilizes near 3320 W, confirming successful tracking of the maximum power point.
These steady waveforms demonstrate proper MPPT control, efficient energy extraction, and stable performance of the photovoltaic system under the given operating conditions.
Figure 16 illustrates the amplitude of the load voltage is in the range of 358V to -358V with each level is of 120V. In this there are 3 positive voltage levels and 3 negative voltage levels and with zero level, we got 7 level voltage. The 7 voltages level involves 0V, negative and positive voltage levels of 120V,240V and 360V. The two waveforms represent the load voltage and load current of a multilevel inverter system. The upper waveform shows a seven-level output voltage with an amplitude ranging from +358 V to −358 V. Each voltage step is approximately 120 V, resulting in three positive levels, three negative levels, and one zero level.
This stepped waveform closely approximates a sinusoidal voltage and helps reduce harmonic distortion. The lower waveform represents the load current, which follows the voltage waveform and reaches an approximate amplitude of 18 A. The smooth current shape indicates effective filtering and stable power delivery to the load. The lower waveform represents the load current, which closely follows the voltage waveform and reaches an approximate peak amplitude of 18 A. Its smooth, continuous shape reflects effective filtering by the system, minimizing ripple and distortion. This behaviour indicates stable power delivery, efficient energy transfer, and reliable operation of the load under steady-state conditions.
The load voltage and current is provided below:

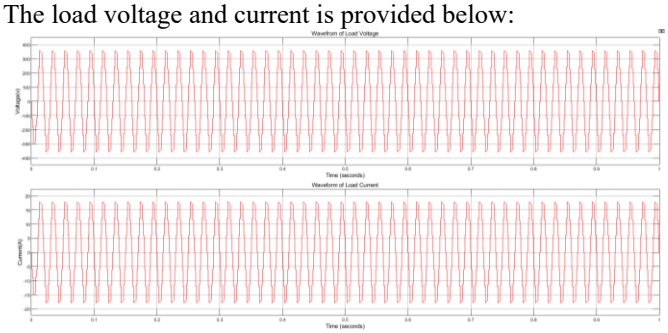

Figure 16. Waveform of load voltage and current.

The capacitor voltages are provided below:

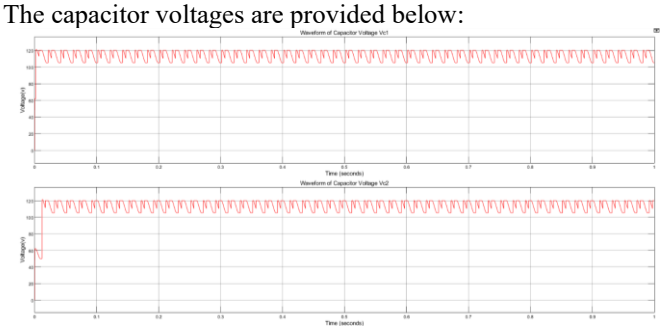

Figure 17. Waveform of capacitor voltages.

Figure 17 illustrates the capacitor voltage waveform illustrates a well-regulated DC-link voltage that varies within a narrow band between 110 V and 120 V. During the initial startup phase of the system, the voltage gradually increases as the DC-link capacitor charges through the power converter, indicating proper energy buildup and controlled inrush behaviour. After the system reaches steady-state operation, the voltage stabilizes and remains confined to this specified range. Small voltage ripples are still observable, primarily due to the high-frequency switching action of the converter and dynamic changes in the load demand. These minor fluctuations reflect the normal charging and discharging cycles of the capacitor as it continuously supplies and absorbs energy to support the inverter stage. Overall, the maintained DC-link voltage range confirms effective voltage regulation, adequate energy buffering, and reliable performance of the power electronic system, ensuring stable operation and consistent power delivery to the connected load.

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Figure 18 illustrates the load power waveform represents how power is delivered to the load over time, showing both transient and steady-state behaviour. During the initial transient period, the power increases rapidly as the converter and inverter start operating and system conditions stabilize. Once steady state is achieved, the power settles around an average value of approximately 3173 W. The waveform remains mostly constant, with only small oscillations present. These minor ripples are caused by switching actions and voltage–current harmonics introduced by the multilevel inverter and the load characteristics. Such fluctuations are normal in power electronic systems. Overall, the steady power output indicates efficient energy transfer, stable operation, and reliable performance of the power conversion system supplying the load.

The output power is provided below:

Figure 18. Waveform of output power.

The efficiency of the proposed inverter is provided below:

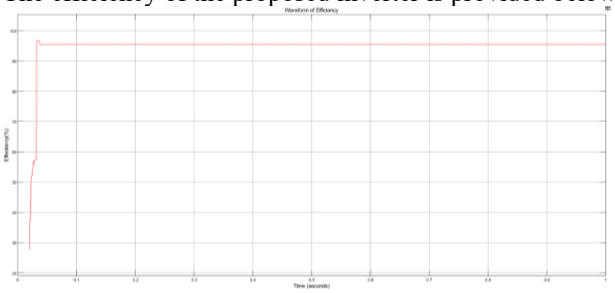

Figure 19. Waveform of efficiency of the proposed inverter.

Figure 19 illustrates the efficiency waveform of the proposed inverter illustrates how effectively the system converts input DC power into usable AC output power over time. An average efficiency of around 95.5% indicates that only a small portion of the input energy is lost during the conversion process. Minor fluctuations in the efficiency waveform are expected and occur due to switching losses in the semiconductor devices, conduction losses in power components, and variations in load conditions during operation.

Despite these small variations, the efficiency remains consistently close to 95.5%, demonstrating stable and reliable performance. This high efficiency highlights the effectiveness of the inverter's design, including the selection of low-loss power electronic components and well-implemented control strategies. As a result, the inverter minimizes energy wastage, reduces heat generation, and enhances system reliability.

Figure 20 illustrates The FFT (Fast Fourier Transform) analysis of the load current waveform reveals the harmonic content present in the signal. With a total harmonic distortion (%THD) of around 3.46% at the fundamental frequency of 50Hz (maximum of 1000Hz) and start time of 0.3s, the current waveform is very close to an ideal sinusoid, indicating low distortion.

This low %THD means that the inverter and filtering components effectively minimize harmonic generation caused by switching operations and the multilevel output voltage. Low harmonic distortion reduces losses, electromagnetic interference, and stress on electrical equipment, improving system reliability and efficiency. The FFT plot typically shows a dominant fundamental frequency peak with only small magnitudes of higher-order harmonics, confirming that the load current waveform maintains high power quality, which is essential for sensitive electrical loads and compliance with grid standards.

The %THD for the output current of the proposed inverter for RL load is provided below:

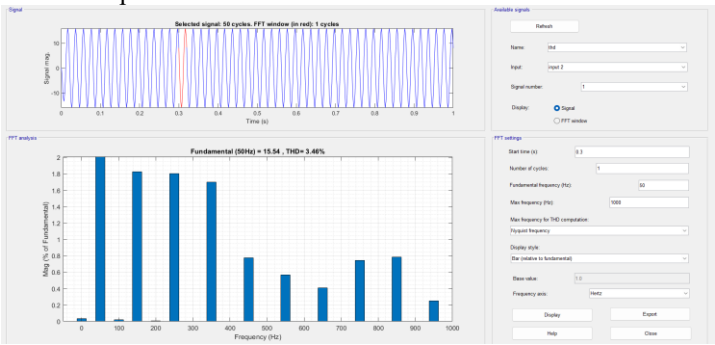

Figure 20. Waveform of the FFT analysis

IV. CONCLUSION

In this paper, The simulation results confirm that the proposed inverter meets its design goals. The AC load voltage waveform is a seven-level stepped sinusodial with amplitude approximately ±360 V (i.e. ±3× the 120 V PV input) and a clear zero level, as expected. Each step has amplitude 120 V (the PV nominal), giving the levels (0, ±120, ±240, ±360 V). The capacitor voltages remained close to the PV voltage: during operation C1 and C2 each charged to about 110–120 V, demonstrating the intended self-balancing action.

Key performance metrics from the simulation include:

Output Power & Efficiency: The AC load draws around 3173 W. With the PV supplying ≈3320 W, the inverter efficiency is about 95.5% (power out divided by PV power). This high efficiency is due to the reduced device count and low switching/diode losses.

Total Harmonic Distortion (THD): The output current THD was simulated at roughly 3.5%. The stepped 7-level waveform significantly suppresses low-order harmonics compared to a two-level inverter, consistent with expectations for multilevel topologies.

These results show that the inverter successfully boosts the PV input by a factor of three and delivers a clean multilevel AC output. The PWM or modulation strategy (e.g. nearest-level or sinusoidal PWM) can be applied on top of this switching structure to synthesize a near-sinusoidal output. In practice, the fast switching of the SC network can achieve waveform quality and THD comparable to other modern MLIs. The high efficiency and low THD observed are in line with recent

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literature on SC-boost MLIs, which report similar performance using compact topologies.

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