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Phase Locked Loop: A Review

Rachana Arya
Ph.D. Scholar, ECE Separtment
OPJS university, Churu, India

Suman
Associate Professor
OPJS university, Churu, India

***Abstract*— Phase locked loop act as colossal role towards the expansion of the ASIC (application specified integrated circuits). With this technology, the delay time of the circuits was decreased. It is primary building block for several devices, like clock pulse creation, microprocessors, fasten the circuits and lots of. The essential quality like locking capability of this locked loop, it can be present in various applications. At the present time, wireless equipments can show the way in our lives. All engineering mind focused on the tininess of the circuits, mechanism and dimensions the devices. The RF communication is indispensable for promptness of data transition in wireless systems. Through the frequency synthesis, RF transmission use steady timing signals to be generated by phase locked loop. After detailed study of many papers, the performance, design, and enlargement of PLL circuit is framed.**

I. INTRODUCTION

Phase lock loop is a fundamental part of radio, wireless and telecommunication technology. Nowadays digital systems are using clocks for sequencing their operations and synchronizing different functional units. The most versatile application of phase locked loops (PLL) is clock generation and clock recovery. The data transfer rates and clock frequencies have been constantly increasing with every generation of processing technology. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with faster locking ability.

The history of the phase-locked loop dates back to as early as 1932. According to author Dr. Rolland Best, the French engineer De Belle size is the inventor of coherent communication. Phase locked-loops (PLLs) are extensively used to generate well-timed on-chip clocks to be used in high-performance digital systems. Phase locked loop is a closed loop system which locks the phase of its output signal to reference input signal. PLL is a mixed signal circuit as its architecture involves both digital and analog signal processing units.

Classification of PLLs

Using the notation of Best [8] and Gardner in [9], the different classes of PLLs are as follows:

1. Analog Phase-Locked Loop (PLL)
2. Digital Phase-Locked Loop (DPLL)
3. All-Digital Phase-Locked Loop (ADPLL)

On the basis of component used, the PLL can be divided into sub-sections; given in table 1.

TABLE 1: CLASSIFICATION OF PLL ON THE BASIS OF COMPONENT USED

PLL Type	Phase Detector	Loop Filter	Controlled Oscillator
Analog PLL	Analog Multiplier	RC	Voltage
Digital PLL	Digital Detector	RC	Voltage
All Digital PLL	Digital Detector	Digital	Digital Controlled
Software PLL	Software Multiplier	Software	Software

II. RELATED WORK

In 2019, Shruti Hathwalia and Naresh Grover [14], presented a comparative study on DPLL. In that research they present a relative review of Ring oscillator and LC oscillator for PLL. They also discuss both the oscillator's parameters and pros and cons of the systems.

Lei Zhang et al. [15], uses a fast acquisition PFD to eliminate non ideal effects of PLL. 65nm technology is used for designing of PFD. This consumes the area of 0.0016mm^2 for 1.5mW power only. By the simulation, the maximum operating frequency is 5GHz.

Usha Kumari and Rekha Yadav [12] reviews and article on Digital PLL. They had discussed about the basic building blocks and the features of them. By the comparison analysis they concluded a circuit having low noise and better control range. The circuit is basically used for receivers and wireless systems.

Supraja Tirumalasetti et al. [16], proposed reduces jitter PFD to increase the lock range of PLL. It uses the pass transistor to increase the rise time. The operating frequency of this is 5MHz with delay of 2.93 seconds.

Leela Bitla et al. [17], presented a paper on Analysis of NAND gate based phase frequency detector for phase locked loop. The PFD designed for this is a NAND gate based that consume appreciably low power over different temperature variation. The range of slew rate is 44 v/ns - 30 v/ns on 65˚C.

Shanker N. Dandra and Ankita H. Deshmukh [6], designed DPLL using 45nm technology. X-OR Phase detector is used for DPLL. The V_{dd} is 0.9v with input frequency of 2.4 GHz. The lock frequency of DPLL is 7.1 GHz at 0.9V control voltage. Loop is locked at 2.4 GHz frequency.

In 2017, Nabihah Ahmed et al. [19], obtained a tri-state CP and 2nd order LPF used in PLL system. The projected design has been simulated by 130nm technology in Cadence Tool at 1.2v supply. The throughput swing is 288 mV to 413.8 mV at 4.7 GHz frequency. The layout area measurement is 31.4 µm x 22.6 µm (0.7096 mm^2).

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Gande Bhargav et al. [20], devised a PLL by adjusting the values of CP and LPF. The locking time is about 1.5µs at 1V supply. The total power consumption of oscillator is 0.5uW. CMOS technology (90nm) is used for the proposed design

III. REGION OF OPERATION OF PLL

The PLL have three basic regions of operation for which it can work. If it is not locked (input and output are on different phase) PLL is in dynamic state. And if both phases are same it is called as static state.

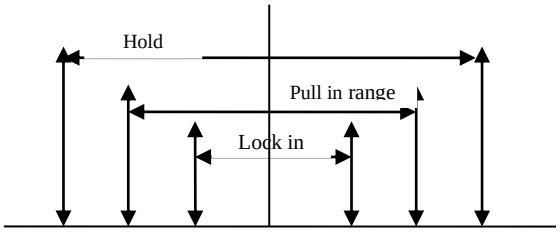

Fig. 1: PLL Region of Operation

A. Hold range

It is the range of frequencies in which PLL can maintain phase tracking between input and output. If reference frequency is gradually condensed or enlarged, the PLL will be unable to find lock. This is called hold range. It will be temporarily stable just in this range [9].

B. Pull in range

In dynamic state it will constantly locked. Initially PLL is unlocked. It will obtain locked state if reference frequency is applied in the pull in range. If input frequency is outside then this, the PLL will never acquire lock condition.

C. Lock range

The range frequencies from which loop can uphold the lock state. All the region of operation is shown in the "Fig 1".

D. Pull out range

The frequency, facilitate the PLL to release. If input frequency is below the pull out range the PLL remain lock. On the other hand if it will exceed, PLL will not be capable to follow the output signal. After some time it may obtain lock. It is called static state of PLL.

IV. OPERATION OF PLL

The Analog PLL is built with entirely analog functional blocks. The basic block diagram of a analog PLL is shown in "Fig. 2". APLL is a closed-loop feedback system that sets fixed phase relationship between its phase of output clock and the phase of a reference clock [9]. This is used to track the phase changes that are within the bandwidth of the PLL. PLL also multiplies a low-frequency reference clock 'θi', to produce a high frequency clock or feedback clock 'θo'. An analog multiplier is used as the Phase Detector (PD) to produces an error output signal based on the phase difference between the feedback clock and the reference clock [10, 11]. The phase difference signal is applied to the Loop Filter. The Loop Filter is basically a low pass filter, built with passive or active components. The filtered error signal acts as a control signal (voltage or current) to the oscillator and adjust the frequency of oscillation to align feedback phase to the reference phase. The Voltage-Controlled Oscillator (VCO) is a ring oscillator constructed by differential inverter stages. As a result, the VCO changes its operating frequency, hence changes the output feedback signal. This output signal is fed back to the Phase Detector. The Phase Detector detects the new phase difference again and the same feedback process occurs. In this way, the phase error vanishes eventually and the phase locking is completed.

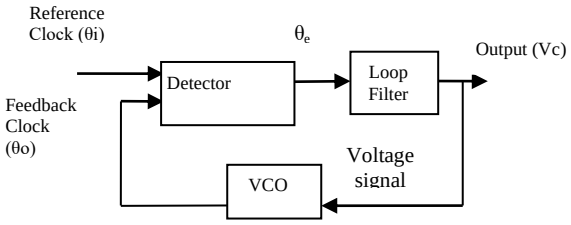

Fig. 2: Block Diagram of Analog PLL

A four-quadrant multiplier Phase Detector is shown in "Fig.3" [12], which is an ideal analog design. The phase detector is a multiplier and it is applied for determining the phase relationship between the reference clock and the feedback clock. The output of the multiplier is made up of two periodic waveforms. One frequency is the difference of the two input sinusoids and the output wave's frequency is their sum [9].

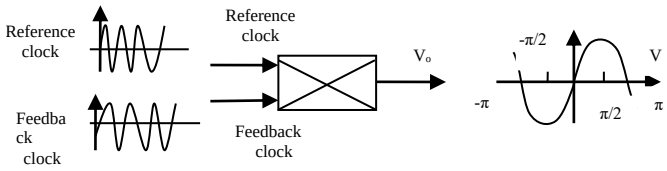

Fig. 3: Operating diagram of a four-quadrant multiplier PD

If we have two sinusoids s1 and s2, both have same frequency but have phase difference of 90º. By multiplying these two signals, s_3 signal is obtained. We take s_1 and s_2 as sine and cosine signal respectively.

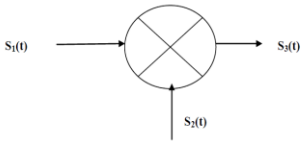

Fig. 4: Multiplier based Phase Detector

$$s_1(t) = A_1 \cos[\omega t + \Theta_1(t)] \quad (1)$$

$$s_2(t) = A_2 \sin[\omega t + \Theta_2(t)] \quad (2)$$

$$s_3(t) = s_1(t).\, s_2(t) \quad (3)$$

The output of the multiplier is

$$s_3(t) = Km\, s_1(t)\, s_2(t)$$

$$= K_m A_1 \cos[\omega t + \Theta_1(t)]\, A_2 \sin[\omega t + \Theta_2(t)] \quad (4)$$

Where 'K_m' is the gain of the multiplier. By the above equation, the multiplier signal s_3 consists of two parts, the first one is the function of only the phase difference of two signals, and the second term is the frequency which is twice of the signal frequency plus the sum of the two phases. The second part of the equation is the high frequency component and it can be discarded by filtering out since it does not contain any necessary information.

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V. COMPARISION OF PLL PARAMETERS

The different comparison parameters of all the components are shown by tables I, II and III.

TABLE I. COMPARISON OF DIFFERENT TYPE OF PHASE DETECTOR

Phase Detector			
S.N.	**Type**	**Advantages**	**Disadvantages**
1	EX-OR	It will generate the output voltage for both the cycles of input pulse.	The data losses occurred, because that is not sensitive for both edges
2	JK flip flop	The data losses will not be occurred because that is sensitive for both clock edges	It produced larger phase tracking and the angle is -180° to 180° phase error
3	PFD	The Phase error shifted for -360° to 360°. It will lock the input for different conditions.	Circuit complexity is high as the numbers of components are more than other phase detectors.

TABLE II. COMPARISON OF DIFFERENT TYPE OF LOOP FILTER

Loop filter			
S.no.	**Type**	**Advantages**	**Disadvantages**
1	Active fliter	In this filter load resistance does not affect the operation of circuit.	At the high frequency circuit output is not fixed
		Bandwidth of the circuit can be easily adjusted by varying the parameters of the circuit.	The throughput is unreliable at high frequencies.
		It provides good isolation between load and the circuit components.	As the change in the input voltage occurs, it will openly change the output of the circuit.
2	Passive filter	Easy to design and compact, light in weight.	Q factor is low.
		Works on very high frequency so it will suffer with noise.	It cannot reduce the ripples.
		Enhances the circuit complexity.	It will easily alter the control voltage.
		No isolation required between load and the circuit.	Modulate the clock frequency so the clock pulse will vary.
		Q factor is high.	It becomes costly as active components are used.

TABLE III. ADVANTAGES AND DISADVANTAGES OF VCO

Voltage Control Oscillator			
S.no.	**Type**	**Advantages**	**Disadvantages**
1	LC Oscillator	Squat phase noise	Outsized layout area->larger area for inductor
		Excellent stability	Tank networks may have resultant resonant frequencies, which cause unwanted performance loss to the circuit.
		Low jitter performance of the circuit	Constricted tuning range, require lot of classification to tune and it has supplementary complex design.
2	Ring	Simple to integrate	Reduced phase noise
		Superior phase noise	Hardly ever worn for RF systems
		Phase generation is 360° at the time of oscillation and it is used in elevated data links	It will suffer with jitter problems

VI. RESULT AND CONCLUSION

The purpose is to limit the centre frequency by the scaling of transistor at the different levels. As a result the locking time of the PLL is reduced as compared to the paper [14]. As the same supply voltage is used in both papers transistor's size would change the all parameters. The oscillation frequency is far better to the compared paper. The power consumption is almost 1.08mW with five stages of oscillator. The comparison parameters are shown in following table 4. By varying the low pass filter parameters the oscillation frequency can be changed.

Parameters	Proposed design	[14]	[17]
Technology	120nm	130nm	130nm
Supply voltage	1v	1v	1.8v
Power consumption	1.08mW	2.07mW	0.061mW
Centre frequency	98.76 MHz.	500MHz	600MHz
No. of Stages	5	5	6
Oscillation frequency	333.4MHz	800MHz	2 GHz
Register R1	300kΩ	1.38KΩ	-
Load capacitance C1	10 pF.	15pF	-
Glitch of PFD	1.016 ns to 1.426 ns	1.5µs	-
Delay time Td	20.25ns	-	-

TABLE 4 THE PERFORMANCE ANALYSIS OF DIFFERENT PARAMETERS

Phase frequency detector is designed by the D flip flop so one glitch is coming at the simulation result at 1.06ns time period. These pulses can change the control voltage for VCO. The maximum peak occurs at 98.76 MHz frequency.

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