Phase Locked Loop – A Review

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***Abstract*—— In this article different types of Phased locked loop technique are studied and after comparing all circuits we found that the Digital phased locked loop have result in good phase noise performance with low power consumption with improved tuning range as compared to other phased locked loop circuits, as it uses the CMOS technology providing the real solution in the band of radio frequency. It is used in various applications such as wireless sensor network, transceiver, Clock generations, clock recovery circuits etc.**

Keywords— Current Starved Voltage Control Oscillator (CSVCO); LC coupled Voltage Controlled oscillator (LCVCO); Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS) ;low noise;ultra low power;phase locked loop (PLL).

I. INTRODUCTION

Phase locked loop is abbreviated as PLL. Brain of phase locked loop is voltage controlled oscillator. In technical fields, such as frequency control, frequency synthesizing, FM (frequency modulation) demodulation, data recovery, signal synchronization, there used PLL. Jitter attenuator for reduce noise within jitter is the versatile application of the phase locked loop that is for communication system, networking, variation of phase carried on a clock signal. Phase locked loop circuit is necessary for increase of circuit speed. This is known to provide a clock recovery circuit using a phase locked loop for example, in a digital transmission system, a clock signal which is used for timing purposes in processing the data signal. The data signal is a serial binary signal having binary 0s and 1s represented respectively by the absence and presence of a positive voltage and the clock signal is produced at the bit rate of the data signal. The present innovation relates to a phase-locked loop, and more particularly, to frequency stabilization of an oscillation output signal generated by a phase locked loop. The present invention further relates to a current drive type charge pump circuit and a voltage controlled oscillator of the phase-locked loop. The phase locked loop was initiated as far back as 1932 by H.de Bellescizi, at that time for synchronous reception of radio signal. Now, the phase locked loop is found in numerous applications of all modern technologies. It is widely used in all areas of electronics and in different fields of communication.

II. RELATED WORKS

In recent development era of new involvement of emerging technologies vastly introduce in the field of VLSI. Our study is based on PLL which is started in early in 1932 which reach to its peak with a great upsurge where as consumption of power and circuit area is reduced. The phase-locked loop (PLL) is a prime component globally used in various integrated circuit IC including clock recovery and wireless communication system frequency synthesizers and communication system. Currently, system-on-chip (SOC) and Microelectronics designs are used for delay-locked loops and for matching the clock [1]. By appropriate choosing the Phase frequency detector framework and adjusting the charge pump current and the loop filter design values gives a better lock time can be achieved [2]. Mahmoud Abdellaoui et.al presented the design of the Inverse Sine Phase Detector (ISPD) with more effective and simplicity, robustness, in this ISPD PLL Demodulator designed without using any of the filters [3]. Modeling and design of a multi-standard fractional PLL in CMOS/SOI technology is used in [4]. To suppress the coupled supply noise A step-down voltage regulator is utilized is described in [5]. By limiting the sweep rate of VCO for a phase-lock loop applied sweep voltage which promptly declined the closed-loop frequency error to a tip where phase lock occurs quickly [6]. A low-power high-compelling ability voltage control oscillator used in PLL is introduced in [7]. To control the loop dynamic characteristics, the capacitance in the loop filter is on-chip calibrated so that the loops are accurately controlled despite the process variation [8]. In this article demonstrate the chaotic behavior of a nonlinear amplifier (NLA) - based delayed phase-locked-loop (PLL) including a first order phase detector for a certain range of system parameters [9]. A multiplexer based length varying ring oscillator and the effects of using it as a voltage controlled oscillator (VCO) in a phase locked loop (PLL) based system is proposed in [10]. A research of true random number generator based on PLL using FPGA in [11]. PLL has been applied in, angle modulation, carrier regeneration and demodulation, frequency synthesis, data/clock recovery etc [12-14]. The main incorporation of data and clock recovery are jitter transfer, tolerance, generation, acquisition time and capture range, among which jitter characteristics are the major and most important clock data recovery specifications is illustrated in [15].a new charge pump circuit is introduced by using 0.18 µm CMOS technology, which helps in reducing the mismatch of current which lies in between two branches of the cascade current mirror topology, By using this proposed circuit, the mismatching between the two input UP/DN current of the Charge pump can be achieved with less than 0.065% from post-layout simulation and spur is also reduced with applying low power consumption and low noise technique which results in better output [16].

TABLE I. CLASSIFICATION OF VARIOUS PLL TOPOLOGY

SL no.	PLL	Phase detector	Loop filter	Oscillator
1.	Linear PLL	Analog	Analog	Voltage Controlled Oscillator
2.	SF -PLL	Analog	Analog	VCO
3.	Q- PLL	Analog	Analog	VCO
4.	Digital PLL	Digital	Analog	VCO
5.	All Digital PLL	Digital	Digital	Digitally controlled oscillator(DCO)
6.	Software PLL	Software	Software	Software

III. BASIC BUILDINGS BLOCK OF PLL

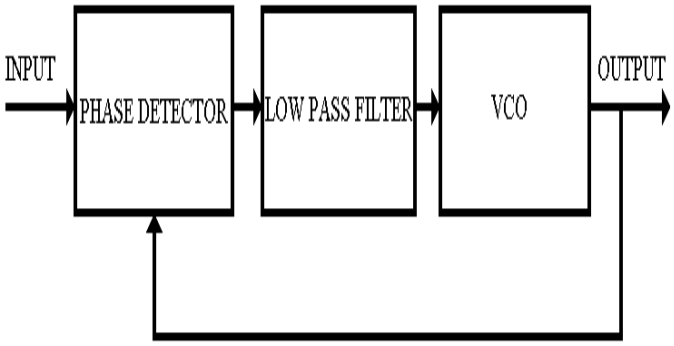

Fig. 1. Block Diagram of PLL

The Conventional Phase Locked Loop (PLL) Circuit forms of the following three fundamental blocks are Phase Detector or Comparator (PD), Low Pass Filter (LPF) and Voltage Controlled Oscillator (VCO). Monolithic integrated CMOS Phase Locked Loops are among the most versatile components of modern integrated systems (system-on-chip) [1]. One of the most demanded PLL functions is its on-chip clock synthesis. Other distinctive features of PLL circuits are that their output frequency is invertible or programmable in proportion with the input phase difference. This is the main reason why PLL finds applications in Frequency Modulation and Demodulation systems, Frequency synthesizer and Clock Generator. The major drawbacks of PLL design are Power-consumption to make power as low as possible, area as lesser the area more is its efficiency and stability of synthesized frequency with low jitter, Although all of the above three must be considered for an efficient PLL design, yet low jitter is the most important among all of them all. Sometimes low jitter is

Obtained at the expense of power consumption, which is again undesirable for mobile applications. Another error that occurs in PLL circuit design is that the synthesized frequency comes to be time variant. A significant point to taken into consideration is with the frequency incrementing of the inputs of the phase comparator, large number of errors are introduced in the phase difference measurement [17]. Thus, to maintain stability in the phase comparator operation at high frequencies, the phase comparator detection-sensitivity must be augmented. A low detection-sensitivity more distantly leads to control voltage instability, thereby augmenting the noise component at the VCO output. The output signal phase noise of PLL again devaluates the data error ratio [18]. In the following sections of the paper, we have analyzed the basic building blocks of the phase-locked-loop circuit. These blocks have been described by each block.

A. Phase Detector

XOR gate is the best example of phase detector which is shown in Fig. 3. In this figure it is expressed that the phase difference between the inputs varies, so does the width of the output pulses. While the XOR circuit produces error pulses on both rising and falling edges [19].

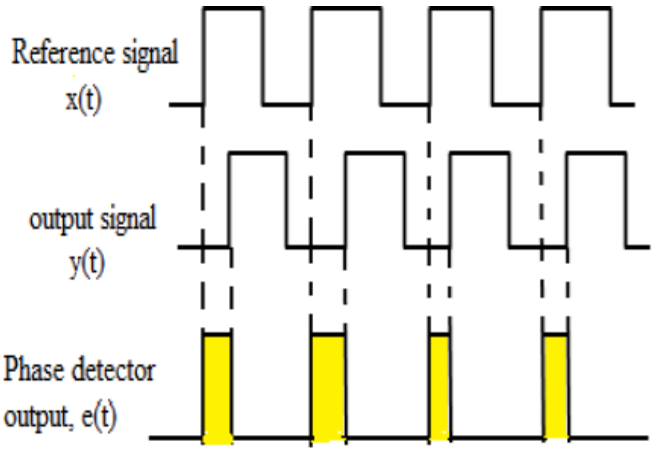

Fig. 2. Phase detector output [20].

B. Low pass Filter

A low pass filter used for passing the low frequency signal and its rejects the higher frequency signal it takes input from the phase detector circuits and produces the appropriate control voltage to the voltage controlled oscillator

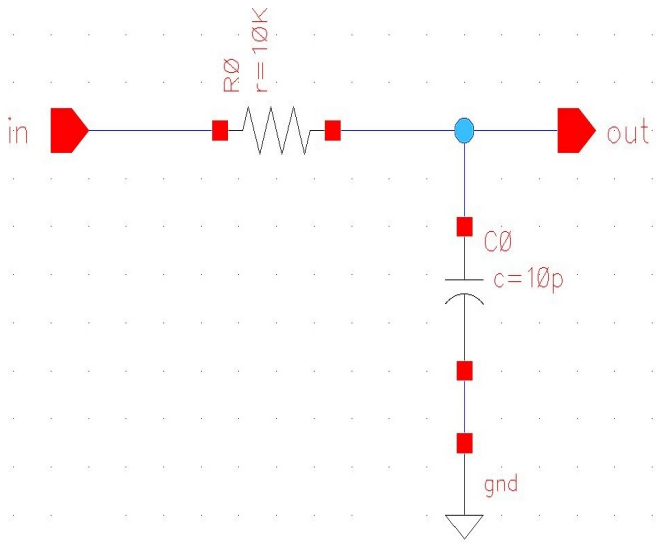

Fig. 3. Low pass filter circuits

Low pass filter is the next block after the phase detector circuits the input of the low pass filter is provided by the output of the phase detector which enables the circuits to pass the lower frequency and suppressed the higher cutoff freq.

TABLE II. PERFORMANCE COMPARISION OF VARIOUS PLL

Work	[23]	[24]	[25]	[26]	[27]	[28]	[29]	[30]	[31]
Technique	Freq Estimation algorithm(FEA)for fast locking	BW Tracking technique	Delay based technique to reduce power dissipation	Bang-Bang algorithm for low power, low jitter Δ Σ fractional - N digital freq. synthesizer	BW And tuning range tracking technique to improve jitter	Floating point representation technique to design TDC	Feed Forward compensation technique for fast frequency locking	Bang-Bang algorithm m for fast locking	Adaptive loop gain control (ALGC) technique to reduce nonlinearity of PFD and reduce O/P jitter
Input frequency	220 KHz to 8 MHz	28 MHz to 225 MHz	12 MHz	40.01MHZ	350MHz	80 MHz	375 MHz	26 MHZ	50MHZ
Output frequency	28 to 446MHz	1.80GHz	2.40GHz	2.92to4.05GHz	0.70 to 3.50GHz	0.90 to 1.25GHz	4 to 416MHz	_ _ 12 mW 16.50 mW	0.30to 1.40GHz
Power Consumption	-	-	12mW	4.50mW	1.60mW at 2.50GHz	18mW to at 75MHz	11.39mW	26 MHZ	16.50mW
Area	330*250um^2	-	0.24mm^2	0.22mm^2	0.30mm^2	0.87*0.68m^2	582.20*343.00^2	Technology	0.20mm^2
Technology	0.18 µm CMOS	65nm CMOs	65nm CMOS	65nm CMOS	90nm CMOS	0.18uM CMOS	0.18um CMOS	peak to peak jitter	0.13um CMOS
Peak to peak jitter	70ps	42ps	-	-	11.60ps	27.80ps	-	Technology	32bps

C. Voltage Controlled Oscillator (VCO)

A VCO is divided into two main parts i.e. Current starved VCO (CSVCO) and LC coupled or source coupled VCO (LCVCO). In the basic building blocks of phase locked loop circuits VCO works as the heart of the circuits. The conventional diagram of current starved VCO is shown in Fig. 2. The circuit includes two parts, the inverter stage and current starving circuits. The design intention of these circuits is to reduce power and phase noise of the CSVCO with a desired frequency of oscillation, subjected to physical constraint. This circuit functions is same as a ring oscillator, here various stages i.e. three, five, seven stages etc, ring oscillator is used and a control voltage (Vctrl) is inputted with a supply voltage of 1-2 V applied in the circuits which extremity the current available to the inverter circuits. In other words, the inverter is starved for current. The oscillation frequency of current starved VCO for 'N' is represented as

$$f = \frac{1}{2N\Gamma} \quad (1)$$

Where f is the frequency of oscillation of CSVCO and $\Gamma=t_1+t_2$ and N is the number of stage.

To determine the total capacitance equation of CSVCO is represented as

$$C_{tot} = C_{out} + C_{in} \quad (2)$$

$$C_{tot} = C_{ox}(W_pL_p + W_nL_n) + \frac{3}{2}C_{ox}(W_pL_p + W_nL_n)$$

$$C_{total} = \frac{5.C_{ox}(W_pL_p + W_nL_n)}{2} \quad (3)$$

Where C_{ox} is the oxide capacitance and W_p & W_n are the width of PMOS and NMOS respectively, L_p & L_n are the length of PMOS and NMOS respectively [19][21]

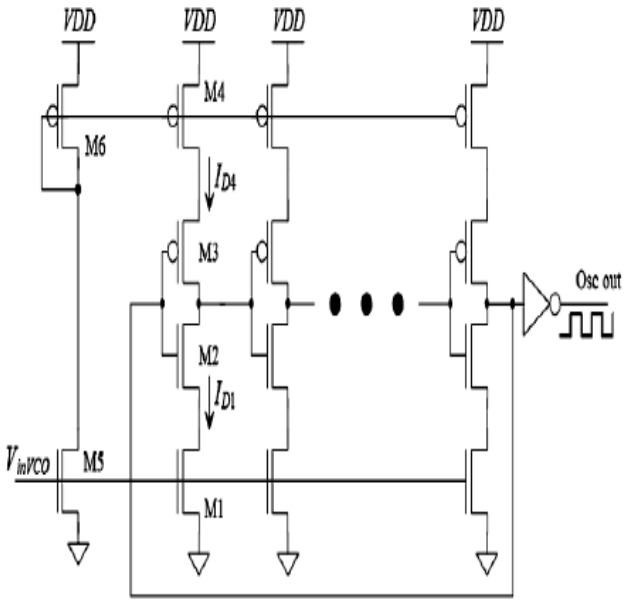

Fig. 4. Conventional current starved VCO [22]

Fig.4 shows the conventional current starved voltage controlled oscillator which consists of input stage where the controlled voltage Vctrl is provided followed by odd number of inverter stage i.e. three, five, seven etc. along with the output stage which output voltages is feedback to the phase detector circuits. In the design of Phase Locked Loop one more VCO is used i.e. LC Voltage Controlled Oscillator or source coupled VCO in which Current Starved VCO results the better phase noise with low power consumption. A VCO control signal is an often used external acquisition aid, while the PLL is not phase locked as the output of the VCO is fed to the phase detector circuit which helps to locked the phase with suppressed jitter. It is widely used in various applications such As in control system and wireless communication.

IV. CONCLUSION

Here in this paper a comparative study is done on various trends in Phase Locked Loop. At the end we conclude that we found that the Digital phased locked loop have result in good phase noise performance with low power consumption with improved tuning range as compared to other phased locked loop circuits Phase locked loop have vast application like communication, networking, control system and also our daily life. Already we design and simulate phase locked loop in different paper about three, five and seven stage current starved voltage controlled oscillator. Here we include how PLL increase in technology day by day. Three components are needed to make a PLL design which is phase detector, loop filter, VCO. The voltage controlled oscillator contain huge range of bandwidth which is used for many wireless application such as transmitter, receiver etc.

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