Phase And Frequency Detector For Low Jitter And High Speed Applications-Review

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Abstract

This paper delineates the performance and comparisons of several architecture methodologies for the high phase noise performance and high speed phase frequency detector (PFD) with a penalty of low power consumption. PFD plays a significant role on whole Phase Locked Loop system (PLL).PFD having an advantageous function over the phase detector (PD) and frequency detector (FD) by detecting phase and frequency detection at a time.PFD is the crucial block for the generation of qualitative clock signal in PLL system. This paper hashes out regarding design challenges of PFD at higher frequencies namely phase noise, jitter, power consumption and area. The proposed design methodology will be the Phase and frequency detector by using transmission gates for low power and high speed PLL applications with an incredible phase noise and Jitter performances. The proposed PFD can be utilized in PLL applications up to 5GHz with low power consumption.

1. Introduction

Generation of a qualitative clock signal is one of the design challenges in all communication systems applications. Due to the unique identity PLL has become an essential block in the generation of high quality clock signal [1]. this paper mainly focusing the performance of non-linear device PFD. The role of PFD is to compare two stimulate frequencies, in terms of phase and frequency and yields two output signals [1]. The contribution of phase noise and jitter due to PFD are analyzed carefully and methodically. Inputs of PFD are (Reference clock) REFclk and (Voltage Control Oscillator clock) VCOclk.

PFD compares input signals in terms of phase and frequency. Based on this comparison PFD generates two non complimentary outputs those are UP and DN. Yielded output signals of PFD fed to the charge pump (CP) and loop filter consecutively. Detection of phase and frequency on the inputs of PFD will influence the Control voltage of VCO. Finally VCO output gives a clock signal with an optimum phase noise and jitter.

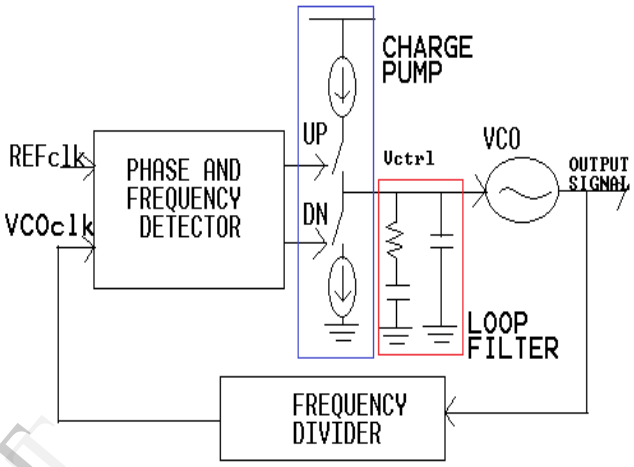

Fig 1. Block diagram of PLL.

2. Traditional PFD and Design Challenges

PFD having an advantageous function over phase detector (PD) and frequency detector (FD) because of PFD (Phase and Frequency Detector) detects both phase and frequency at a time. Detection of phase variation is a major concern because it affects overall performance of PLL such as jitter, phase noise, dead zone and lock-time [2].Traditional PFD architecture is implemented based on concept of finite state machine of three states [1]. Operation of conventional PFD described below by using State diagram shown in figure 2.

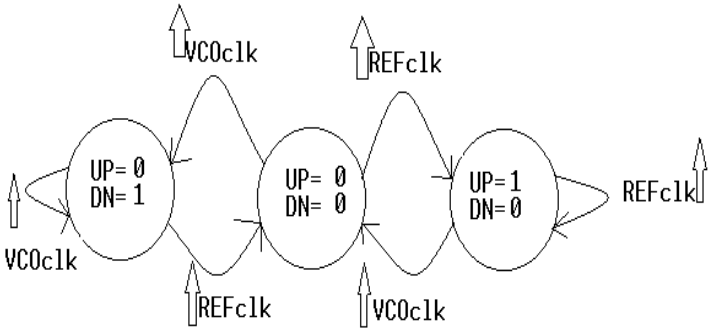

Fig 2. Three state finite state machine diagram.

State machine having two non-complementary outputs UP and DN. which gives the response based on the corresponding

inputs REFclk and VCOclk. If the REFclk leads by VCOclk having same frequency then output signal UP pulse leads than DN by phase difference present between input signals. UP = "1" and DN = "0". Similarly if VCOclk lead by REFclk then DN pulse leads than UP. i.e. UP = "0"and DN = "1" if both signals having same frequency and phase then UP = "0"and DN = "0". Functioning of sequential circuits mainly depends on triggering edge either raising or falling times [3].

Design challenges in PFD architecture are as follows: exhibiting of accurate functional behavior, deviation of threshold crossings at high operating frequency and trade off between phase and power consumption. On the whole PFD suffers from three problems first one is blind zone or dead zone [4]. This problem arises when PFD is not able to detect a very small phase difference on the inputs Due to delay mismatching and circuit mismatching. Second problem is due to the deviation threshold crossings from the ideal case is called Jitter [5]. Fluctuations of threshold crossings mainly because of supply variations and substrate interference with outputs [6]. And third problem in the PFD is power consumption and phase noise tradeoff. Noise is important and major concern parameter in PFD performance. Phase noise performance is always inversely proportional to the power consumption by the device.

3. Existing PFD Architectures Review

Several design topologies are developed based on the concept of state diagram which is having three states. Conventional PFD architecture designed with D- Flip Flop (DFF) and a reset path using Nand gate [1]. Due to its delay mismatches because of reset path DFF based PFD sufferers with dead zone.DFF based design become complex and its internal nodes are not fully discharged, leads to more power consumption. Phase noise performance degrades greater because of tradeoff between power consumption and phase noise performance. Effect of phase noise pulls back the DFF PFD performance. Modified-PFD (Mt-PFD) brought down the complexity of conventional PFD and alters the configuration of tri-state PFD (TSPFD) using 16 transistors. Mt-PFD preserves the conventional characteristics till 300MHz [7].

A fully differential PFD topology grew with an AND gate and a NOR gate having better phase noise as compare to modified and DFF based PFD .due to the circuit complexity it consumes more power and differential PFD is free from dead zone [8]. Falling edge PFD (FE-PFD) existed with an improved performance due to further modifications on Mt-PFD. FE-PFD design composed using only 12 transistors [9]. In FE-PFD total operation depends on the falling edge of the inputs and maximum operation is on at higher voltage levels. If maximum operation of device at higher levels then dives may not reproduce the correct conventional function at higher frequencies.GDI cell based PFD brought down the circuit complexity with only 4 transistors [10]. Maximum operating frequency high as compare to the previous designs and its power consumption very small because of simple topology.

4. Proposed design methodology

Proposed design methodology will be the Phase and frequency detector for high speed and low jitter applications with low power dissipation. This paper comprises investigation of several parameters such as maximum operating frequency, phase noise, jitter, power consumption and area.

Maximum operating frequency is defined as the shortest period conveying functional behavior with correct UP and DN signals united with same and 90 degree phase difference on the input signals [11]. FE-PFD has incredible phase noise performance with low power consumption. But FE-PFD has maximum operating frequency up to 2.5GHz only. As we discussed earlier section FE-PFD maximum operation is at higher voltages based on the falling edge concept but circuit internal nodes are not fully charged and discharged along with inputs at higher rates, results the outputs may not exhibit with correct operation. In proposed methodology when device operate its maximum operation at lower voltages internal nodes are easily charge and discharge with speed. Due to this circuit maximum operating frequency almost double as compare to FE-PFD design i.e. 50% speed of operation increased.

Phase noise in one of the pulverizing parameter in PFD performance. A short term random frequency fluctuation with phase instabilities called Phase noise [12]. Jitter and phase noise mainly due to the presence of correlated & non correlated noises such as substrate & supply noise and thermal noise respectively [13]. In single ended CMOS the maximum channel noise in terms of amplitude and phase exist when the both input and output are at half of the supply voltage i.e. Vdd/2. Amplitude noise can be attenuate by amplitude limited theorem but not phase noise [14]. Among all topologies FE-PFD having good phase noise performance. Phase noise equation suggested by Hajimiri [13].

$$L(f) = \left[\frac{8}{3n} * \frac{kT}{P_{avg}} * \frac{V_{dd}}{V_{char}} * \frac{{f_o}^2}{\Delta f^2}\right] \quad (1)$$

V_{char} =Characteristic voltage of the device.

$V_{char} = \Delta V/\gamma$ For long channel devices.

k =Boltz mans constant.

T =Absolute temperature.

P_{avg} =Average power consumption.

Good phase noise performance is achieved from above equation (1) by lowering threshold voltages and consuming more power. Minimal phase noise is inversely proportional to the power consumption and grows with operating frequency [15]. Phase noise power consumption and frequency are having tradeoff. So choose an offset frequency where the

phase noise and power consumption having optimal tradeoff or dependency.

A short term random variations of threshold crossing over a period of time called jitter [6]. Generally quality of a clock signal is measured by the jitter and phase noise. The presence of jitter in the PFD will shows noisy operation. Jitter exists in PFD due to the supply fluctuations and substrate interferences with outputs. The reasons behind these fluctuations of threshold crossings are due to susceptibility to supply and substrate coupling with output clock signal. Supply fluctuations with respect to time is changes gate propagation delays leads to time changes at V_{th}.similarly substrate is coupled with C_{db} parasitic onto device output voltage wave form [6].

Propagation delay $\tau_d = C_L V_{th}/I_0$ (2)

I_0 =Driving strength

V_{th} =Threshold voltage

C_L =Load capacitance.

$\tau_{d_{inv}}$= Propagation delay of each inverter

$\tau_{d_{tx}}$=Propagation delay of each transmission gate

From the above equation (2) the effect of threshold voltages leads to change in propagation delays and speed of operation.

5. Conclusion

Consideration of all above parameters such as maximum operating frequency, power consumption jitter and phase noise. Design of three state PFD concept using transmission gate can hold all the proposed design methodologies. Transmission gates design composes 12 transistors even complex circuits also. Transmission gate is the unique solution towards voltage-drop problem and rail to rail swing. Rising of signal amplitude is one of method for improving phase noise performance. Jitter performance of PFD improved. Because of most preferable function of transmission gate in sight of Jitter is to rid of power supply variations. Designing o f PFD with all consideration above proposed methodologies that PFD will be superior to all previous designs.

Table 1 Comparative study on different topologies.

Topology	Phase noise (dBc/Hz	Maximum operating frequency (Hz)	Power consumption	No of transistors	Operating voltage	Dead zone	Jitter	Technology
Conventional PFD(TSPC)	-31	800MHz	33.5uw	48	3.3v	100ps	Not given	0.3um
Differential based PFD	-95	2.4GHz-10GHz	3.7mw	38	1v	Free	Not given	0.13um
Mt-PFD(modified PFD)	-131.5	1.5GHz	10uw	16	1.8v	Free	Not given	0.18um
FE-PFD(falling edge)	-167.8	2.5GHz	6.6uw	12	1.8v	Free	Not given	0.18um
GDI-cell based PFD	Not given	5GHz	8uw	4	1.8v	20ps	Not given	0.18um

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