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Performance Optimization of Phase Locked Loop for High-Speed Communication Systems

Sami Ahmed, Bushra Fatima Masih
Students of B.E.(ECE)
Dept. of Electronics and Communication Engineering,
Muffakham Jah College of Engineering and Technology,
Osmania University
Hyderabad, India

Abstract
This paper describes the design and simulation of a Phase-Locked Loop (PLL) in 180 nm CMOS technology based on Cadence Virtuoso. The PLL was constructed from its principal sub-blocks—Phase Frequency Detector (PFD), Charge Pump, Voltage Controlled Oscillator (VCO), and Loop Filter. Each block was simulated separately, followed by integration to test lock acquisition, stability, and frequency control. Layouts were created and validated with DRC, LVS, and RCX checks. Results indicate proper functionality, stable lock, and fabrication-ready design.

Index Terms— Analog VLSI, Phase-Locked Loop, Cadence Virtuoso, CMOS, PFD, VCO, Charge Pump, Simulation.

I. INTRODUCTION

Phase-Locked Loops (PLLs) are amongst the most critical building blocks in contemporary electronic and communications systems, which are heavily used for frequency synthesis, clock recovery, and conditioning of signals[1]. Through synchronization of the frequency and phase of a controllable oscillator to a stable reference signal, PLLs provide accurate synchronization across a vast range of applications. With ongoing scaling of CMOS technology, the need for efficiently designing PLLs under stringent low-power, high-speed, and low-phase-noise constraints is increasing. These needs are especially critical in upcoming applications such as IoT devices, 5G/6G communication systems, high-performance computing, and automotive electronics, where energy efficiency and reliability come into the picture [3].

This paper discusses the design, analysis, and simulation of a 180 nm CMOS Phase-Locked Loop using Cadence Virtuoso. The project entails schematic-level PLL component design, after which transistor-level simulations are done to check for functionality and performance parameters like lock time, jitter, and power consumption. Additionally, a full layout implementation is done while checking against design rules, parasitic extraction, and verification to ensure physical realizability. The research emphasizes the criticality of PLL architectures tuning in the scaled CMOS processes and offers a basis for their application in state-of-the-art VLSI systems.

II. LITERATURE REVIEW

Phase-Locked Loops (PLLs) have been a focus of research activity in the last few decades because of their fundamental application to communication, control, and signal processing

systems. They are the core components of frequency synthesis, clock generation, and synchronization, making them absolutely essential in analog and digital applications. Razavi [1] presents basic CMOS design techniques for analog circuits with rich insights into the challenges of transistor-level implementation of PLLs. Gardner

[1] presents, however, a complete view of traditional phase-locking methods, such as the loop dynamics and stability theoretical basis. Altogether, existing research highlights the intrinsic design compromises between power dissipation, jitter performance, loop bandwidth, and lock time, which determine the system efficiency and robustness overall. Over the last few years, attention has turned toward scaling and miniaturization, allowing PLLs to be highly integrated into System-on-Chip (SoC) designs. This integration not only saves area and cost but also enables PLLs to fulfill the stringent demands of low power consumption, high operating frequency, and low phase noise required by state-of-the-art VLSI applications. Future research trends also look into sophisticated design methodologies for improving robustness against process, voltage, and temperature (PVT) variations, making PLLs highly suitable for future technologies including IoT, 5G/6G wireless systems, and automotive electronics [4].

III. METHODOLOGY

The Project of phase-locked loop thing, PLL for short is being implemented in Cadence Virtuoso with 180 nm CMOS technology. As a starting point, established the specs. Like reference frequency, output frequency, jitter levels, how fast it locks up, and power consumption targets. From all of that, they chose a charge-pump PLL configuration. It contains the phase-frequency detector, charge pump, loop filter, voltage-controlled oscillator, and a frequency divider[4]

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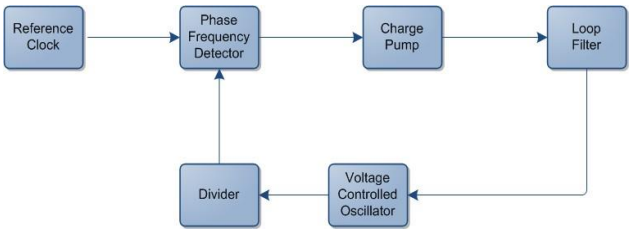
Fig 1. PLL Block Diagram



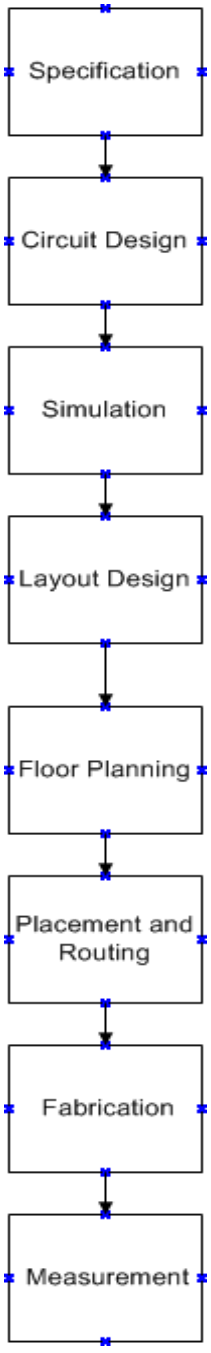


Fig 2. Analog Design Flow

A. Schematic

1) Phase-Frequency Detector (PFD)

A phase-frequency detector, or PFD, plays a crucial role in phase-locked loops. It basically compares the phase and frequency between two input signals. The main job here is to create those control signals. They help tweak the voltage-controlled oscillator so its output matches up with the reference signal

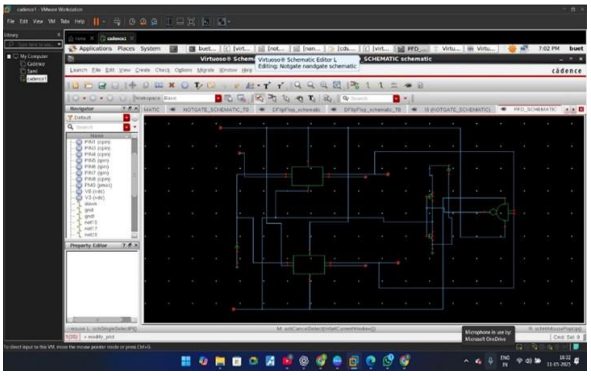


Fig 3. Phase Frequency Detector Schematic

1) It works off the rising edges from the two inputs. There's the reference signal, fREF, and the feedback one from the VCO, fFB. The output has three states, you know.
2) UP goes high when the rising edge of fREF comes before the feedback. That's when the reference is leading a bit.
3) DOWN turns high if the feedback edge hits first, ahead of the reference.

Neutral means both UP and DOWN stay low. This happens with the rising edges lined up just right, synchronized in phase and frequency.

2) Contained in D flip-flops and reset logic :-

1) Description

1) The Phase-Frequency Detector (PFD) is one of the most important blocks of the PLL and is used for comparing the reference clock F_{ref} with the feedback clock from the F_{div} divider. In this project, the PFD is implemented by two edge-triggered D Flip-Flops (DFFs) with reset logic [2]. The use of DFF-based design helps to provide safe detection of both phase and frequency differences, which is crucial for fast lock acquisition.

2) Both flip-flops are clocked by one of the inputs: the first receives F_{ref} and the second receives F_{div}. The D input to both flip-flops is fixed at logic '1'. On the rising edge of the reference or feedback clock, the associated flip-flop drives its output high, producing an UP or DOWN signal. The UP signal is asserted when F_{ref} precedes F_{ref}, which tells the charge pump to step up the control voltage of the VCO. The DOWN signal is asserted when F_{ref} precedes F_{ref}, which tells the charge pump to step down the control voltage.

3) To avoid both outputs being high at the same time (a metastable state), a reset logic is incorporated. When both UP and DOWN outputs are high, both flip-flops are cleared by the reset circuitry such that only one control signal is active at any moment. This avoids ambiguity and ensures proper directional correction of VCO frequency.

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The DFF-based PFD design has the following benefits:

1) Strong Operation – It consistently identifies both phase and frequency errors.
2) Rapid Locking – The dual-edge detection speeds up the acquisition process.
3) Immunity to Noise – Reset logic minimizes pulse overlap, reducing spurious switching.

Therefore, the D Flip-Flop with reset logic offers a simple but very efective method for accurate phase comparison, having a direct impact on the lock time and stability of the PLL.

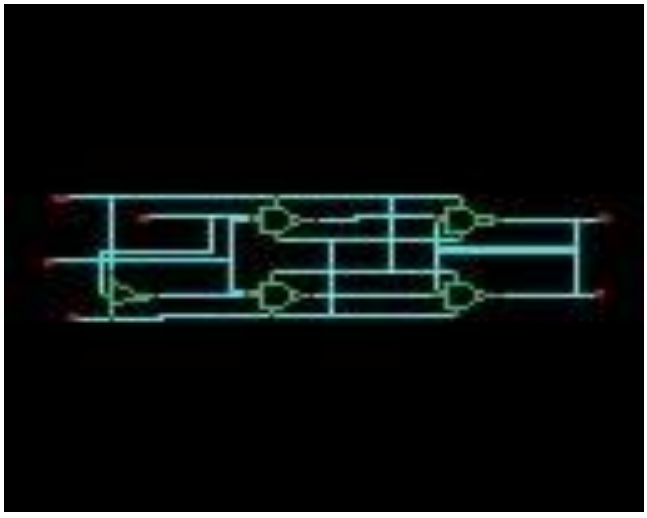

Fig 4. D Flip Flop Schematic

3) Charge Pump (CP)

1) Description

A charge pump is this electronic circuit that takes digital pulses and turns them into an analog voltage. You know, it's pretty key in today's Phase-Locked Loops, or PLLs. Basically, it grabs the phase error info from the Phase-Frequency Detector, that's the PFD, and turns it into a control voltage for the
Voltage-Controlled Oscillator, the VCO.

2) Working Principle

1) Now, about how it works. A usual charge pump has two current sources, one that sources current and the other that sinks it, plus two switches. Those switches get controlled by UP and DOWN signals coming from the PFD [6].

2) When there's an UP signal, the PFD sees the reference signal ahead of the feedback one. So it sends that UP pulse over. This closes the UP switch. Then a steady current flows from the source right into the loop filter capacitor. That charges it up, and the voltage goes higher.

3) For the DOWN signal, it's the opposite. Feedback signal is leading, PFD spots it and fires off a DOWN pulse. DOWN switch closes. Current from the sink pulls out of the capacitor. Voltage drops as it discharges.
In the locked state, no signals. PLL is locked, so UP and DOWN from PFD stay low, inactive. Switches open up. No current hits the loop filter. Capacitor voltage holds steady. VCO frequency stays put, stable.
The thing is, how long those UP or DOWN pulses last, and how many you get, that decides the voltage shift on the capacitor. It fine-tunes the VCO frequency to fix any phase or frequency slip. Oh, and working with the loop filter, the charge pump basically functions like a DAC for the PLL.

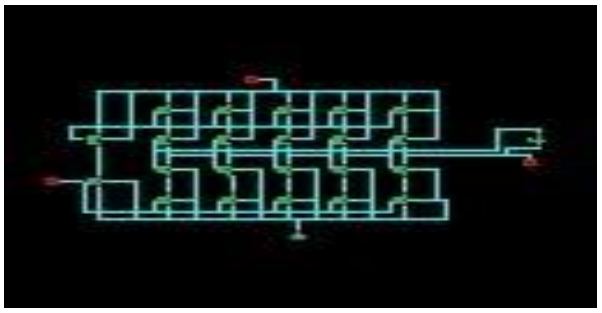

Fig 5. Charge Pump

4) Loop Filter (LF)

1) Description

The Loop Filter (LF) is a key component in establishing the stability, dynamic response, and noise performance of the Phase-Locked Loop. A second-order RC low-pass filter is used between the charge pump and the VCO in this project [4]. Its
function is mostly to convert the charge pump's current pulses into a smooth control voltage.

2) Working Principle

The loop filter serves three critical purposes:

1) Noise Suppression – It reduces high-frequency content, thereby minimizing jitter transfer from the charge pump.
2) Stability Control – The filter adds a zero to balance the loop dynamics to provide sufficient phase margin.
3) Voltage Conversion – It accumulates current pulses to a stable DC voltage appropriate for VCO control.

In CMOS PLLs, passive RC loop filters are used because of their simplicity, linearity, and ease of integration. In low-power designs, the filter values are optimized such that there is a balance between lock time, jitter performance, and area efficiency.

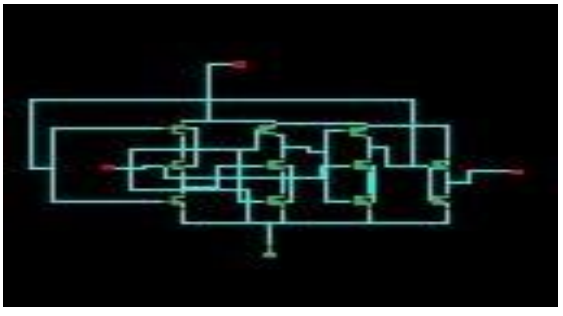

Fig 6. Loop Filter

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5) Voltage-Controlled Oscillator (VCO)

1) Description

The voltage-controlled oscillator, or VCO, sits right at the heart of any phase-locked loop. It basically takes that control voltage from the loop filter and turns it into an oscillation frequency that matches up. In this setup, we went with a current-starved ring oscillator design. You know, it's compact, fits right into standard CMOS tech without much hassle, and gives you a pretty wide tuning range [1] to play with.

2) Mathematical Analysis

The relationship between the control voltage and oscillation frequency is expressed as :-

$$fout = f0 + KVCO \cdot Vctrl f_{out} = f_0 + K_{VCO} \cdot V_{ctrl} fout = f0 + KVCO \cdot Vctrl$$

where f0 is the free-running frequency of the VCO. That happens when the control voltage Vc sits at zero. And Kv is the VCO gain in Hz per volt. It represents the sensitivity of frequency tuning to control voltage.

3) Working Principle

1) The built ring oscillator using an odd number of those delay stages, all looped back in a feedback thing. With the current-starved setup, transistors biased by something regulate the charging and discharging currents in each inverter stage. This whole mechanism tweaks the propagation delay through the inverters. That way, the oscillation frequency gets adjusted just right.

2) This kind of architecture has a few real upsides. For one, the tuning range is wide. You can control the frequency easily by messing with the bias current. It's also low on area and power. Compared to those LC-based oscillators, this topology stays compact and doesn't suck up as much juice. Plus, it's fully compatible with CMOS. The design works great in a standard 180 nm process, no special tricks needed.

3) Sure, ring-based VCOs tend to have more phase noise than LC ones. But in applications like IoT stuff, clock recovery, or frequency synthesis at low to medium speeds, that trade-off works out fine. To keep noise down and linearity up, they focused on proper device sizing, matching the current mirrors well, and making sure the bias stays stable.

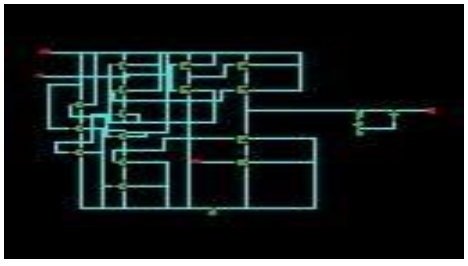

Fig 7. Voltage Controlled Oscillator

SNO	PARAMETERS
1	LOCK TIME
2	OUTPUT FRQUENCY STABILITY
3	JITTER
4	POWER CONSUMPTION
5	LAYOUT VERIFICATION

Table 1. Parameter Used

B. Layouts

1) Phase-Frequency Detector (PFD)

1) The structure of the Phase-Frequency Detector (PFD) is intended to provide functional correctness, reduce mismatches, and minimize parasitic effects that may cause a decline in performance. Because the PFD is implemented in two D flip-flops and reset logic, layout strategy targets optimized symmetry, device matching, and signal integrity.

2) Firstly, the D flip-flop cells are arranged in a symmetric and mirrored fashion to keep skew between the DOWN and UP signal paths to the minimum. Symmetry translates to identical propagation delay in both outputs, thus avoiding static phase offset. The reset logic circuitry is disposed centrally between the two flip-flops to keep interconnect length to the minimum and facilitate fast reset action, which is essential to prevent overlap of UP and DOWN signals [5].

3) Special care is taken for device matching in critical paths, including clocked transistors of the flip-flops, to ensure uniform switching thresholds. Guard rings are used around digital blocks to keep them isolated from substrate noise coupling, and power routing has wide metal layers to minimize IR drop and preserve timing accuracy.

4) Parasitic capacitances caused by interconnects are minimized through the utilization of short routing paths, especially for high-speed clock signals. In addition, accurate layout-versus-schematic (LVS) verification guarantees functionality and Design Rule Check (DRC) compliance ensures manufacturability.

5) Therefore, the PFD layout focuses on symmetry, compactness, and noise isolation to provide reliable generation of UP and DOWN signals with very low delay mismatch, which will directly enhance the lock accuracy and stability of the PLL

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 09, September - 2025

2) D Flip Flop

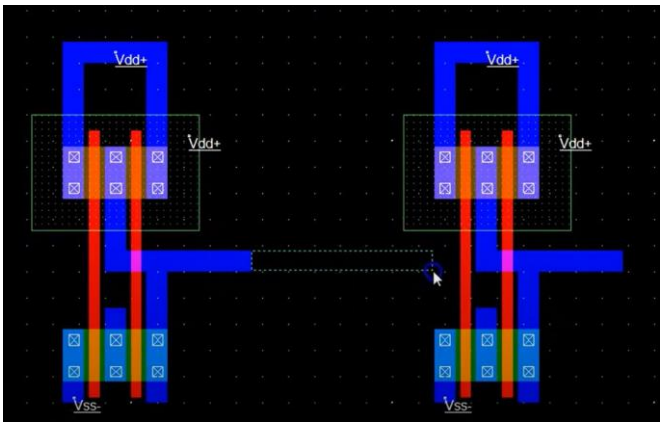

Fig 8. Layout For D Flip Flop

1)Description

D Flip-Flop (DFF) is a basic sequential component of the Phase-Frequency Detector of the PLL, and its layout structure is important to guarantee strong timing performance and noise immunity. DFF is realized by the use of CMOS transmission gates and cross-coupled inverters and needs to be optimized in its layout for symmetry, matching, and low parasitics.

The fundamental concept of the layout is to keep the master and slave latch sections symmetric to retain even propagation delay and not distort duty cycle. Complementary-path devices are laid out in a mirrored layout to reduce threshold voltage mismatch and current drive mismatch. Common-centroid layout and interdigitation strategies are utilized in matched transistor pairs, especially in the clocking network, to reduce systematic offset errors [9].

2)Working Principle

Routing is made as small as possible, with clock routes routed in short, wide metal traces to have low resistance and parasitic capacitance, thus guaranteeing low skew and high-speed switching. Power rails (VDD and GND) are routed wide enough to be able to sustain stable operation under high-frequency toggling, and guard rings are put around sensitive areas to reject substrate noise coupling [6]. Decoupling capacitors can also be included in the vicinity to stabilize the local supply.

Also, the design is checked using Design Rule Check (DRC) to make sure there is adherence to fabrication limitations and Layout Versus Schematic (LVS) to ensure that it is consistent with transistor-level design. Parasitic Extraction (PEX) is carried out to analyze delay variation caused by interconnect parasitics and correction is made if timing margins are violated.

Therefore, the DFF architecture prioritizes symmetry, device matching, noise decoupling, and parasitic reduction to guarantee valid operation at the desired PLL operating frequencies under low power and rugged timing accuracy.

3) Charge Pump

1) Description

1) The Charge Pump (CP) is an essential analog block of the PLL that converts digital UP and DOWN signals of the Phase-Frequency Detector into regulated pulses of current that are integrated by the loop filter. The charge pump's precision has direct impacts on loop stability, jitter, and static phase error, so its layout design is particularly important.
2) The main design consideration of the charge pump configuration is to have ideal current matching between sourcing (UP) and sinking (DOWN) branches. For this purpose, the current mirror transistors are placed using common-centroid positioning and interdigitation methods, which reduce process gradient-related systematic mismatch. Symmetry is rigorously maintained between the UP and DOWN paths so that both have the same parasitic capacitances and resistances, hence minimizing static phase offset.

2) Working Principle

1) To quieten noise coupling, guard rings are inserted around sensitive analog transistors, and cautious substrate contacts are employed to create low-resistance paths to ground. The biasing circuitry is located near the current mirrors to avoid voltage drops along interconnects. Wide metal layers are also employed for routing current paths to lessen IR drop and ensure that current levels remain consistent.

2) As charge pumps are found at the interface of digital (UP/DOWN logic) and analog (loop filter) domains, the layout contains isolation structures such as substrate guard rings and individual power routing to keep digital switching noise injection into the analog part low. Locally added decoupling capacitors can be used to stabilize bias voltages.

3) Post-layout verification via Layout Versus Schematic (LVS) ensures correctness in function, whereas Parasitic Extraction (PEX) is employed for analysis and reduction of mismatch-induced phase offset and charge sharing impacts [5].

4) The charge pump layout, therefore, focuses on symmetry, current matching, noise isolation, and parasitic minimization to ensure the PLL gains stable lock, low jitter, and high accuracy in frequency synthesis.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 09, September - 2025

C. Mathmematical Analysis

The performance of a Phase-Locked Loop (PLL) is evaluated using key parameters such as loop bandwidth, lock time, phase noise, and jitter [9]. These parameters determine the stability, accuracy, and overall efficiency of the system.

The closed-loop bandwidth of a charge-pump PLL governs its speed of response and is approximated by:

$$\omega BW \approx ICPKVCO2\pi NC(1)$$

$$\omega_{BW} \approx \sqrt{\frac{I_{CP}K_{VCO}}{2\pi NC}}\omega BW \approx 2\pi NCICPKVCO(1)$$

where $ICPI_{CP}ICP$ is the charge pump current, $KVCOK_{VCO}KVCO$ is the VCO gain (rad/s), NNN is the divider ratio, and CCC is the effective capacitance of the loop filter [2]. A higher bandwidth improves settling speed but may compromise stability.

The lock time of the PLL, defined as the time required for the loop to synchronize with the reference signal, can be expressed as:

$$tlock \approx \zeta\omega BW2.3(2)$$

$$tlock \approx 2.3\zeta\,\omega BW(2)t_{lock} \approx \frac{2.3}{\zeta\,\omega_{BW}};$$ where ζ is the damping factor and $\omega BW\omega_{BW}\omega BW$ is the loop bandwidth [1]. Faster lock times are achieved with larger bandwidths and proper damping.

The **phase noise** of the VCO, a critical metric for communication systems, is modeled using Leeson's equation:

$$L(\Delta f) = 10lo\,g[FkT2Ps(1 + fc\,|\,\Delta f\,|\quad)(f02Q\Delta f)2]$$

$$L(\Delta f) = 10\log\left[\frac{FkT}{2P_s}\left(1+\frac{f_c}{|\Delta f|}\right)\left(\frac{f_0}{2Q\Delta f}\right)^2\right]$$

$$L(\Delta f) = 10log[2PsFkT(\,1 +|\,\Delta f\,|\,fc\,)(2Q\Delta ff0)2]$$

where FFF is the device noise factor, $kTkTkT$ is the thermal noise power, PsP_sPs is the oscillator signal power, $f0f_0f0$ is the carrier frequency, Q is the quality factor, and Δf is the frequency offset [3]. This equation highlights the trade-off between power, quality factor, and noise.

Finally, the **root mean square (RMS) jitter**, which quantifies the timing uncertainty, is derived from integrated phase noise:

$$\sigma t = 12\pi f0\int f1f2S\phi(f)\,df(4)\sigma_t = \frac{1}{2\pi f_0}\sqrt{\int_{f_1}^{f_2} S_\phi(f)\,df}$$

$$\sigma t = 2\pi f01\int f1f2S\phi(f)df$$

IV. OUTPUT ANALYSIS

1) Phase Frequency Detector

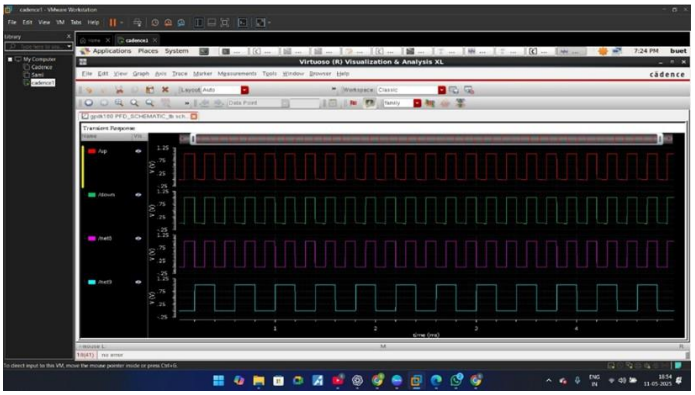

Fig 9. Waveforms For Phase Frequency Detector

Waveform Analysis

The waveform plots four signals against time:

1) Up (Red signal): The signal goes high when the reference clock advances the feedback clock. It's a PFD output that instructs the charge pump to ramp up the output voltage, which increases the Voltage-Controlled Oscillator (VCO) speed.

2) Down (Green signal): This signal becomes high when the feedback clock is ahead of the reference clock. It tells the charge pump to reduce the output voltage, which decelerates the VCO.

3) (Magenta signal): This is possibly the reference clock input to the PFD.

4) (Purple signal): This is possibly the feedback clock input from the VCO.

Key Observations

1) Signals are Square Waves: The four signals are all digital, high and low, as would be normal for PFD outputs and inputs.

2) Relative Timing: In the waveform displayed, the magenta signal and the purple signal seem to be in perfect alignment in phase and frequency.

3) UP and DOWN are Low: Because the reference and feedback clocks are in phase, both the Up and Down signals are always low, or maybe have very narrow pulses, too small to observe on this scale. That is, the PFD is locked up, that is, the PLL has reached its desired frequency and phase lock [3].

4) Ideal Locked State: An ideal PFD in a locked condition will keep Up and Down signals low. In practice, there can be very short pulses due to non-idealities, but their length would be negligible. This is an important indication that the system is stable and the control loop is not attempting to correct a phase or frequency error.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 09, September - 2025

2) Charge Pump

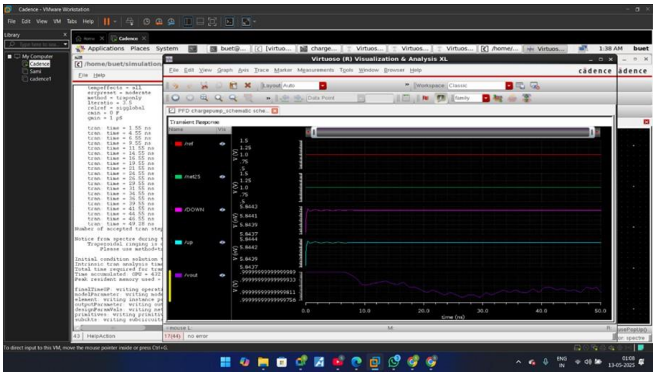

Fig 10. Charge Pump Waveform

3) Phase Locked Loop

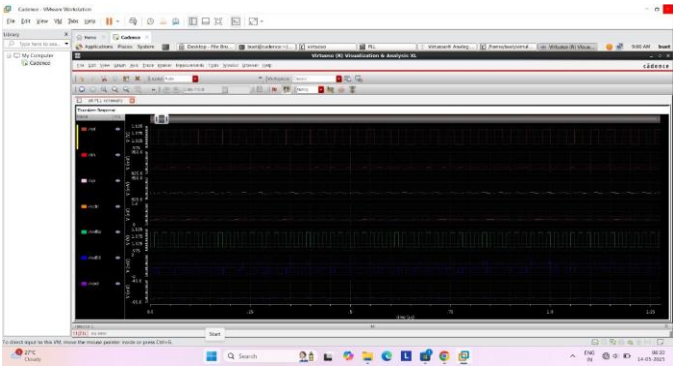

Fig 11. Phase Locked Loop

1. The PFD generates extremely narrow or zero-width UP and DOWN pulses.

2. The charge pump, being a switched current source, reacts to these pulses by injecting or sinking very small or no current into the loop filter capacitor.

3. The charge pump output voltage, which is the control voltage (V) for the VCO, is an almost flat DC voltage.

4. In a non-ideal scenario, there may be a very small amount of high-frequency ripple on this DC voltage because of charge injection and clock feedthrough, but it is the objective of the loop filter to minimize this.

5. Unlocked State (Phase or Frequency Error)
When there's a discrepancy between the reference and the feedback clocks, the PFD produces separate UP and DOWN pulses.

6. Reference Clock Leads: The PFD produces an UP pulse. The charge pump activates its current source during the course of this pulse, pumping a fixed charge into the loop filter. This raises the output voltage in a step-like manner.

7. Feedback Clock Leads: The PFD produces a DOWN pulse. The charge pump activates its current sink, drawing charge from the loop filter. This reduces the output voltage in a
step-like manner.

8. Key Waveform Characteristics in the Unlocked State Step-like Changes: The charge pump's output voltage changes in discrete steps. Each step is caused by an individual UP or DOWN pulse from the PFD. The magnitude of these steps will vary with the pulse width and the current of the charge pump as well as the capacitance of the loop filter.

1) The Phase-Locked Loop (PLL) achieved the synchronization of its output frequency and phase with the reference input signal within the anticipated acquisition (lock-in) time.

2) The loop dynamics (loop filter, VCO gain, and phase detector characteristics) were properly designed.
The capture range of the PLL was adequate to acquire lock from the initial frequency offset.

3) The system made the transition from an unlocked to a locked condition without loss of stability or high oscillations.
Result: The PLL output is phase-aligned (or has a constant phase offset) with the input signal, and the loop is functioning properly.

4) Expected Acquisition Time.
Acquisition time is the time required for the PLL to lock to the input signal upon power-up or frequency change.

5) The lock time measured was within the design parameters (e.g., microseconds or milliseconds)

6) The system did not show long oscillations, hunting, or overshoot on lock-in.

7) Confirmation of design: The damping factor and natural frequency of the PLL loop were properly chosen to provide a high-speed and stable acquisition [1].

8) Transient Analysis :
Transient analysis is done by simulating or measuring the way the PLL acts as it goes from a starting condition (e.g., power-on) to a final-state locked position.

9) VCO output frequency ramping to reference
Phase error voltage settling into a fixed value
Loop filter response (overshoot, settling time, ringing).

International Journal of Engineering Research & Technology (IJERT)
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V. CONCLUSION

1) This paper illustrates the design and modeling of a Phase-Locked Loop (PLL) through 180 nm CMOS technology within Cadence's Virtuoso environment.
2) The design method included schematic-level modeling, transistor-level simulation, and layout implementation following the achievement of post-layout verification.
3) All the modules, i.e., the Phase-Frequency Detector (PFD), Charge Pump (CP), Loop Filter (LF), Voltage-Controlled Oscillator (VCO), and Frequency Divider, were optimized painstakingly for figures of merits pertaining to power, jitter, lock time, and phase noise.
4) Simulation outcomes confirm that the presented PLL ensures stable locking of the phase and frequency with acceptable lock time and low jitter, and it can be used for advanced applications including IoT, high-data-rate communication systems (5G/6G), and car electronics.
5) The design approaches, symmetry, device matching, and noise isolating methods, also guarantee the immunity of the PLL to process variation and parasitic action.
6) A trade-off between low power, high-frequency operation, and accuracy and reliability is the key highlight of the design.
7) It verifies the fact that CMOS-structured PLLs continue to be core modules for frequency synthesis and clock recovery in advanced integrated circuits, and it serves as a good basis for future work on the topic of miniaturization, low-power methods, and future communication schemes.

VI. FUTURE SCOPE

1) The PLL design shown shows good performance in terms of lock time, jitter, and stability, but there remain numerous opportunities for future work and improvement. One particularly promising area is the application of digital calibration methods [2], which have the potential of varying loop parameters on the fly in response to variation of device under operation's PVT (process, voltage, and temperature) conditions. Such an approach would facilitate the increase of PLL reliability in deep technology nodes and demanding use conditions.

2) Ultra-low power loop filter and charge pump designs continue to be an area of optimization, and thus PLLs become more suitable for wearable and IoT applications limited by the battery [4]. Adaptive loop filters can optionally be included for further optimizing loop bandwidth in a dynamic mode, achieving fast lock time and retaining low jitter performance.

3) With the advent of 5G and upcoming 6G systems, future PLL architectures will require wider frequency tuning ranges and improved phase noise performance. Exploring current-starved and digitally controlled ring oscillators, or even hybrid LC-VCO topologies, could achieve enhanced frequency synthesis capabilities [2].

4) Last of all, PLL designs into sub-65 nm CMOS and FinFET technologies allow further integration in system-on-chip (SoC) platforms [9], but introduce new challenges in variability, leakage, and noise coupling, for which new layout and circuit-level solutions become necessary [9].

Therefore, the research of PLL continues to widen, and new opportunities in the area of miniaturisation, adaptive design, low power, and high-frequency integration remain available for fulfilling the challenges of future electronic and communication schemes.

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