Performance Evaluation of Multilevel Inverter using Embedded and Digital Control

S. Shama
Department of EEE
Arunai Engg. College Tiruvannamalai,
India

C. R. Balamurugan
Department of EEE Arunai Engg.
College Tiruvannamalai,
India

Dr. S. P. Natarajan
Department of EIE Annamalai
University Chidambaram,
India

Dr. R. Bensraj
Department of EEE
Annamalai University
Chidambaram, India

***Abstract*— A new topology of cascaded multilevel inverter is proposed in this paper that utilizes eight switches and produces seven level output in symmetric mode of operation. Embedded and digital controllers are the two non- pwm techniques which are employed in these proposed topology. In embedded controller, Codings are used to generate pulse. By using switching table Codings are written. Embedded switching scheme is used to meliorate the functioning of the multi level inverter. While in digital controller logic gates and flip flop are used to generate pulses. This proposed topology produces seven-level inverters which are nearer to the sinusoidal wave. The switching scheme reduces the THD, switching loss and increase output level FFT analysis and output result of the inverter with R-load and RL load has been analyzed by using MATLAB/SIMULINK.**

Keywords* — *Embedded controller, digital controller, non pwm technique, total harmonic distortion(THD).

I.INTRODUCTION

Multilevel inverter is used to convert uncontrolled D.C to controlled A.C. For generation of pulse non pulse width modulation technique is used. This technique is mostly used in Industrial Application. FFT analysis is used to determine the Harmonic analysis for five level inverters. The proposed topology is operated in symmetric mode and produces seven level inverter are nearer to the sinusoidal wave. Naumanen et al [1] the DC link voltage in multilevel inverter fluctuates under load and cannot be considered constant. Voltage fluctuation causes several problem including erroneous voltage vector production and undesired harmonics to voltage and current. Cortes et al [2] developed to predict the value of current for all voltage vector, this control methods uses a discrete-time model of the system due to the large number of voltage vectors available in multilevel inverter. De et al [3] A technique of avoiding reverse recovery loss of MOSFET body diode in a three-level neutral point camped inverter is suggested. The use of multilevel inverter enables operation at high switching frequency Grigoletto et al [4] the algorithm that has been developed within the carrier-based pwm frame work and its implementation in diode clamped converters for four or more levels. Rahim et al [5] developed three reference signals that are identical to each other with an offset that is equivalent to the amplitude of the triangular carrier signal were used to generate the PWM signals. Ghazanfari et al [6] the objective of this study is to extend the attractive features of the cascaded H-bridge voltage source inverters (VSI) to low-voltage and low-power applications. Najafi et al [7] proposed a new topology with reduced number of switches which is used to operate in high power and voltages and improved output waveform quality and flexibility. Kangarlu et al [8] developed to obtain optimal structure in different criteria such as number of switches, standing voltage on the switches, number of dc voltage sources etc. Ebrahim et al [9] proposed at the output, generation of all voltage levels both odd and even many different algorithms are used. Yuanmao Ye et al [10] this topology is designed based on a switched capacitor technique. Capacitor voltage problem is avoided and one dc source is used. Sumit et al [11] proposed using LDN takes the form of a half bridge. During positive and negative cycle without any closed loop control algorithm for the construction of self balancing. Babaei [12] developed this type of inverter is comprised of a series connection proposed basic unit and is able to only generate only positive levels at the output. Reddy et al [13] a generalized multilevel inverter with front-end DC-DC conversation stage followed by synchronized H-bridge is presented. M.R.J Oskuee et al [14] the proposed inverter can generate all levels at the output associated with the lower number of switches.

II. PROPOSED TOPOLOGY

The basic block of proposed multilevel inverter consists of two voltage sources. The proposed topology constitutes 8 switches S_1, S_2, S_3, S_4, S_5, and S_6, S7, S8. Power switches can be implemented using a transistor device insulated-gate bipolar transistor (IGBT)] with an anti parallel diode. The proposed topology is described with the help of a single-phase inverter with two input dc sources V_{dc1} and V_{dc2}. The

proposed multilevel inverter has been analyzed is operated in symmetric mode of operation so V_{dc1} and V_{dc2} must be equal. 100 V is given in both voltage sources. The load is supplied with seven level $+3V_{dc}$ $+2V_{dc}$, $+V_{dc}$, 0, - V_{dc}, $-2V_{dc,}$ $-3V_{dc}$ with R load and RL load are used in this paper and differences are shown in output voltage and output current. Voltage measurement and current measurement are verified. Embedded controller is a device that is used to perform the embedded control. Flip flop and logic gates are used to generate pulse in digital controller. Pulse is given to every switch according to the block diagram.

Table1. represents switching table for seven –level multilevel inverter. Here S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8 represents switches of the multilevel inverter and Vdc represents the input voltage source. To obtain $+3V_{dc,}$ S_1 S_3 S_6 S_8 will be active high and other switches will be S_2, S_4, S_5 and S_7 active low. For $+2V_{dc}$ S_1, S_3, S_4 and S_6 will be active high and rest of the switches S_2, S_5 S_7 and S_8 will be active low. For $+V_{dc}$ S_1, S_6, S_7 and S_8 will be active high and remaining switches $S_{1,}$ S_2, S_3, S_4 will be active low.S_5, S_6, S_7, S_8 will be active high for $0V_{dc}$ reset of the switches For $-V_{dc,}$ S_2, S_3, S_4, S_5 will be active high and other switches will be automatically active low. For $-2V_{dc}$ $S_{2,}$ S_5 S_7, S_8 will be active high and other switches like S_1, S_3, $S_{4,}$,S_6 will be active low. S_2, S_4 and S_5 will be active high S_7, S1, S_3, S_6 and S_8 will be active low for-$3V_{dc.}$ By using this switching table pulses are generated for both embedded and digital controller. This will improve the switching scheme for proposed topology.

TABLE I. SWITCHING TABLE FOR PROPOSED TOPOLOGY

Switching table								Output voltage
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	
1	0	1	0	0	1	0	1	+3Vdc
1	0	1	1	0	1	0	0	+2Vdc
1	0	0	0	0	1	1	1	+Vdc
0	0	0	0	1	1	1	1	0
0	1	1	1	1	0	0	0	-Vdc
0	1	0	0	1	0	1	1	-2Vdc
0	1	0	1	1	0	1	0	-3Vdc

A. Embedded controller

Embedded Controllers (ECs) are mostly used in low power embedded reference designs, performing a range of input/output and system management functions. In these methods, Codings are used to generate pulses by using switching table. Clock, Demux and switches are used in this topology. It is very easy to simulate.

Clock 10 decimation is given as input and fed into the embedded function in which coding are written and 8- input demux is used here which generate pulse by using coding, it fed directly to the switches.

By using external pc the operation of the system is not controlled. Embedded controllers has major role in modern machine and automobile than power control systems. Embedded system is used to specific tasks such as digital watches, MP3 players, traffic lights and factory controllers. Pulses are given to every switches according to the simulated block. Each switch capable of producing pulse by using embedded technique. Fig 1 shows the proposed circuit. Table. I gives the possible switching pattern for the proposed seven level inverter. Switching states of the seven level inverter using embedded and flip flop oriented control are similar. The proposed control strategies are based on bipolar strategies. In non PWM methods variable voltages cannot be obtained.

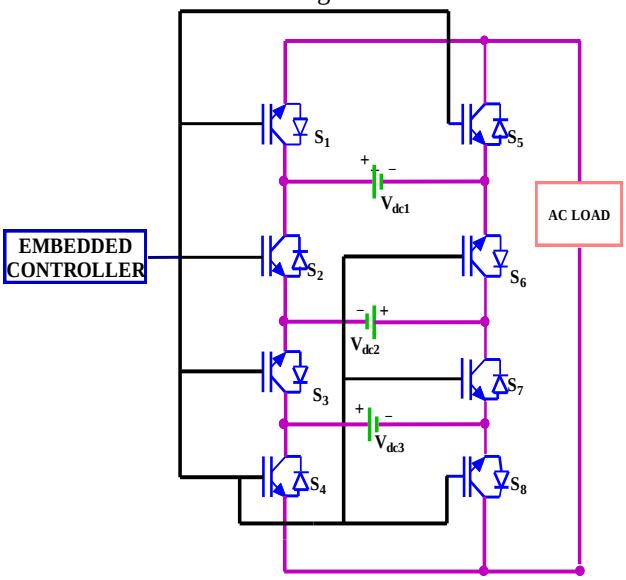

Fig. 1. Block diagram of proposed MLI using embedded control.

Figure2 represent the pulse generation for seven level inverter based on embedded controller. Figs 3 to 10 shows the output voltage, current waveform and FFT plot for R and RL load.

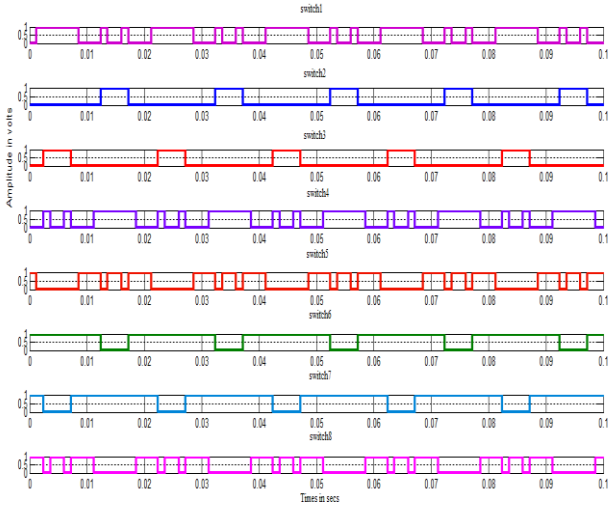

Fig. 2. Pulse pattern for seven level inverter using embedded control.

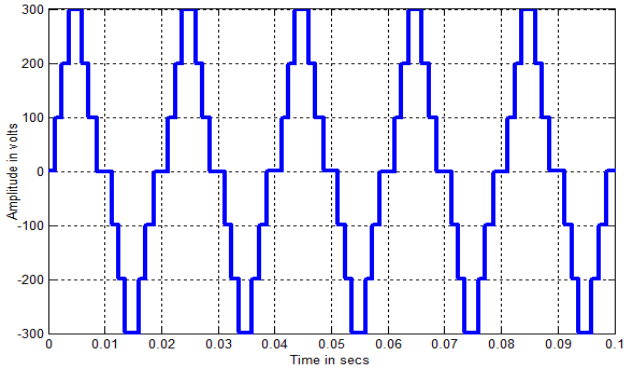

Fig. 3. Output voltage waveform with R load

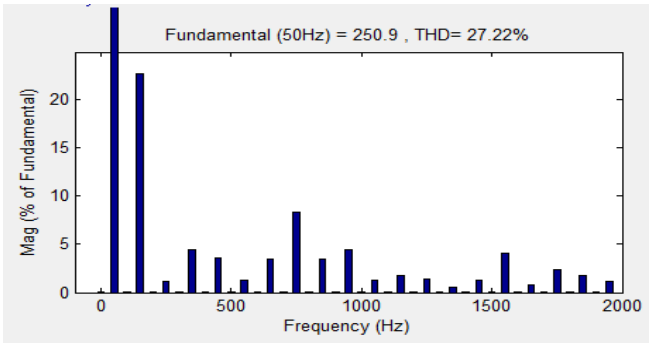

Fig. 4. FFT Analysis with R load (Voltage)

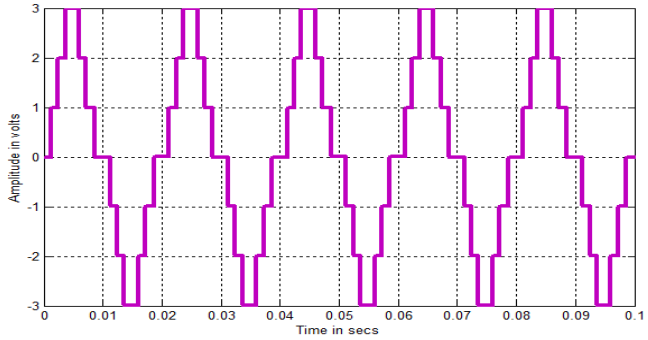

Fig. 5. Current waveform with R load

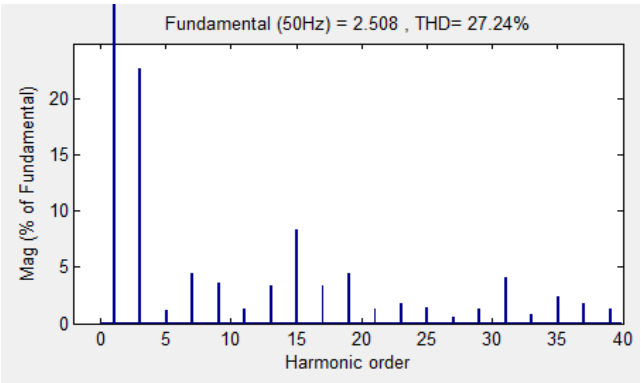

Fig. 6. FFT Analysis with R load (Current).

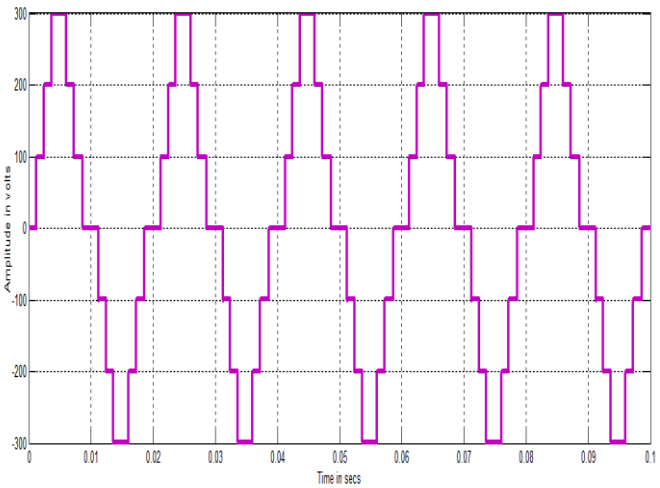

Fig. 7. Voltage waveform with RL load

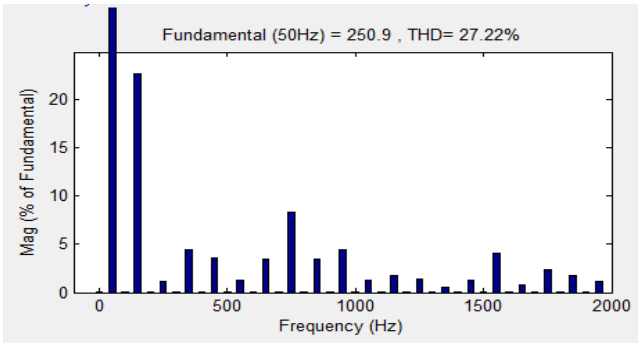

Fig. 8. FFT Analysis for RL load (voltage)

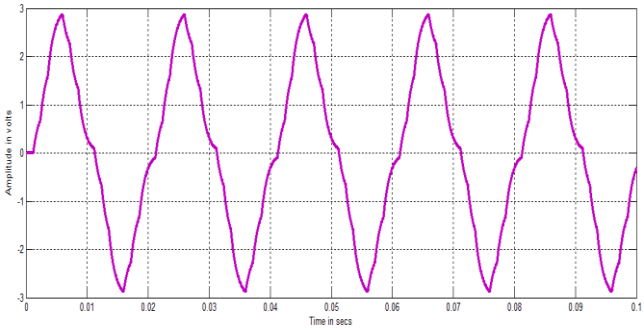

Fig. 9. Current waveform with RL load.

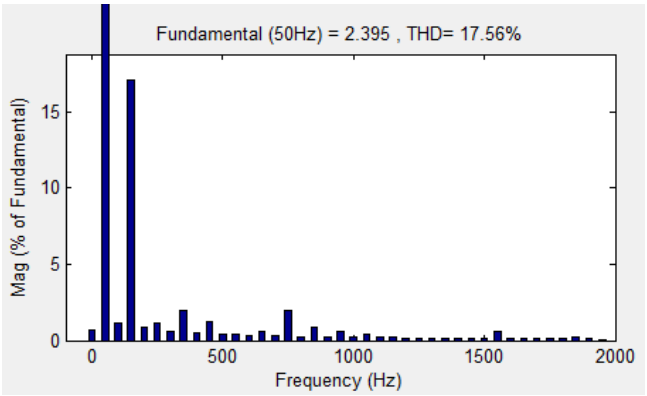

Fig. 10. FFT Analysis for RL load (Current).

B. Coding

```
function y  = fcn(u)
a = mod(u*1000,10);
b = mod(u*1000,20);

if a<1.2 %0
   S1=0;
   S2=0;
   S3=0;
   S4=0;
   S5=1;
   S6=1;
   S7=1;
   S8=1;
elseif a<2.4%
   S1=1;
   S2=0;
   S3=0;
   S4=0;
   S5=0;
   S6=1;
   S7=1;
   S8=1;
elseif a<3.6 %4
   S1=1;
   S2=0;
   S3=1;
   S4=1;
   S5=0;
   S6=1;
   S7=0;
   S8=0;
elseif a<6.0 %5
   S1=1;
   S2=0;
   S3=1;
   S4=0;
   S5=0;
   S6=1;
   S7=0;
   S8=1;
elseif a<7.2 %6
   S1=1;
   S2=0;
   S3=1;
   S4=1;
   S5=0;
   S6=1;
   S7=0;
   S8=0;
 elseif a<8.6 %7
   S1=1;
   S2=0;
   S3=0;
   S4=0;
   S5=0;
   S6=1;
   S7=1;
   S8=1;
 else %0
   S1=0;
   S2=0;
   S3=0;
   S4=0;
   S5=1;
   S6=1;
   S7=1;
   S8=1;
end
if b<10
y=[S1,S2,S3,S4,S5,S6,S7,S8];
else
y=[S4,S3,S2,S1,S8,S7,S6,S5];
```

C. Digital controller

In this method logic gates and flip flop are used to generate the pulse. Pulse are applied to the switches, therefore the circuit is simulated using MATLAB/SIMULINK. Finally, seven-level outputs are generated near sinusoidal wave. JK flip flop is used in this algorithm because only JK flip flop will act as a universal flip flop that is it behaves as other flip flop like RS flip flop, T flips flop, D flip flop, JK flip flop. Constant 1 is given here. JK is nothing but a RS flip flop. Fig.11 shows the flip flop connection for the digital control method. A JK flip-flop is nothing but a RS flip-flop along with two AND gates which are augmented to it. The flip-flop is constructed in such a way that the output Q is AND ed with K and CP. This arrangement is made so that the flip-flop is cleared during a clock pulse only if Q was previously 1. Similarly Q' is AND ed with J and CP, so that the flip-flop is cleared during a clock pulse only if Q' was previously 1.

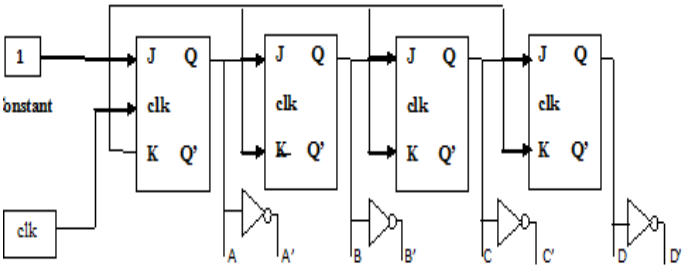

Fig. 11. Schematic Diagram of Flip flop.

D. Logic Gates

Logic gates are formed by using Boolean equation. These equations are deduced from switching table by using logic Friday software. This software is used to work with legacy digital circuits it is applicable only for four bit counter or 16 bit inputs. This type of algorithm is applicable up to 15 levels.

S1=D'CA'+D'B'A+D'B'A'+D'C'B (1)
S2=DCA'+DB'A+DC'B (2)
S3 =DCBA'+DC'B'A+D'CB'+D'C'B (3)
S4=D'C'BA'+DCB'A+DCA'+DC'A (4)
S5=C'B'A'+CBA+D (5)
S6=C'B'A'+CBA+D' (6)
S7=DB'A'+ DCA+ DC'B'+D'C'B'+D'CB (7)
S8=D'B'A'+D'C'A+D'CB+DC'A' (8)

The output of the JK flip flop represent as A A', B B,C C', and D D'. For each switches these output are given as the input to the logic diagram which is formed by using logic gates. Only AND gate, OR gate are used.

Each switch has the separate logic diagram logic gate is a physical device which is used to implement a Boolean function that is; it performs a logical operation on one or more logical inputs and produces a logical output. This logical output is used to produce pulse. This pulse is given to each switch. Actually, there are six switches are constructed in these topology. So, pulse is given to each switch according to the construction of the simulated circuit. Fig. 12 displays the proposed seven level MLI for digital control method.

Finally, the model of the proposed topology is simulated. This topology produces the five level output with reduced Total Harmonic Distortion (THD). Pulse every two switches are shown in simulated mat lab/simulink. Mainly, pulse is generated using flip flop and logic gates. By using JK flip flop and AND and OR gates. Fig. 13 gives the pulse pattern for the proposed seven level inveter using digital control.

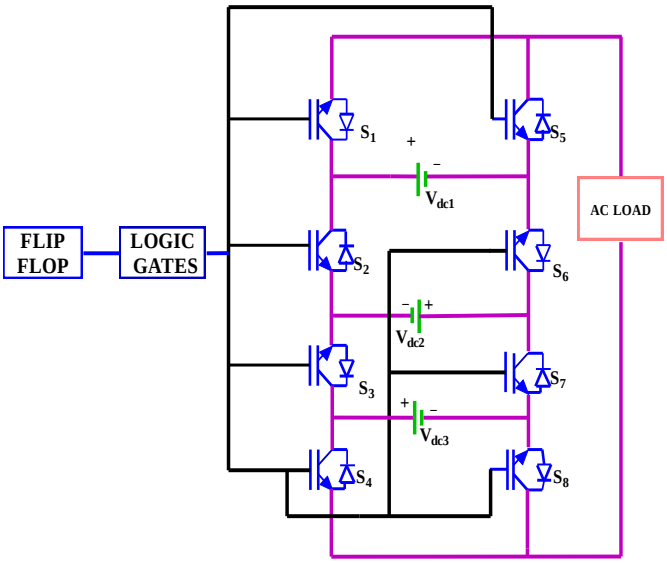

Fig. 12. Block diagram of proposed MLI using digital control.

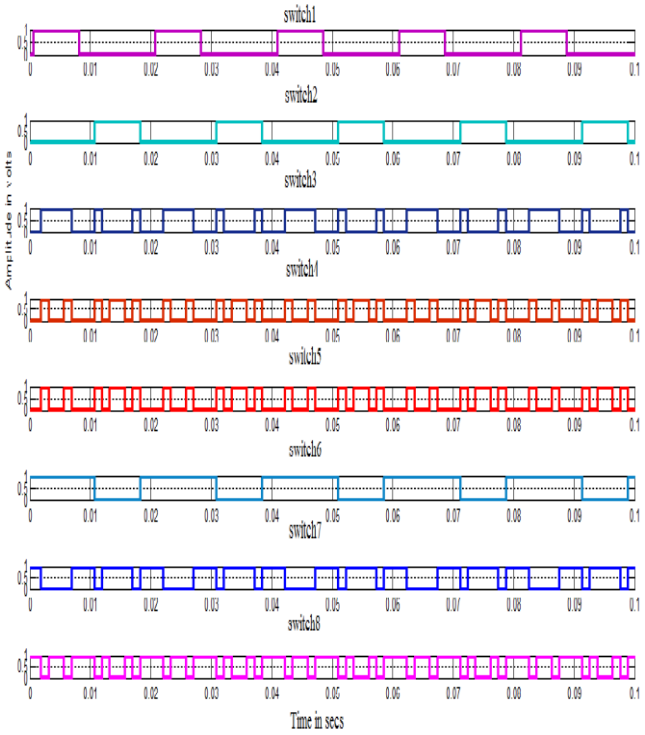

Fig. 13. Pulse pattern for seven level inverter using digital control.

Figs 14 to 21 shows the output voltage, current waveform and FFT plot for R and RL load

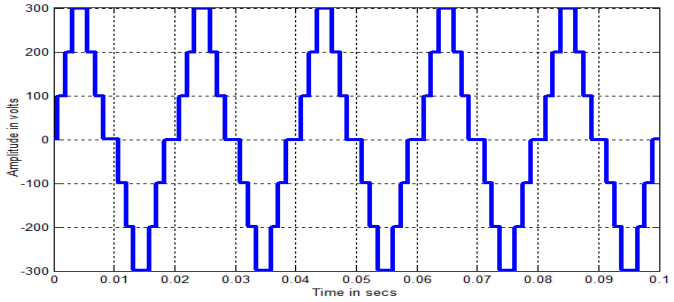

Fig. 14. voltage waveform with R load

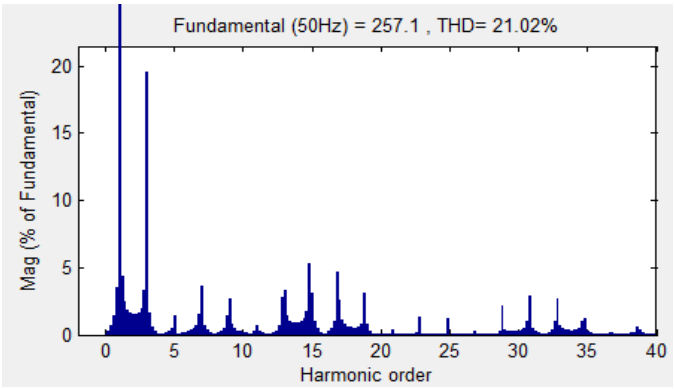

Fig. 15. FFT Analysis for seven level voltage waveform.

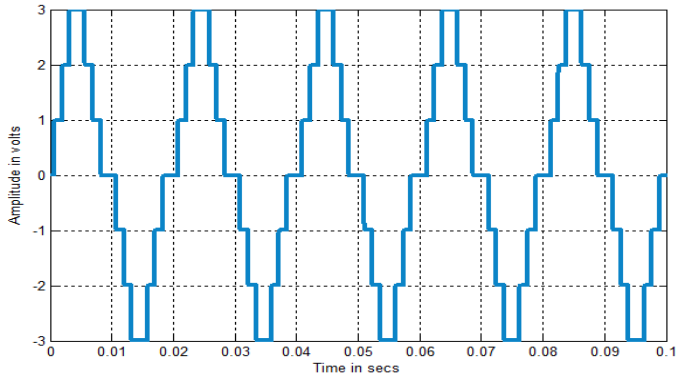

Fig. 16. Output current waveform with R load.

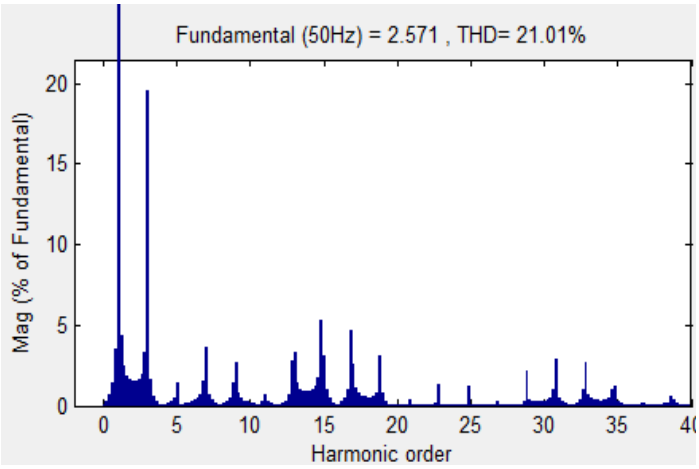

Fig. 17. FFT Analysis for seven level current waveform.

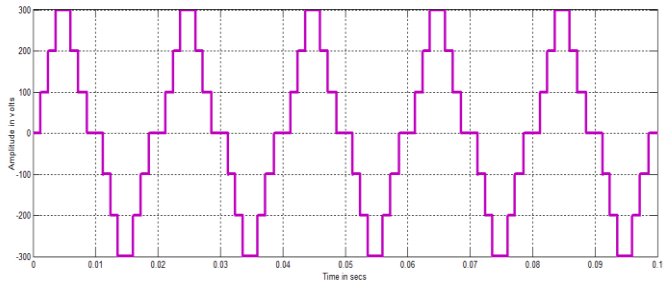

Fig. 18. Output voltage waveform with RL load.

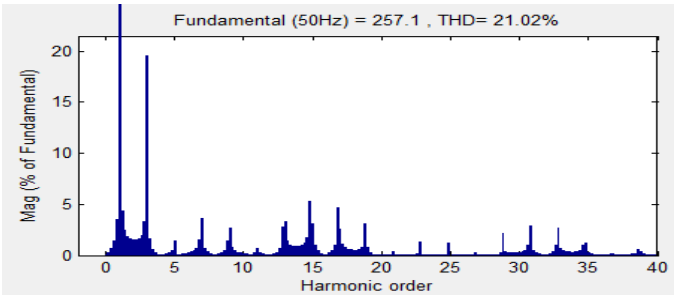

Fig. 19. FFT Analysis for seven level voltage waveform.

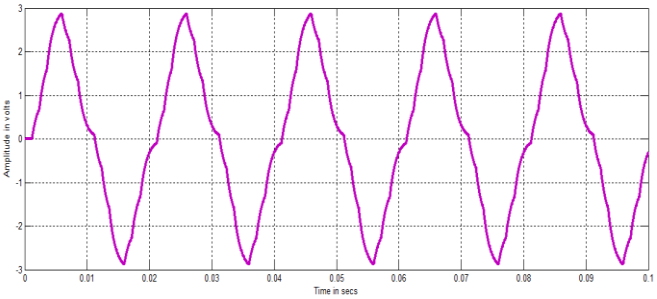

Fig. 20. Current waveform with RL load.

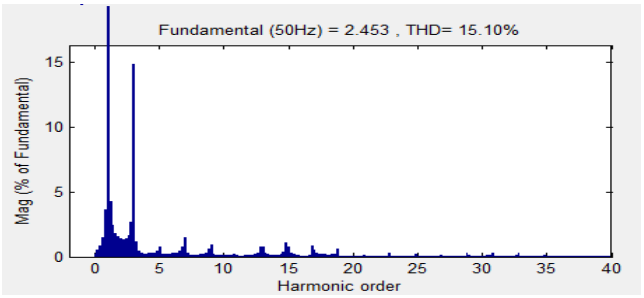

Fig. 21. FFT Analysis for current waveform with RL load.

TABLE II. PEFORMANCE MEASURMENT OF MLI FOR R-LOAD IN TERMS OF VOLTAGE.

Topology	Digital Controller	Embedded Controller
V_{THD}	21.02%	27.22%
V_{RMS}	181.8	177.4
V_{PEAK}	257.1	250.9
Dc component	4.627e-^{008}	0.05

TABLE III. PEFORMANCE MEASURMENT OF MLI FOR RL-LOAD IN TERMS OF VOLTAGE.

Topology	Digital Controller	Embedded Controller
V_{THD}	21.02%	27.22%
V_{RMS}	181.8	177.4
V_{PEAK}	257.1	250.9
Dc component	1.82e-005	0.5006

TABLE IV. PEFORMANCE MEASURMENT OF MLI FOR R-LOAD IN TERMS OF CURRENT.

Topology	Digital Controller	Embedded Controller
I_{THD}	21.01%	27.22%
I_{RMS}	1.818	1.774
I_{PEAK}	2.571	2.509
Dc component	0	0.0005

TABLE V. PERFORMANCE MEASURE OF MLI FOR RL- LOAD IN TERM OF CURRENT.

Topology	Digital Controller	Embedded Controller
I_{THD}	15.10%	17.56%
I_{RMS}	1.753	1.694
I_{PEAK}	2.453	2.395
Dc component	0.004579	0.01578

III. CONCLUSION

In proposed work, the performance of symmetrical cascaded seven level inverter with R-load and RL load by using sinusoidal non pulse width modulation technique has been analyzed by MATLAB /SIMULINK. Performance measurement of mli for R and RL load in terms of of voltage and current are measured. It has lower THD and higher fundamental root mean square value in digital controller compared to embedded controller. Tables II to V shows the various parameters obtained using embedded and digital control. To improve the efficiency of the system , by implementing closed loop control for better performance in future work.

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