Performance Evaluation Of Different Types Of Analog To Digital Converter Architecture

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Abstract

Signal processing is very important in many of the system on-a-chip applications. Analog to digital converters (ADCs) is a mixed signal device that converts analog signals which are real world signals to digital signals for processing the information. A paper present review study of the most popular type of Analog to Digital Converters like flash, pipelined, sigma-delta and successive approximations. The paper represents the fundamental operating principles of these architectures with the sources of error. At last comparison between all analog to digital converters also discussed.

Keywords: Flash ADC, Sigma Delta ADC, Pipelined ADC, Successive Approximation ADC

1. Introduction

In the recent years, the need to design a low voltage, low power, high speed and wide bandwidth analog-to-digital converter has increased tremendously. Analog to digital converters are the basic building blocks that provide an interface between an analog world and the digital domain. As it is the main block in mixed signal applications, it becomes a bottleneck in data processing applications and limits the performance of the overall system. In this paper we present a number of A/D converter architectures. We discuss different architecture of ADCs that include Flash, Pipeline, Sigma-Delta and Successive Approximation ADCs. [1] [2]

2. ADC Architecture

At present, there exists a variety of ADCs with different architectures; accuracies power consumptions, specifications, sampling rates, resolutions and temperature ranges. These ADCs are used in different applications according to the characteristics of ADCs. Since the performance resolution, sampling rate and power consumption of an ADC is basically determined by its architecture, one single ADC type cannot cover all applications. For instance, flash (parallel) ADCs can be used in high speed and low resolution applications. Because of its parallel architecture, all conversions are done in one cycle with many comparators. On the other hand, a successive approximation ADC can be used in low-speed and high-resolution applications since the conversions are done in many cycles with only one comparator. Therefore, it is important to select a proper ADC for each particular application. [2].

3. Types of ADCs

Among the variety of ADC architectures, there are four most popular ADC architectures presently used. These are as follows:

3.1 Flash ADC

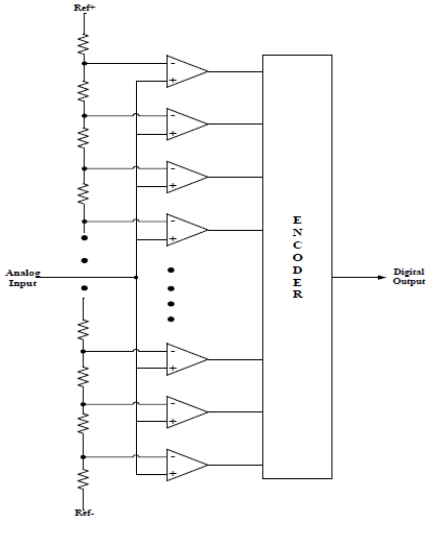

Figure 1. Block Diagram of Flash ADC

The flash ADC is known for its fastest speed compared to other ADC architectures. Therefore, it is used for high-speed and very large bandwidth applications such as high-density disk drives, radar processing, digital oscilloscopes, and so on. The flash ADC is also known as the parallel ADC because of its parallel architecture.

Figure 1 illustrates a typical flash ADC block diagram. As shown in Figure 1, this architecture needs $2^n - 1$ comparators for an n-bit ADC; for example, a set of 63 comparators are used for 6-bit flash ADC.

Each comparator has a reference voltage that is provided by an external reference source. These reference voltages are equally spaced by VLSB from the largest reference voltage to the smallest reference voltage. An analog input is connected to all comparators so that each comparator output is produced in one cycle. The digital output of the set of comparators called the thermometer code is changed into a binary code through the encoder. [2]

3.1.1. Design Considerations and Implications

The flash ADC architecture has high speed conversion due to its parallel structure. However, the flash ADC needs a large number of comparators as the resolution increases. For instance, a 6-bit flash ADC needs 63 comparators, while 10-bit flash ACD need 1023 comparator. The increase in comparator will increase die size and power consumption. [14] Represent technique for reducing circuit complexity for encoder design.

3.1.1. Error Sources in Flash ADC

- **Metastability**

  When a digital output of a comparator is ambiguous i.e. neither a one nor a zero, the output is defined as metastable. Metastability can be reduced by allowing more time for regeneration. Gray-code encoding can be used to improve metastability. Gray-code encoding allows only one bit in the output to change at a time. The comparator outputs are first converted to gray-code encoding and then later decoded to binary. Another problem occurs when a metastable output drives two distinct circuits. It is possible for one circuit to declare the input a "1" while assumes it's a "0". This can create major errors. To avoid this, only one circuit should sense a potentially metastable output.

- **Sparkle Codes**

  Normally, output of the comparator is thermometer code, such as 00111111. Errors may cause an output like 0011011. The spurious "0" in the result sequence is called a sparkle. The sparkles can be due to imperfect input settling or comparator timing mismatch. The magnitude of the error can be quite large and can be avoided by employing an input track-and-hold in front of the ADC along with an encoding technique that suppresses sparkle codes [7].

- **Clock Jitter**

  Jitter in sampling rates decrease Signal to Noise ratio in Analog to Digital Converter. This becomes noticeable for high analog input frequencies. To achieve accurate results, it is critical to provide the ADC with a low-jitter, sampling clock source [8].

3.2 Pipelined ADC

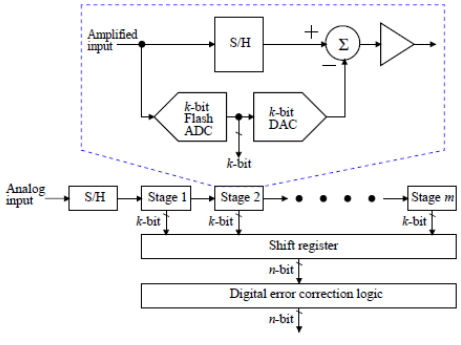

Figure 2. Block Diagram of Pipeline ADC

A pipeline ADC quantizes input voltage in a number of stages. The pipelined ADC architecture is implemented using at least two or more low resolution flash ADCs as shown in Figure 2. Each stage has a S/H circuit to hold the amplified residue from the previous stage. Then, the input is fed to the low resolution flash ADC to generate a segmented binary output. Like the sub-ranging ADC, the segmented output is changed to an analog signal and is subtracted from the input. This residue is amplified in an amplified to send to the next stage. The segmented binary outputs from each stage are time-aligned with a shift register. The final binary output is obtained after passing through digital error correction logic. This conversion process in the pipelined ADC is shown in Figure 2. [2]

3.2.1 Design Considerations and Implications

In Pipelined converters it is possible to achieve higher resolutions than flash converters containing a similar number of comparators. However this comes at the price of increasing the total conversion time from one cycle to *x* cycles. But since each stage samples and holds its input, *x* conversions can be carried out simultaneously. The total throughput can therefore be equal to the throughput of a flash converter, i.e. one conversion per cycle. The difference is that for the pipelined converter, latency equal to *x* cycles is introduced. The power consumption is also increase in Pipelined ADC. Another limitation of the pipelined architecture is that the conversion process

generally requires a clock with a fixed period. Converting rapidly varying non-periodic signals on a traditional pipelined converter can be difficult because the pipeline typically runs at a periodic rate. Different ways to overcome these practical design issues have been discussed in [8, 09, 10].

3.1.1. Error Sources in Pipelined ADC

- **Overlapping**

  The following condition should be met to correct for overlapping errors:

  $$J \times L+K > M$$

  where J is the number of stages, L is the coarse resolution of subsequent stages in the ADC circuit, K is the fine resolution of the final ADC stage, and M is the pipeline ADC's overall resolution. Pipeline ADCs include digital error-correction circuitry which is operates between the stages. Some pipeline quantizers have a calibration unit that compensates for unwanted side effects such as capacitor mismatch or temperature drift in the multiplying DAC.

- **Other Difficulties in Pipeline ADC**

  - Pipeline latency, caused by the number of stages through which the input signal must pass.
  - Sensitivity to process imperfections that cause nonlinearities in gain, offset, and other parameters.
  - Complex reference circuitry and biasing schemes.
  - Critical latch timing, needed for synchronization of all outputs.
  - Greater sensitivity to board layout, compared with other architectures.

3.1 Sigma Delta ADC

The sigma-delta architecture takes a fundamentally different approach from the other architectures. Sigma-delta converters offer high integration, high resolution, and low cost, making them a good ADC choice for different applications such as weighing scales and process control. [2]

Sigma-delta (Σ-Δ) converters have relatively simple structures. Also called oversampling converters.

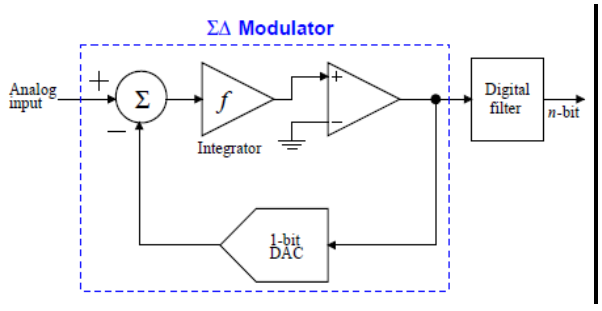

Figure 3. Block diagram of a Sigma Delta ADC

It consists of two main blocks. One is the Sigma-delta modulator that includes an integrator, a comparator, and a single-bit DAC. The other is a digital filter that changes the Sigma-delta output to binary code with filtering. Its block diagram is shown in Figure 3. The output of the 1-bit DAC is subtracted from the input signal, integrated, and then converted to a 1-bit binary output. This single bit again goes to the DAC to be processed. This closed-loop process is performed at a very high oversampled rate [12].

3.3.1 Design Considerations and Implications

- **Noise Shaping**

  One of the most advantageous features of the sigma-delta architecture is the capability of noise shaping, a phenomenon by which much of the low-frequency noise is effectively pushed up to higher frequencies and out of the band of interest. As a result, the sigma-delta architecture has been very popular for designing low-bandwidth high resolution ADCs for precision measurement [12] [13].

- **Oversampling**

  Delta-sigma ADCs use sample rates that are a large multiple, for instance, 128 times the sample rate sufficient for a given signal. For example, to sample a 25 kHz signal, a sample rate greater than the Nyquist rate (that is, > 50 KHz) would be sufficient. However, a delta-sigma ADC using an oversample factor of 128 samples the signal at 6 MHz This approach has several benefits, such as better antialiasing and higher resolution.

  In the frequency domain, sampling a signal effectively modulates the input signal spectrum with carrier frequencies that are multiples of the sample rate F_s (that is, 0, F_s, $2F_s$, 3 F_s, and so on). To recover the signal the sampling rate require must be greater than the Nyquist rate (Fs > 2Fmax). The oversampling property of sigma delta ADC will provide better antialiasing as shown in Figure 4.

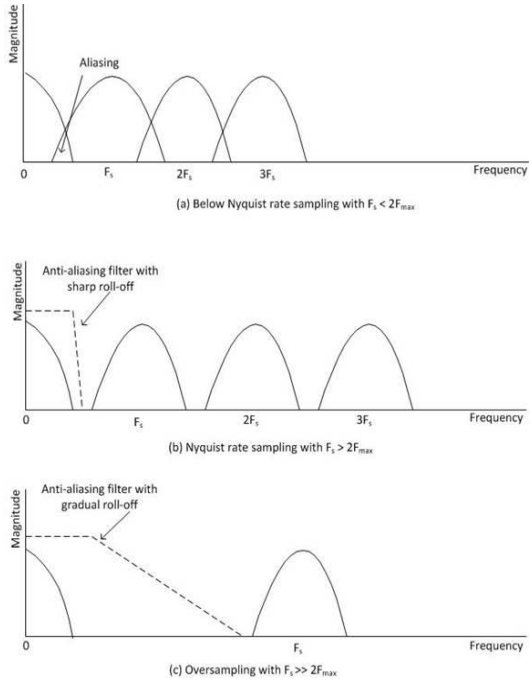

Figure 4. Concept of Oversampling in Sigma Delta ADC

3.3.2 Error Sources in Sigma Delta ADC

A limitation of Sigma delta architecture is its latency, which is substantially greater than all other types of architecture. Because of latency and oversampling sigma-delta converters are not often used in multiplexed signal applications. To avoid the interference between multiplexed signals, a delay at least equal to the decimator's total delay must occur between conversions. These characteristics can be improved in sophisticated sigma-delta ADC designs by using multiple integrator stages and/or multi-bit DACs [12] [13].

3.4 Successive Approximation ADC

Successive Approximation Register ADC is a proper choice for low power applications. SAR ADC employs a successive approximation algorithm to convert analog input to a digital code successively. In other words, one bit is determined in each clock cycle using binary search algorithm.

In this structure track/hold circuit is used to hold the analog input voltage (*VIN)*. The binary search algorithm is implemented by N-bits register. The block diagram is shown in Figure 5.

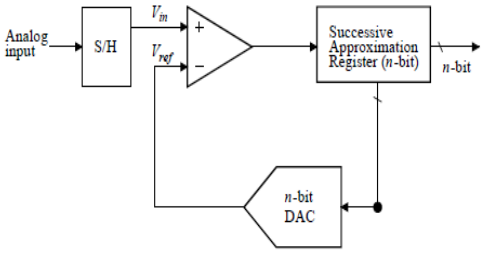

Figure 5. Block diagram of a successive approximation (SAR) ADC

Initially the value of register is set to mid scale i.e. MSB set to "1" and all the other bits are set to "0". The output of DAC (*VDAC)* becomes half the reference voltage V_{REF} /2, where V_{REF} is the reference voltage of ADC. The comparator will compare the input voltage V_{IN} with V_{DAC}. If V_{IN} is greater than V_{DAC}, the comparator output will be set to "1", and the MSB of the N-bit register remains at '1'. If the input voltage V_{IN} is less than V_{DAC} then the comparator output becomes "0". The SAR control logic will change the MSB of the register to '0', set the next bit to "1" and perform comparison again. The operation of 4-bit SAR ADC is shown in figure 6. This process continues till LSB and once this process is completed the N-bit digital word is available in the register. [2]

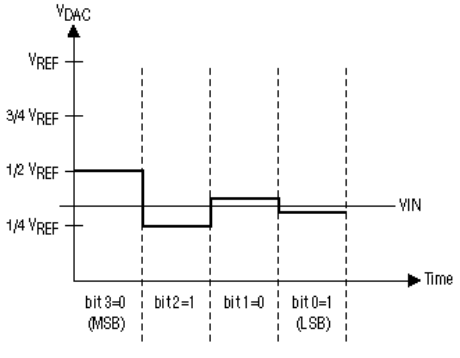

Figure 6. A 4-bit SAR ADC operation

3.4.1 Design Considerations and Implications

A SAR converter using a single comparator it is possible to realize a high resolution ADC. To achieve n-bit resolution n comparison cycles are requires, compared to p cycles for a pipelined converter and 1 cycle for a flash converter. Since a successive-approximations converter uses a fairly simple architecture employing a single SAR, comparator, and DAC, and the conversion is not complete until all weights have been tested, only one conversion is processed during n comparison cycles. For this reason,

SAR converters are more often used in higher-resolution and lower speed applications.. This feature makes the SAR architecture ideal for converting a series of time-independent signals [2]. [15-16] Suggest methods for high-speed low-power structures for SAR ADCs. Aliasing is another parameter of consideration when using a SAR ADC.

The process of sampling a signal leads to aliasing - the frequency-domain reflection of signals about the sampling frequency. In most applications, aliasing is an unwanted effect that requires a low-pass anti-alias filter ahead of the ADC to remove high-frequency noise components, which would be aliased into the passband. However, undersampling can put aliasing to good use, most often in communications applications, to convert a high-frequency signal to a lower frequency. Undersampling is effective as long as the total bandwidth of a signal meets the Nyquist criterion (less than one-half the sampling rate), and the converter has sufficient acquisition and signal sampling performance at the higher frequencies where the signal resides.

3.4.2 Error Sources in Successive Approximation ADC

The different sources of error and drawbacks are:

- The serial nature of SAR architecture limits its speed.
- The settling time of the DAC, this must settle to within the resolution of the overall converter, for example, ½ LSB.
- Comparator noise causes performance degradation of the ADC because of the lack of gain in the ADC architecture. One can put a preamplifier before the comparator to reduce this noise, but at the expense of burning more power in the preamplifier.

4. Comparison of all ADC Architecture

In this section we represent the comparison of all ADC architecture by considers different parameter like conversion methods, encoding method, conversion time, size, resolution and disadvantages. The comparison of different ADC can be understood from following Table-1.

Parameter –1 Select this architecture if you want?	
Flash	Ultra-High Speed when power consumption not primary concern
Pipeline	High speeds, few Msps to 100+ Msps, 8 bits to 16 bits, lower power
Sigma-Delta	High resolution, low to medium speed, no precision external components.
Successive Approximation	Medium to high resolution (8 to 16bit), 5Msps and under, low power, small size.
Parameter –2 Conversion Methods	
Flash	N bits - 2^{N-1} Comparators Complexity increase by a factor of 2 for each bit.
Pipeline	Small parallel structure, each stage work on one to a few bits.
Sigma-Delta	Oversampling ADC, 5-Hz - 60Hz rejection programmable data output.
Successive Approximation	Binary search algorithm, internal circuitry runs higher speed.
Parameter –3 Encoding Methods	
Flash	Thermometer Code Encoding
Pipeline	Digital Correction Logic
Sigma-Delta	Over-Sampling Modulator, Digital Decimation Filter
Successive Approximation	Successive Approximation
Parameter –4 Disadvantages	
Flash	Sparkle codes / metastability, high power consumption, large size, expensive.
Pipeline	Parallelism increases throughput at the expense of power and latency
Sigma-Delta	Higher order (4th order or higher) - multibit ADC and multibit feedback DAC
Successive Approximation	Speed limited to ~5Msps. May require anti-aliasing filter

Parameter –5 Conversion Time	
Flash	Conversion Time does not change with increased resolution
Pipeline	Increases linearly with increased resolution
Sigma-Delta	Tradeoff between data output rate and noise free resolution
Successive Approximation	Increases linearly with increased resolution
Parameter- 6 Size	
Flash	2^N-1 comparators, Die size and power increases exponentially with
Pipeline	Die increases linearly with increase in resolution
Sigma-Delta	Core die size will not materially change with increase in resolution
Successive Approximation	Die increases linearly with increase in resolution
Parameter- 7 Resolution	
Flash	Component matching typically limits resolution to 8 bits
Pipeline	Component matching requirements double with every bit increase in resolution
Sigma-Delta	Component matching requirements double with every bit increase in resolution
Successive Approximation	Component matching requirements double with every bit increase in resolution

Table-1 Comparison of ADCs Architectures. [3]

5. Conclusion

In this paper various types of ADCs have been discussed with their architectures and working principal. The design constraints and sources of errors for all architectures have been highlighted to draw a fair comparison of all architectures. At last comparison between all ADC architecture by considering different parameter is also presented.

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