

# Performance Evaluation of Bridgeless High Power Factor Buck Front End

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**Abstract**—This paper focuses a bridgeless buck converter providing high power factor and thereby improves the efficiency of the buck front end. The proposed buck PFC rectifier also act as a voltage doubler, whose output voltage is twice that of a conventional Buck PFC rectifier. The proposed buck PFC rectifier uses fewer components when compared with previous buck topology. The performance comparison between the conventional buck PFC rectifier and the bridgeless PFC buck rectifiers are performed by simulating them in PSIM.

**Index Terms**—Buck converter, Power factor correction (PFC), Bridgeless

## I. INTRODUCTION

Performance and efficiency of converters is increased by high power factor and low current distortion. By introducing some form of PFC circuits, the requirement of high power factor is usually achieved. Maintaining a high efficiency across the entire line ranges poses a major challenge in ac/dc converters that require power factor correction (PFC). At the earlier stage the boost topology was widely used. The output voltage of the boost converter is greater than input. This fact leads to the use of higher rating semiconductor device at the dc-dc output stages. By implementing buck PFC topology, the drawback of boost PFC rectifier can be overcome.

Conventional Buck PFC rectifier comprises of full bridge rectifier followed by a buck converter. Conventional buck PFC rectifier suffers from high conduction losses and switching losses due to the presence of input rectifier bridge. To reduce this, a bridgeless configuration [2] was introduced which eliminates the use of diode bridge rectifier. Through the minimization of simultaneously conducting components, the proposed PFC rectifier enhances the low line efficiency of buck front end. The proposed rectifier also works as a voltage doubler circuit whose output voltage is twice that of a conventional buck PFC rectifier. The switching losses of primary switches of downstream dc/dc stages are still lower than that of boost PFC, though the output voltage across the

load is doubled. The modified bridgeless PFC rectifier further improves the efficiency and power factor with reduced ripple content. Also this configuration uses one capacitor. Thereby reduce its cost.

Following the introduction, the proposed topology is given in section III, the modified bridgeless buck topology is given in section IV. Section V provides simulation results to validate the analysis. Finally, conclusions are given in section VI.

## II. CONVENTIONAL BUCK PFC RECTIFIER

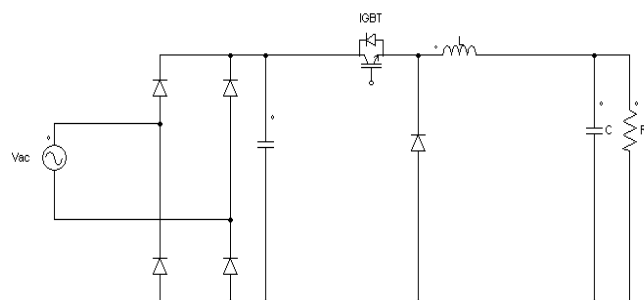


Fig.1. Conventional buck PFC rectifier.

Conventional buck PFC converters consist of a full bridge diode rectifier followed by buck converter. When the switch is closed, the DC source supplies power to the circuit and it gives rise to an output voltage across the resistor. When the switch is opened, the energy stored in the inductor and capacitor discharges through the resistor. By controlling the duty ratio appropriately a desired value of output voltage, lower than the input voltage can be obtained. It has drawback having high conduction losses in the rectifier bridge.

### III. PROPOSED TOPOLOGY

The bridgeless buck PFC rectifier is shown in the figure.2. It uses the configuration of two back-to-back connected buck converters. Each buck converters operate in alternative half cycles of the line voltage.

The Output voltage of the proposed PFC rectifier is the sum of the voltages across the capacitors  $C_1$  and  $C_2$ , which is given by

$$V_{out} = 2DV_{in} \quad (1)$$

Where  $D$  is the duty cycle and  $V_{in}$  is the instantaneous rectified ac input voltage. Since it is buck topology, the relationship which is shown in expression (1) is valid for  $V_{in} > V_{out}/2$ .

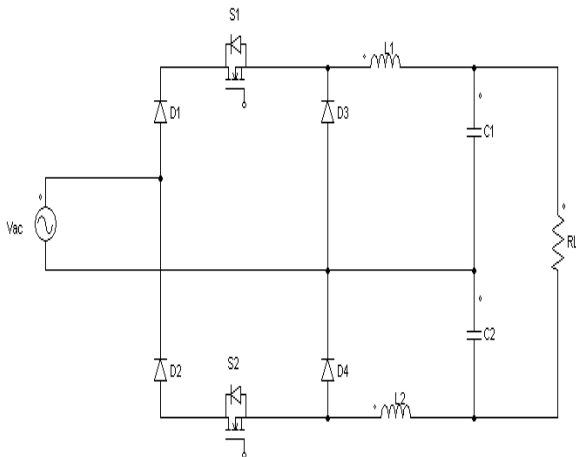


Fig.2. Bridgeless buck PFC rectifier.

In order to make the switch unidirectional, a diode  $D_1$  and  $D_2$  is connected in series with the switch  $S_1$  and  $S_2$  respectively. During the positive half cycles of line voltage  $V_{ac}$ , as illustrated in fig.2, the buck converter consists of a switch  $S_2$ , freewheeling diode  $D_3$ , filter inductor  $L_1$ , and output capacitor  $C_1$  operates. When the switch  $S_1$  turns on, current flows through supply- $D_1$ - $S_1$ - $L_1$ - $C_1$ -supply and energy is stored in  $L_1$ . When the switch is turned off, this current freewheels through freewheeling diode  $D_3$ . Pulse width modulation of switch  $S_1$  regulates the voltage across the capacitor  $C_1$ .

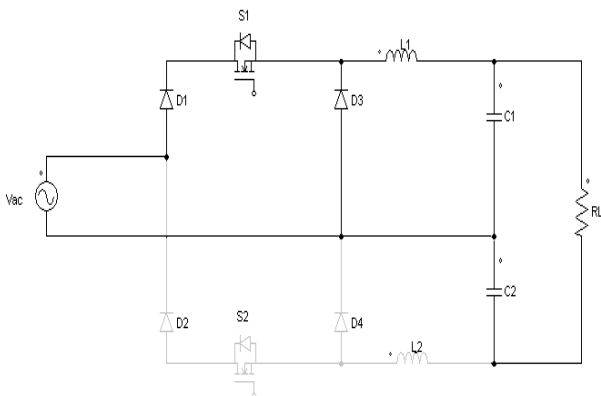


Fig.3. Operation when the line voltage is positive.

During the negative half cycles of line voltage  $V_{ac}$ , as illustrated in fig.3, the buck converter consists of switch  $S_2$ , freewheeling diode  $D_4$ , filter inductor  $L_2$ , and output capacitor  $C_2$  operates. When the switch  $S_2$  turns on, current flows through supply- $D_2$ - $S_2$ - $L_2$ - $C_2$ -supply and energy is stored in  $L_2$ . When the switch is turned off, this current freewheels through freewheeling diode  $D_4$ . Pulse width modulation of switch  $S_2$  regulates the voltage across the capacitor  $C_2$ .

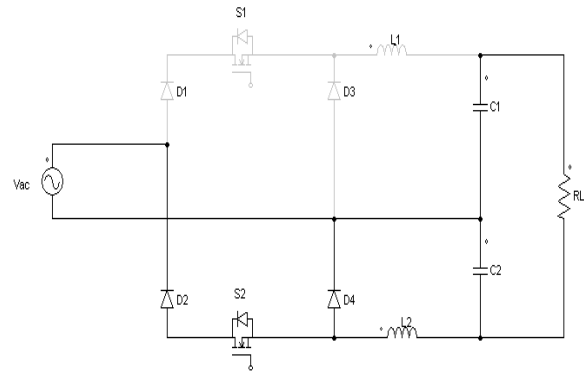


Fig.4. Operation when the line voltage is negative.

From figs.2 and 3, when switch conducts, it can be seen that the input current always flows through only one diode either  $D_1$  or  $D_2$ . By eliminating input bridge diodes, efficiency is increased. When the input voltage falls below the output voltage the rectifier does not operate. Hence the switching loss of the rectifier is considerably low. But during that time, total harmonic distortion (THD) is increased along with a lower power factor.

### IV. NEW BRIDGELESS TOPOLOGY

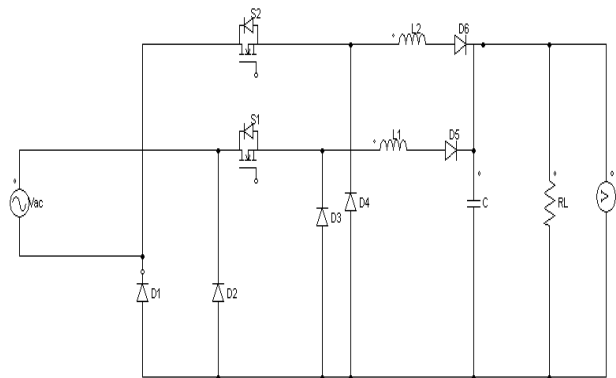


Fig.5. Modified Bridgeless buck PFC rectifier.

In this configuration, diode 5&6 employed to allow unidirectional current flow through the inductors. During the positive half cycle, switch  $S_1$  conducts and during the negative half cycle, switch  $S_2$  conducts. It shows excellent power factor correction. But the main drawback associated with this is that it works well in 0.9 duty ratio. This configuration uses one capacitor.

## V. SIMULATION RESULTS

The performance of the proposed rectifier was designed to operate from ac input supply with switching frequency  $f_s = 10$  kHz. This topology was simulated using PSIM in open loop configuration. Here the duty cycle was adjusted manually to obtain the operation of the converter. Simulation results are illustrated in Fig.6 to Fig.13. The simulation results reveal that a power factor around 0.9 can be achieved using the proposed topology.

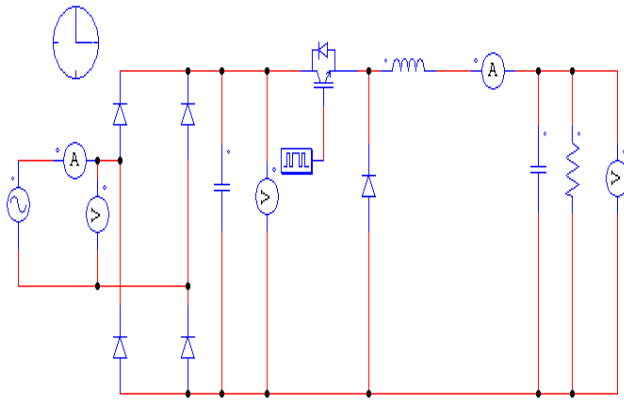


Fig 6. Conventional PFC Circuit layout in PSIM

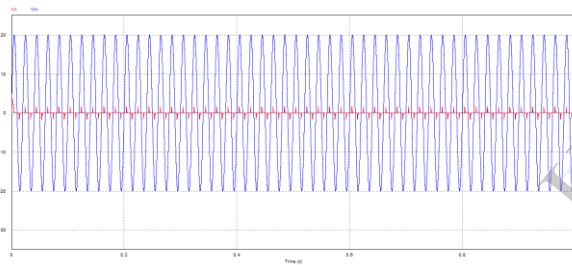


Fig.7.Input Voltage and Input Current waveform of Conventional PFC circuit.

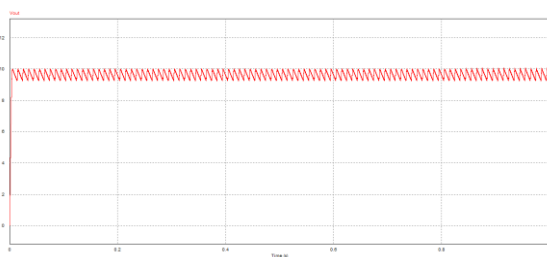


Fig.8. Output Voltage Waveform of Conventional PFC Circuit

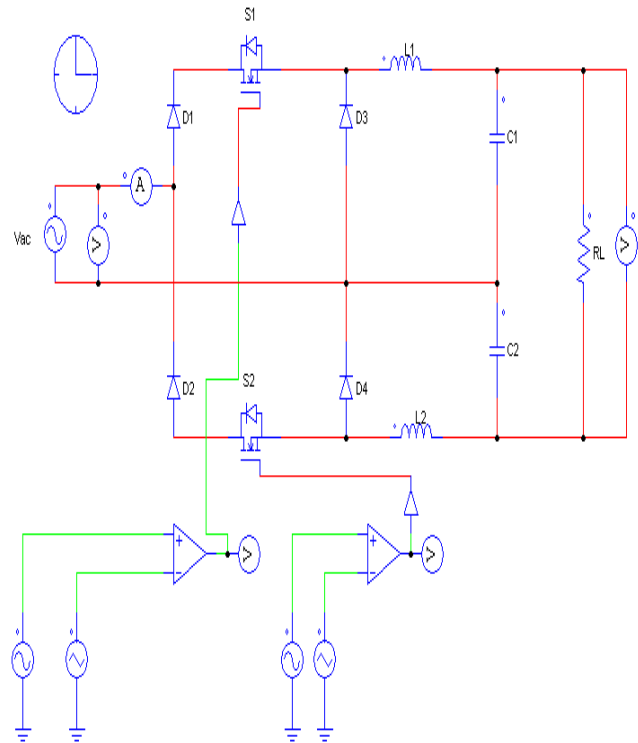


Fig.9. Bridgeless PFC Circuit layout in PSIM

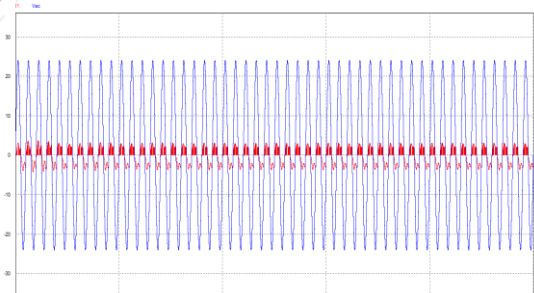


Fig.10.Input Voltage and Input Current waveform of Bridgeless PFC Circuit

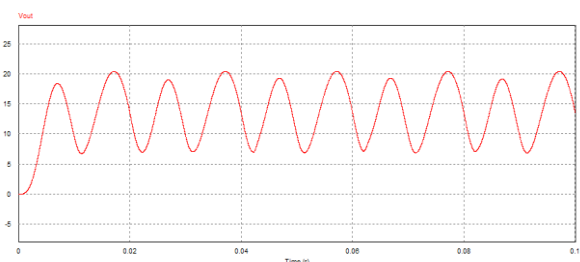


Fig.12. Output Voltage Waveform of Bridgeless PFC Circuit

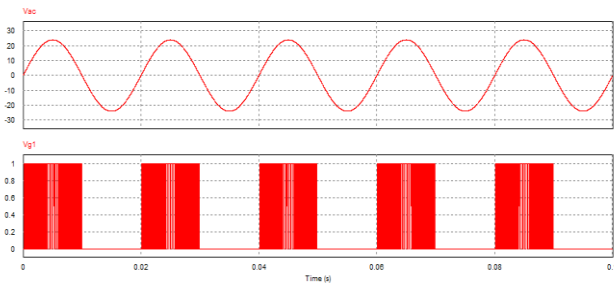


Fig.13.PWM across switch S1 of Bridgeless PFC Rectifier

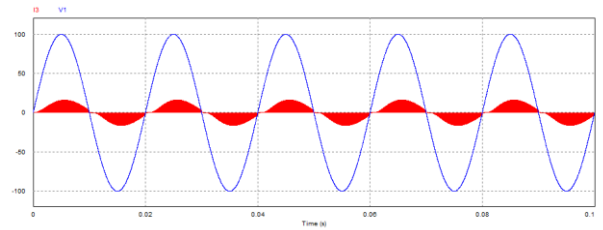


Fig.16.Input Voltage and Input Current waveform of New Bridgeless PFC Circuit

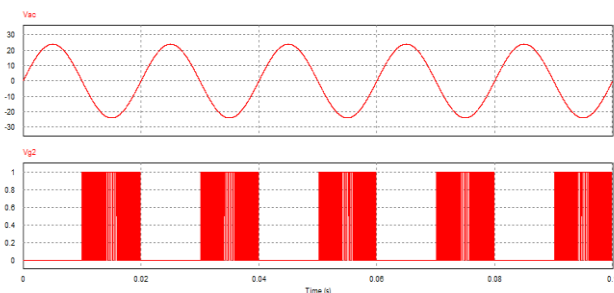


Fig.14.PWM across switch S2 of Bridgeless PFC Circuit

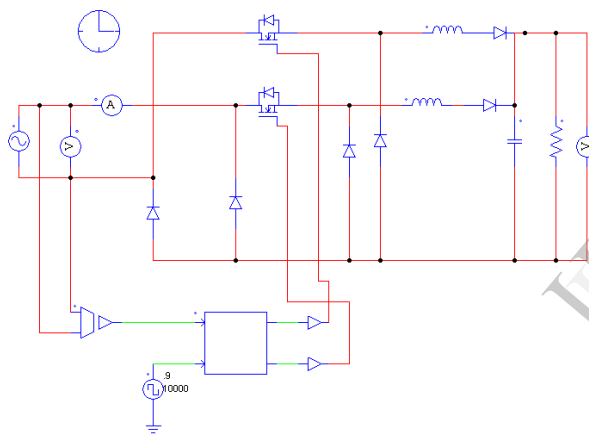


Fig.15. New Bridgeless PFC Circuit layout in PSIM

## VI. CONCLUSION

The bridgeless PFC buck topology is analyzed and simulated using PSIM software. The proposed buck converter doubles the output voltage and it operates with low common mode noise. The new bridgeless topology improves the power factor to around unit power factor. Simulation reveals that the proposed buck converter possesses inherent PFC ability and higher efficiency by minimizing input bridge diode.

## REFERENCES

- 1) L. Huber, L. Gang, and M. M. Jovanović, "Design-Oriented analysis and performance evaluation of buck PFC front-end," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 85–94, Jan. 2010.
- 2) Yungtaek Jang, Milan M Jovanovic "Bridgeless High Power Factor Buck Converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 602–611, Feb. 2011.
- 3) H. Endo, T. Yamashita, and T. Sugiura, "A High-Power-Factor Buck Converter," *IEEE Power Electronics Specialists Conference*, pp. 1071–1076, 1992.