Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 10 Issue 09, September-2021

Performance Evaluation of 6T SRAM cell using 90 nm Technology

Varanasi Koundinya, Jithendra Pulivarthi, Madanu Karun Chand, D.Jayanth Sai Kumar
SRM University, Andhra Pradesh

***Abstract*: Over the last few decades, Static Random-Access Memory or SRAM has become the universally utilized memory technology. It can hold its stored information or data as long as the power is provided and it can be referred to as a type of random-access memory that utilizes latching circuitry in order to store the bits. The SRAM cells are made of MOSFETs. Additionally, the System of Chip advancements requests low-power SRAMs. In this paper performance evaluation of 6T SRAM cell topology has been carried out using Cadence virtuoso tools in a 90 nm technology node. It is performed in terms of the read and write operations, power, noise, temperature, and also the hold operations have been analyzed. Likewise, to assemble a dependable memory or storage, the individual cell (SRAM) should be intended to have a high Static Noise Margin (SNM). The main objective is to comprehend and analyze these activities of the SRAM.**

Keywords* : *SRAM; SNM; Read; Write; Hold; Noise; Power; Temperature

I. INTRODUCTION

In the recent forty years, Moore's law has been expediently improving VLSI arrangement through CMOS advancement scaling. Typically, at 18 months to two years, the quantity of semiconductors ends up being twofold in the integrated circuits. This example of advancement scaling has worked strongly in the semiconductor industry however in the past years, the speed of this scaling has been easing back down. Dynamic Power and static power unquestionably reduce due to the scaling of the supply voltage. Cutting down the supply voltage expands delay to keep up drive current and also the threshold voltage ought to be decreased in a similar way.

SRAM or the static arbitrary access memory is a sort of semiconductor memory that stores each bit by utilizing a bi-stable latching circuitry. It shows information remanence, yet is still customarily unpredictable just as the information put away will in general get lost when the device is not powered.

For the arranging of SRAMs least component size matters however, CMOS advancement scaling increments extreme requirements these include process variations, transistor degradation due to aging. MOSFET-based memory thought was popularized in the seventies. The essential DRAM chip with 2k-bits was marketed in the year 1971 however the DRAM working doesn't coordinate with the working of the processor since the DRAM is more power hungry and its access time is additionally long [1]. The DRAM nature is

dynamic so it needs that the memory should revive intermittently for not to lose the information of memory cells.

The processor required another sort of memory called cache memory to keep consistently used data. SRAMs coordinated with the execution of processors however it has less capacity limit due to restricted area and its expense was additionally high.

Up to 70% of the Systems on Chip area is involved by embedded memories, thusly, it transforms into an issue of importance to improve the reliability of SRAM cells. A wide extent of microelectronics, System on Chip applications, SRAMs continue being an essential section. To meet the necessities SoC applications and processors demand more on-chip memory. Presently, the SRAM is a utilized memory innovation all around. Quick access and low power SRAM are particularly required for System on chip innovations.

II. LITERATURE REVIEW

Deepak Mittal and V.K. Tomar proposed a research paper in which the 6T SRAM cell has been related with the 7T SRAM, 8T SRAM, and 9T SRAM cells with regard to read delay and write delay, read power and write power, Read Static Noise Margin (RSNM) and Write Static Noise Margin (WSNM) and the outcomes have been produced through Cadence Spectre test system [1].

Ms. Isma Rizvi, Nidhi, Dr. Rajesh Mishra, and Dr. M. S. Hashmi introduced a paper in which a subjective understanding of a 6T Static Random-Access Memory (SRAM) cell has been carried out when it has been affected by some noise in the power supply and also in the inverter latch. The research has been carried out in 180nm CMOS innovation with respect to the Write Margin, the Write time, and Static Noise Margin on the induction of noises [2].

C. Premalatha, K. Sarika, P. Mahesh Kannan proposed a paper in which the main focus was to manage the power dispersal which happens regularly in the Static Random-Access Memory or the SRAM cells during the write and the read activity. This issue was solved by applying dual limit voltage for 6T SRAM, 7T SRAM, 8T SRAM, and 9T SRAM cells. Their delay and power dissemination of all these cells are determined and analyzed in this paper. This is carried out utilizing Cadence Virtuoso tools and the Spectre as the test system in the 90nm Generic Process Design Kit [3].

III. CELL DESIGN

The conventional 6T Static Random Access Memory design comprises six transistors, where 2 transistors are of PMOS type and 4 transistors are of NMOS type. The setup is to such an extent that the PMOS type and NMOS type structure make a cross-coupled inverter while two NMOS type transistors are associated with the bit lines. Subsequently, these NMOS type bit lines associated transistors are alluded to as the access semiconductors which are constrained by the word line. Fig. 1 shows the circuit of the 6T SRAM connected in Cadence Virtuoso [5].

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International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 10 Issue 09, September-2021

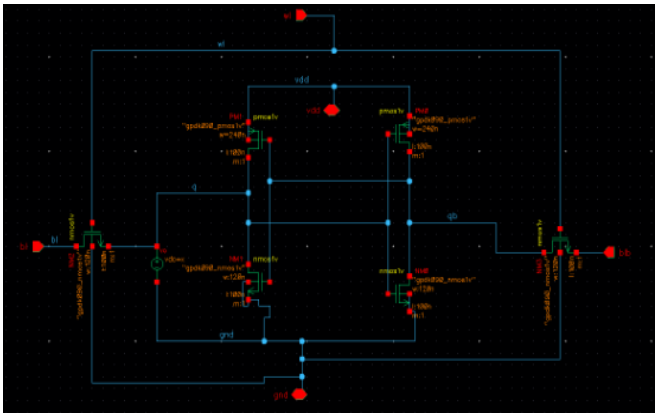

Fig.1 6T SRAM Circuit Design

The two cross-coupled inverters forming a latch with two access transistors for getting to the information or the data taken care of in the memory cell. The plan of the SRAM cell ought to be done so that it allows a good read activity simultaneously with a good write margin. The cell is composed by driving the desired value and its complement onto the bit lines, BL and BL_ Bar at that point raising the word-line WL.

The cell is read by pre-charging the lines high, at that point permitting them to float. When the word-line is raised one-bit line is pulled down while the other stays high. For appropriate read activity, the access transistor-NMOS and also the pull-down NMOS are estimated to such an extent that the value of voltage for the other inverter and quick read activity is performed. Likewise, to guarantee appropriate write activity it requires access transistor and pull up PMOS are estimated.

When switching operation happens in the circuit for a little period, the pull up and pull-down transistor turns out to be short which makes the static impact in the circuit, for example, the supply voltage Vcc and ground terminal turns out to be short which prompts static power loss so the overall power loss increases in the read operation.

IV. PROPOSED WORK

In read activity information is required from the memory cell. In this manner, to understand information, both the bit-line BL and the bit-line bar BL_Bar are at first pre-charged to state 1, when the word line is low that is WL will be zero. Once it is pre-charged the word line will be equal to one and hence the access transistors are turned ON subsequently associating with the bit-lines. For the write activity, if the BL is high, the BL_Bar will be low, for example, both the BL and BL_ Bar line will be complementing to one another.
Two CMOS inverters are connected and they act as memory. It is similar to that of the NOT gate operation. The outputs are taken as Q and Q_Bar. We use access transistor to access the BL and BL_Bar in order to perform read and write operations.

If WL=1;
Both access transistors are ON and the read and write are possible.

If WL=0;
The memory will be in hold state.

BL and BL_Bar will act as input lines when we have to write into the memory. If we have to read from the memory they will act as output lines.

For write consider Q=0 and Q_Bar=1
WL=1
BL and BL_Bar = input and BL_Bar=GND
Voltage decreases if V<Vth of NM3
NM3=OFF and PM2=ON
Implies Q=1

For read consider Q=0 and Q_Bar=1
WL=1
BL and BL_Bar = output
if V>Vth of NM0
NM0=ON
Q_Bar=0
Q and Q_Bar both are zero. So, we have to make sure that voltage does not exceed Vth of NM0.

Fig. 2 and Fig. 3 shows Read 0 and Read 1 Circuit Design respectively.

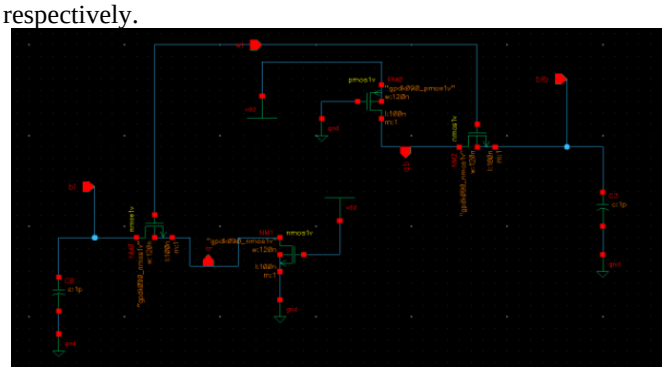

Fig. 2 6T Read 0 Circuit Design

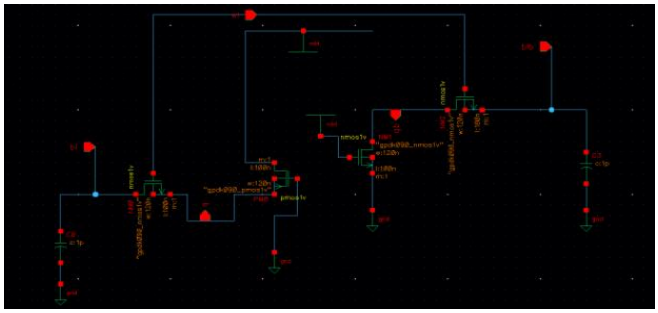

Fig. 3 6T Read 1 Circuit Design

Fig.4 represents the Write Operation circuitry as shown below.

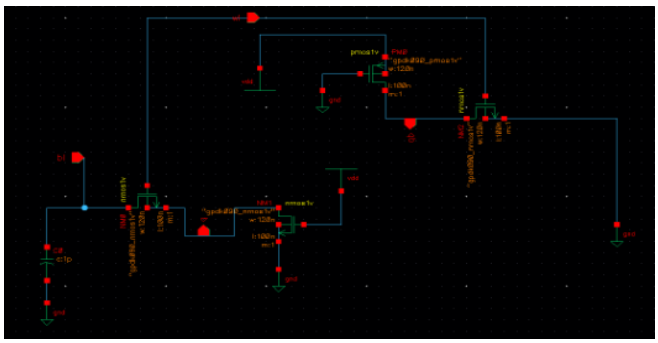

Fig.4 Write Operation Circuit Design

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International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 10 Issue 09, September-2021

The hold activity is a state when the SRAM cell information is held in the latch and the data paths that is the bit-line BL and bit-line bar BL_Bar information are kept at the GND when the access semiconductors are separated because word line isn't embedded. Subsequently, the PMOS transistors will proceed to re-implement each other as long as they are associated with the power. The circuit for hold operation is shown in Fig. 5.

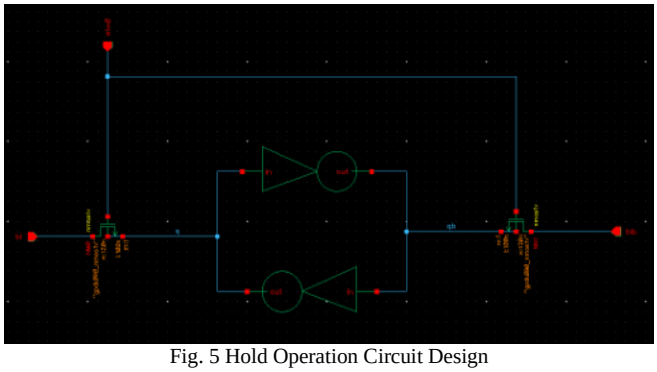

Fig. 5 Hold Operation Circuit Design

The 6T SRAM variation with regard to the temperature and power have also been simulated using the Cadence Virtuoso tools in 90nm technology. The DC response of temperature is analyzed in Cadence.

The Static Noise Margin commonly known as SNM is one of the main metrics considered while designing memory. This noise margin influences both the write and the read margins [4]. The steadiness of Static Random Access Memory cell is chiefly characterized by the utilization of SNM which is the highest value DC noise voltage that can be endured without any change in the internal storage condition of the cell. Ordinarily, to build the SNM, the voltages of the PMOS and NMOS should be expanded. But, the increment in the voltage of PMOS and NMOS is restricted. Fig. 6 represents the SNM Circuit.

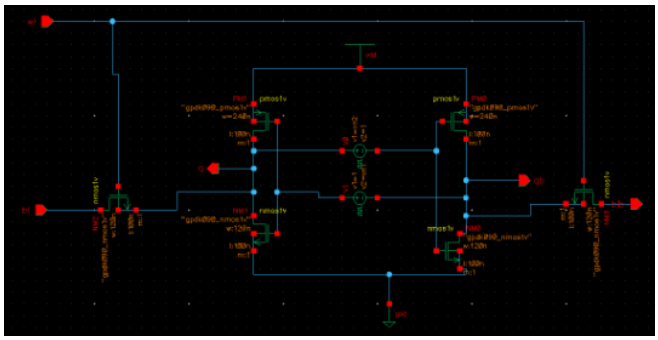

Fig. 6 SNM Circuit Design

V. RESULTS

The operations mentioned above have been performed in through the Cadence Virtuoso tools platform and the response have been obtained.

Fig. 7 and Fig. 8 shows the transient response for the read 1 and read 0 operations performed.

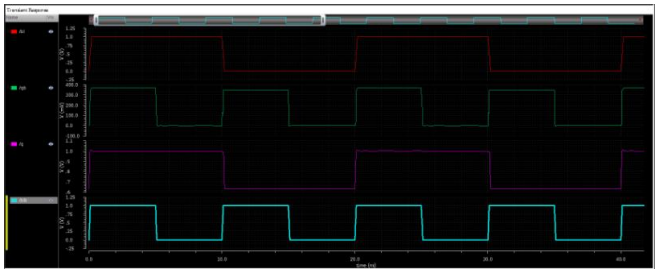

Fig. 7 Read 1 Transient Response

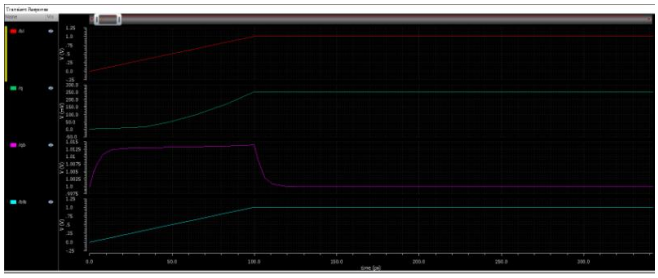

Fig.8 Read 0 Transient Response

Fig. 9 depicts the transient response for the write opearation performed.

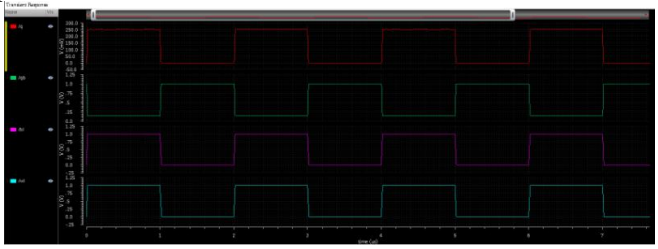

Fig. 9 Write Transient Response

Fig. 10 shows the tranisent response for the hold operation performed

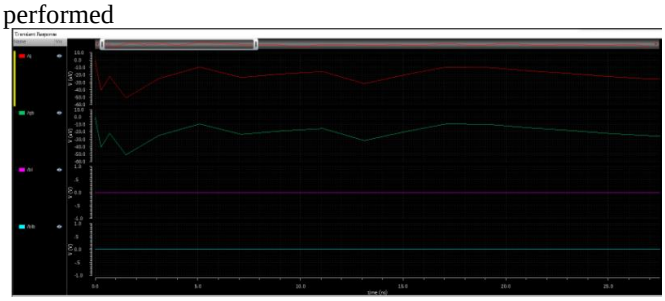

Fig. 10 Hold Transient Response

Fig. 11 depicts the DC response of temperature

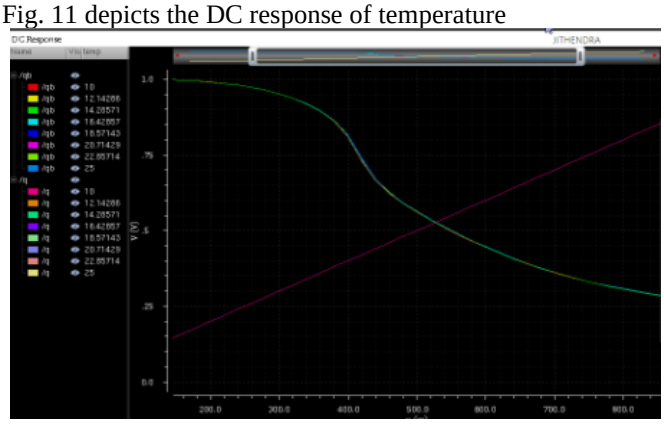

Fig.11 Temp DC response

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International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 10 Issue 09, September-2021

Fig. 12 represents the DC response of power

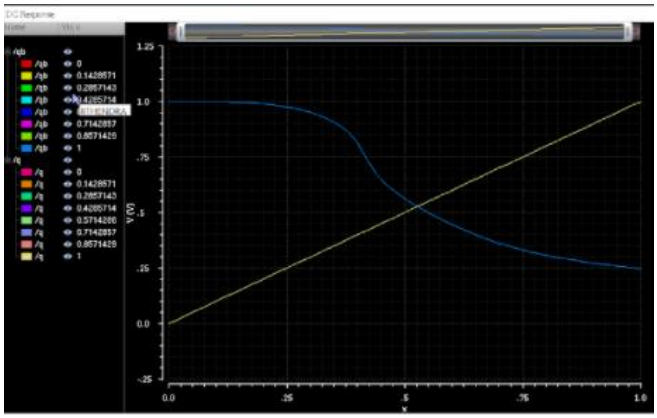

Fig. 12 Power DC response

Fig.13 shows the SNM Noise Response

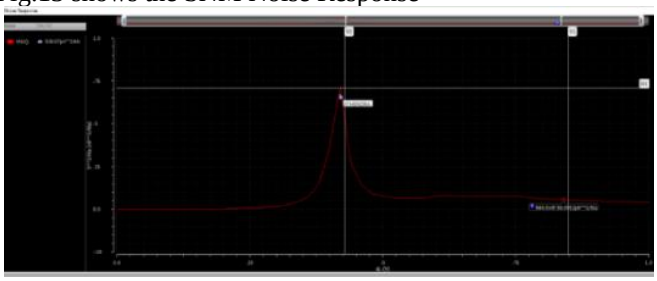

Fig.13 SNM Noise Response

Fig. 14 shows the Noise Read Response

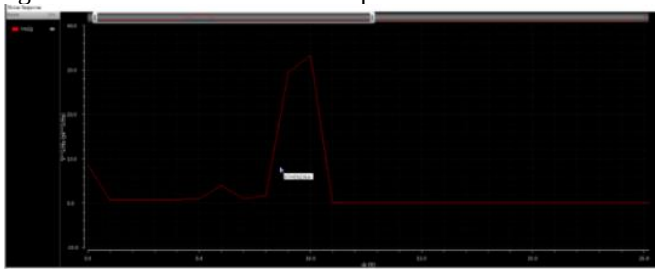

Fig. 14 Noise Read Response

Fig.15 shows the Noise Write Response

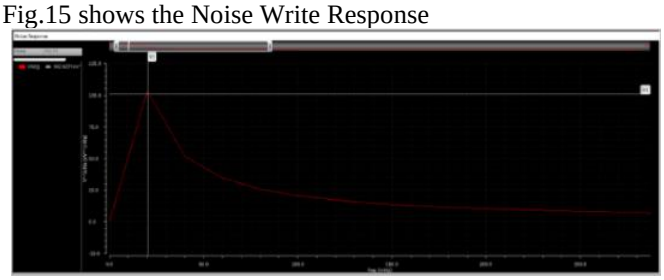

Fig. 15 Noise Write Response

Fig.16 represents the values of power consumed when input voltage is supplied

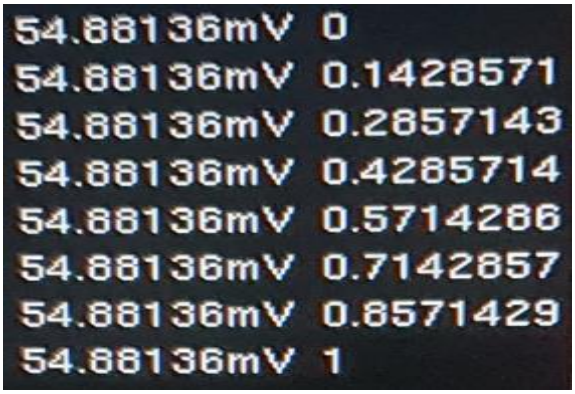

Fig. 16 Power values

VI. CONCLUSION

The analysis of 6T Static Random-Access Memory is done in this paper. The read, write, hold, operations were performed for the 6T SRAM. Also, DC response for temperature and power is simulated. Another major factor that is the Static Noise Margin has been done and the noise responses obtained are shown for both read and write operations. All the simulations were carried out utilizing Cadence Virtuoso Tools in 90nm CMOS technology. In the future, we can upgrade the Static Random Access Memory cell and make it dependable and robust to the noise present in the environment.

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International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 10 Issue 09, September-2021

AUTHORS PROFILE

Varanasi Koundinya *Department of Electronics and Communication Engineering* SRM University Andhra Pradesh, India

Jithendra Pulivarwthi *Department of Electronics and Communication Engineering* SRM University Andhra Pradesh, India

Madanu Karun chand *Department of Electronics and Communication Engineering* SRM University AndhraPradesh,India

D.Jayanth sai kumar *Department of Electronics and Communication Engineering* SRM University Andhra Pradesh, India

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