Performance Enhancement of Complex Multiplier using Vedic Sutras

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***Abstract*— Vedic mathematics is the ancient system of mathematics based on simple rules and principles. It reduces the complexity in current system of mathematics to very simple one. It works similar to how a human mind works. Vedic mathematics has a lot of algorithms to compute complex mathematical operations. Now a day, application of Vedic Mathematics got increases in the field of applied electronics. Among the arithmetic operations multiplication is an important arithmetic which is used frequently. It's application involves convolution, digital signal processing, Fast Fourier Transform (FFT). All the signal and data processing operations involve multiplication. Speed is one of the important constraints in the multiplication operation. Increase in speed can be achieved by reducing the number of steps in the computation process. The speed of multiplier determines the efficiency of such a system. Multipliers based on Vedic Multiplication reduce the delay, memory usage and power consumption. This paper deals with the application of logical algorithms mentioned in Vedas to modify the functioning of conventional multiplier. The simulation of two relevant sutras is done using ModelSim software and its performance analysis using Xlinix software.**

***Index Terms*— Multiplier, Vedic Sutras, Nikhilam sutra, Urdhava tiryagbhyam sutra**

I. INTRODUCTION

It may be defined the paper title ''Performance Enhancement of Complex Multiplier using Vedic Sutras", as an effort to analyze how a multiplier can be improved in terms of operational speed, memory usage and power consumption by accompanying the logical algorithms of different Vedic sutras and to quantify it by comparative performance analysis with the conventional multiplier.

Vedic mathematics is a part Adharva Veda, the last of four Vedas .The word "Vedic" is derived from the word "Veda". Which means the fountain-head and illimitable store-house of all knowledge. Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884- 1960) introduced Vedic Mathematics. Swamiji developed sixteen sutras (formulae) and thirteen Upa-sutras (sub formulae) after extensive research. Vedic mathematics is not a mere mathematical wonder, it is pure logical. These Sutras along with their brief meanings are enlisted below.

1) Ekadhikina Purvena – By one more than the previous One
2) Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10
3) Urdhava-tiryagbhyam – Vertically and crosswise
4) Paraavartya Yojayet – Transpose and adjust
5) Shunyam Saamyasamuccaye – When the sum is same that sum is zero
6) (Anurupye) Shunyamanyat – If one is in ratio, the other is zero
7) Sankalana-vyavakalanabhyam – By addition and by subtraction
8) Puranapuranabyham – By the completion or non-completion
9) Chalana-Kalanabyham – Differences and Similarities
10) Yaavadunam – Whatever the extent of its deficiency
11) Vyashtisamanstih – Part and Whole
12) Shesanyankena Charamena – The remainders by last digit
13) Sopaantyadvayamantyam – The ultimate and twice penultimate
14) Ekanyunena Purvena – By one less than the Previous one
15) Gunitasamuchyah – The product of sums is equal to the sum of products
16) Gunakasamuchyah – The factors of sum is equal to the sum of factors.

II. SUTRAS OF INTEREST

Among the sixteen sutras of Vedic mathematics three are dealing with multiplication. One is exclusively to find squares. The rest two are discussed here. Urdhava tiryagbhyam sutra is the only one yet tried by any research work for the similar studies. The adaption of both together is supposed to be a challenge in this work. The two sutras of interest are briefed below.

A. Nikhilam Navatashcaramam Dashatah Sutra

This sutra by name means, "All from 9 and the last from 10". The Nikhilam Sutra can be used to multiply any number, but is very effective when applied to numbers nearer to the powers of 10. The procedure of multiplication using the Nikhilam involves minimum number of steps, space, time saving and only mental calculation. The nearest 10^n of both multiplicands is taken as the base of operation. The numbers taken can be either less or more than the base considered. The

difference between the number and the base is termed as deviation. Deviation may be positive or negative. Let N_1 and N_2 be two numbers near to a given base in powers of 10, and D_1 and D_2 are their respective deviations from the base. Then $N_1 \times N_2$ can be represented as

Numbers		Deviations = (Number – Base)
N_1 N_2		D_1 D_2
$(N_1 + D_2)$ or $(N_2 + D_1)$	$(D_1 \times D_2)$	

Fig .1: Formulation of Nikhilam sutra.

If R. H. S. contains less number of digits than the number of zeros in the base, the remaining digits are filled up by giving zero (or zeroes) on the left side of the R. H. S. If the number of digits is more than the number of zeroes in the base, the excess digit (or digits) is to be added to L. H. S. of the answer.

E.g. 1: 986 X 989 = 975154, here nearest power of 10 is 1000, which is taken as base.

Numbers		Deviations = (Number – Base)
986 989		- 014 - 011
(986+ -011) or (989+ -014)	(14 x 11)	
975	154	
975154		

E.g. 2: 994 X 988 = 982072. Base is 1000

Numbers		Deviations = (Number – Base)
994 988		-006 -012
(994+ -012) or (988+ -006)	(6 x 12)	
982	072	
982072		

1) ARCHITECTURE OF NIKHILAM MULTIPLIER

The mathematical expression for the "Nikhilam Navatascaramam Dasatah" algorithm is given below. The Nikhilam algorithm is divided into three fundamental parts namely, (i) Base Selection Unit (ii) Exponent Determinant (iii) Complex Multiplier Unit.

Consider two n bit numbers X and Y. K_1 and K_2 are the exponent of X and Y respectively. X and Y can be represented as:

$$X = 2^{K_1} \pm Z_1 \quad (1)$$
$$Y = 2^{K_2} \pm Z_2 \quad (2)$$

$$Y * 2^{K_1 - K_2} = (2^{K_2} \pm Z_2)(2^{K_1 - K_2}) = (2^{K_2} * 2^{K_1 - K_2}) \pm (Z_2 * 2^{K_1 - K_2}) = 2^{K_1} \pm Z_2 * 2^{K_1 - K_2} \quad (3)$$

$$X*Y * 2^{K_1 - K_2} = X * (2^{K_1} \pm Z_2 * 2^{K_1 - K_2}) \quad (4)$$

After substitutions and solving the equation becomes,

$$P = XY = X*Y*2^{K_1 - K_2} / 2^{K_1 - K_2} = 2^{K_2}(X \pm Z_2 * 2^{K_1 - K_2}) \pm Z_1 * Z_2 \quad (5)$$

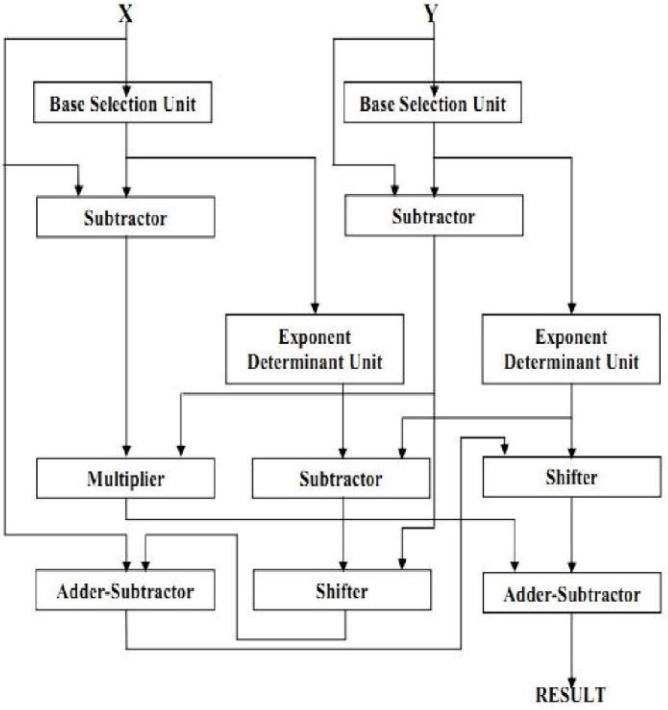

Fig. 1: Architecture of Nikhilam Multiplier

B. Urdhava Tiryagbhyam Sutra

Urdhava – tiryagbhyam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. It literally means "Vertically and crosswise". This sutra is useful for the multiplication of two decimal numbers also. Logic is explained via two examples.

E.g. 1: (48 X 47) = 2256

```
  48
  47
------
1606
  65
------
2256
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Step (i): (8 X 7) = 56; 5, the carried over digit is placed below the second digit.
Step (ii):(4 X 7) + (8 X 4) = 28 + 32 = 60; 6, the carried over digit is placed below the third digit.
Step (iii): (4 X 4) = 16; Write it completely.
Step (iv): Respective digits are added.

The above described procedure can be adapted to any number of digits.

Since there is a parallel generation of the partial products and their sums, the processor becomes independent of the clock frequency. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The advantage here is that parallelism reduces the need of processors.

1) URDHAVA 2 X 2 MULTIPLIER

Let us consider two data inputs, each of length 2 bits; say A_1, A_0 and B_1, B_0. The output can be of four bit length, say P_3, P_2, P_1, and P_0.

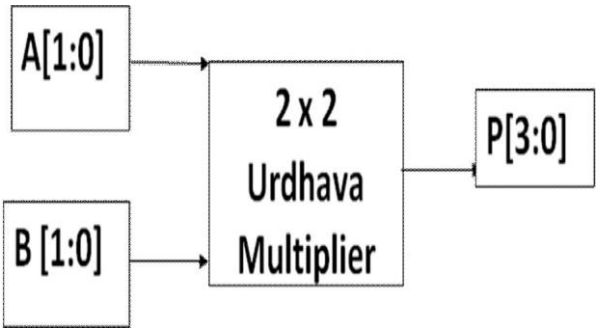

Fig. 3. Block diagram of Urdhava Sutra Multiplier

In Vedic multiplier, P_0 is obtained by vertical multiplication of data bits A_0 and B_0, P_1 is obtained by addition of crosswise bit product i.e. A_1B_0 and A_0B_1 and next P_2 is obtained by adding the product vertical data bits A_1 and B_1 with the carry generated from the previous addition during P_1. P_3 is the nothing but carry generated in calculation of P_2. This part is the operation of 2x2 multiplier block.

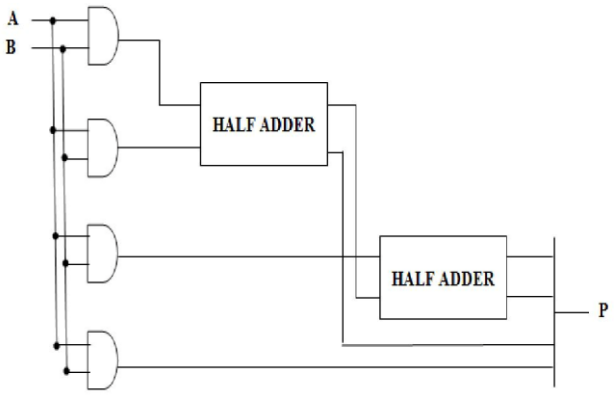

Fig. 4: Circuit diagram for 2bit Urdhava Sutra Multiplier

2) URDHAVA 4 X 4 MULTIPLIER

As number of bits increases in input, a small modification is required. Divide the total number of bits of each input into two equal parts .Now let us design 4x4 multiplications with inputs as $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$. The result obtained by multiplication the two inputs are represented as $P_7P_6P_5P_4P_3P_2P_1P_0$. Let us divide the inputs A and B into two equal parts as mentioned above, say A_3A_2 and A_1A_0 for input A and B_3B_2 and B_1B_0 for input B. Take two bits at a time by using the basic principle of Vedic multiplication and using 2 bit Vedic multiplier block. The final result is obtained by adding the outputs of 2×2 bit multipliers in a specific way. Hence three ripple carry adders are required at final stage; is given in Figure 5. By observing the algorithm, it is clear that 4 x 4 bit multipliers are designed from 2 X 2 bit blocks. The design includes 4 2 x 2 multipliers and 3 Ripple Carry Adders.

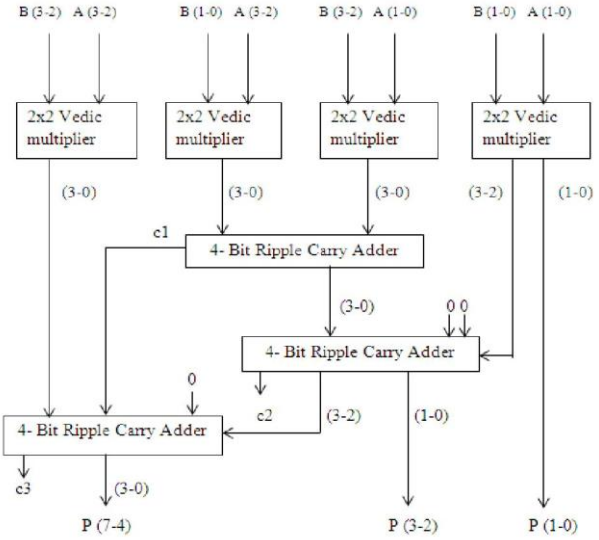

Fig. 5. 4X 4 Urdhava multiplier

III. IMPLEMENTATION

Since the Nikhilam sutra is simple only when the numbers to be multiplied as nearer to the bases, that faster formulation is supposed to limit for such numbers. And all other multiplication may be done using Urdhava sutra formulation.

It is not found the ModelSim software being used in this kind of projects. The ModelSim software is licensed to support designs written in VHDL. Xilinx ISE (Integrated Software Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize their design. Hence the simulation using ModelSim and performance analysis using Xlinix, a much powerful tool, are proposed.

IV. SCOPE OF THE WORK

Various researchers are ongoing around the world to adapt the Vedic Mathematics into modern computing technology. Yet the researchers are based only on one sutra. In this paper collaboration of two sutras i.e., Urdhava Tiryagbhyam Sutra

and Nikhilam Navatashcaramam Dashatah Sutra are applied simultaneously for the performance enhancement of the multiplier. The performance analysis is done in xilinix software. The concept is that, the initial conditions are set at the start (say) at around 20% from the nearest base as the Nikhilam limit. If the inputs lie inside Urdhva limit, Urdhava based multiplier will perform the multiplication and if the inputs lie inside Nikhilam limit, Nikhilam based multiplier will perform the multiplication. This is extended for all higher order cases. This proposed architecture is aimed at achieving faster results. Also, when one multiplier is 'ON', the other is 'OFF'.

V. RESULT AND DISCUSSION

The entire algorithm in this paper was simulated and their functionality was examined by ModelSim software. The performance Analysis was done using Xilinix Software.

A. CONVENTIONAL MULTIPLIER UNIT

Figure 6 shows the waveform of a conventional multiplier system. In this multiplier, two inputs are stored in the registers x & y. Both x& y are 8-bit registers. The register N represents a 8-bit register which has the same value stored in register y. The clock pulse is also given, so for every clock pulse, it will produces the multiplied values of two input numbers. The multiplied value is stored in the output register multi. The ModelSim simulated result is shown below.

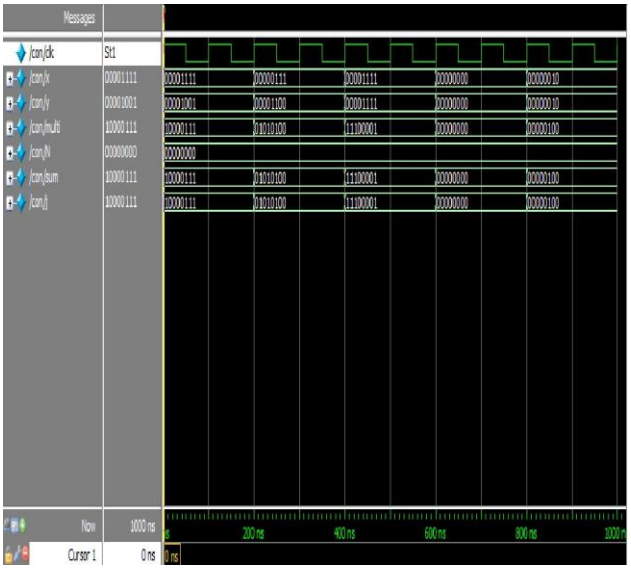

Fig. 6. Conventional Multiplier Unit

B. NIKHILAM NAVATASHCARAMAM DASHATAH SUTRA MULTIPLIER

Figure 7 shows output of the proposed multiplier unit. The two 8-bit input numbers which has to be multiplied is stored in the registers A1& A2. The clock pulse is also given as an input. Here multiplying two 8-bit numbers, so the output will be a 16-bit binary number. The output is stored in a 16-bit register indicated by the name result. The intermediate registers sub1, sub2 etc includes the various operation associated in order to reach the final output value.

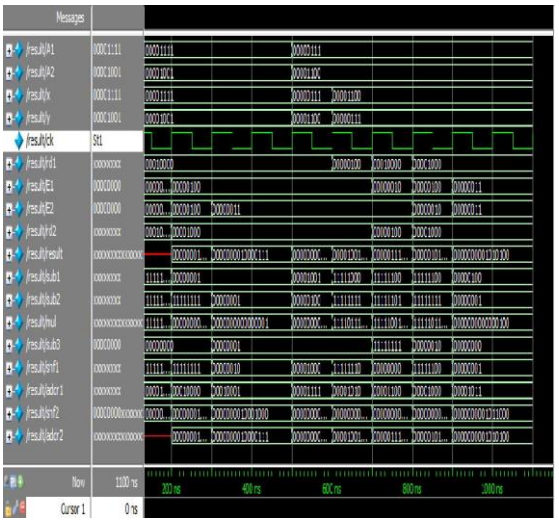

Fig. 7. Nikhilam Navatashcaramam Dashatah Sutra Multiplier

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