Performance Analysis of Vertical Slit Field Effect Transistor

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Abstract

A novel twin gate junction less VeSFET device with ideal subthreshold slope, minimum I_{off} has been described in this paper. The device is manufactured over the SOI infrastructure. The VeSFET device with tied gate and independent gate is studied and compared for low I_{off} current. Tied gate structure at different N poly and Nsub are compared for reduction in off current. It is reported that Si_3N_4 as an insulator for the TGC configuration results in 100 times reduction in off current as compared to SiO_2..

1. Introduction

Energy efficiency and optimisation is of main concern for modern applications, especially in power battery devices. It is observed that portable devices requires a long term charge batteries and low power consumption. Voltage scaling, i.e. reducing voltage supply level, allows a reduction of dynamic power as they are having quadratic relation at the expense of decreased performance. To reduce the effect of speed loss in submicron era, transistor's threshold voltage is typically scaled as well. But this leads to the enhancement of leakage power. Studies have shown that minimum energy operating point exists, usually in sub-threshold region [1-3]. Vertical Slit Field Effect Transistor (VeSFET) [5] is a novel twin-gate (having two symmetrical, independent gates) device with excellent I_{on}/I_{off}. The device proposed by W. Maly, *et al* [5] has shown ideal subthreshold slope and reduced I_{off}. These devices can also offer more than just improved gate control, such as, increased function per transistor, provided, the gates are controlled separately [6].

Adding more functionality to a single device could be a way, other than scaling, to increase the functional density for a given silicon area. For example, realizing AND/OR functionality in a single transistor allows implementation.

the VESFET is that the gates can be controlled independently, and therefore the threshold voltage of the VESFET can be automatically adjusted by varying gate voltage of either of the two independent gates. This can be used to implement a logic "NOT", "OR" or "AND" functionality within one transistor only. IGC (independent gate control) and TGC (Tied gate control) two configurations can be realized in VeSFET device that shows number of applications in digital circuits and analog circuits as well. In addition to multi-functions, VeSFET offers many advantages, including no lithography on topography, and optical proximity correction (OPC) free device structure etc [4].

The paper is organized in the following manner. Device description and working operation of the device is described in section 2 of the paper. Section 3 demonstrates the input output characteristics of the device, comparison of I_{off} current for IGC and TGC VeSFET and conventional MOSFET is also shown. The behavior of device with variation in substrate doping and gate doping concentration for TGC VeSFET and the comparison of reduced I_{off} with Si_3N_4 as insulator is shown in section 3 only and section 4 concludes the paper.

2. Device description and operating principle

A Junction-less VeSFET comprises of source, drain and channel region with same dopants, shown schematically in Fig.1a. It is a gated resistor in which the current is controlled by depletion regions created by the two gates on either side of the channel [1, 6].

In the OFF state, the depletion region, created due to the work function difference between the channel and the gate material, packs up the channel completely know as fully depleted channel, which leads to low OFF current. In the ON state, when a voltage is applied on the gate to counter the work function difference, the depletion region recedes and a path is created for the current to flow between source and drain. VeSFET exhibits majority carrier flow

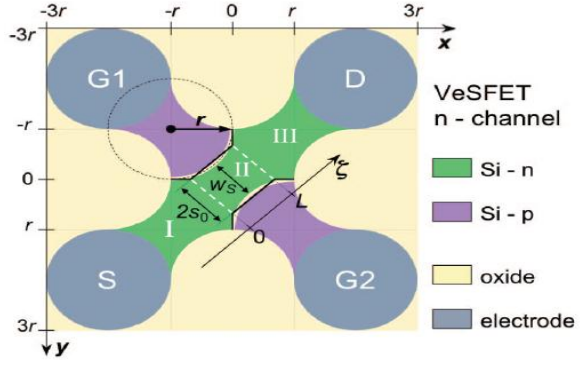


Fig.1a Top view of n channel symmetrical twin gate VeSFET with radius=50nm and uniform channel doping 5×10^{17} cm^{-3}

The VeSFET device is hybrid of both JFET and MOSFET device but unlike the above mentioned two devices it is junction less and an insulator is present with majority carrier flow that contributes to the total current in the junction less devices.

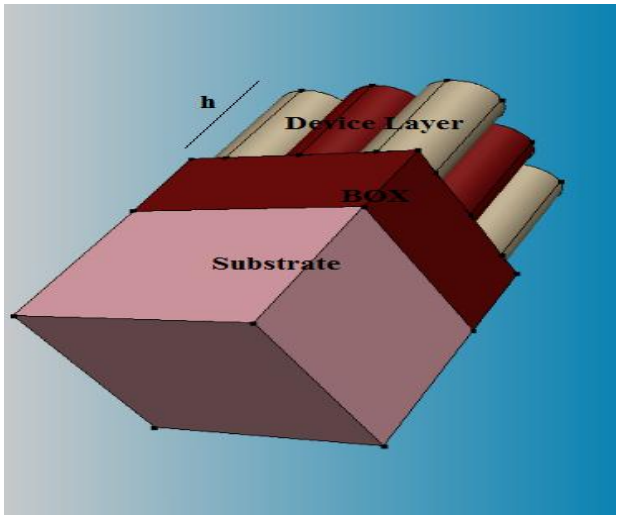


Fig.1b 3D structure of VeSFET built on SOI

The device structure as shown in Fig.1b is defined in the form of cylindrical pillars forming the source, drain and two gate contacts. The radius of the cylinder r is the smallest printable disk in the available technology, and simultaneously the radius of electrodes and STI fillers as well as the radius of cylindrical part of gate trenches filled with polysilicon after sidewall oxidation. Assuming the centers of the gate trenches at x=y=$\pm$r. The minimal slit width W_s is defined as reprted in [10],

$$W_S = 2.[r(\sqrt{2}-1) - 0.44.t_{ox}] \quad (1)$$

where t_{ox} is the oxide thickness, the height of the VeSFET structure *h* (corresponding to a planar MOSFET's channel width) is equal to the SOI Si layer thickness. The substrate layer is uniformly doped with n-type impurities and polysilicon gates are doped with p-type impurities. To improve the channel conductance control, impurity concentrations in the gates, *N poly* (poly silicon gate doping) are much higher than the *Nsub* (substrate doping) concentration.

Table 1 Parameters used for the device simulation

Parameters	Value
Radius of metal pillars	50nm
Radius of STI fillers	50nm
Thickness of gate dielectric (t_{ox})	4nm
Slit width (W_s)	37.9nm
Height of the device (h)	200nm
Substrate doping (N_{sub})	4.75×10^{17} cm^{-3} to 5.25×10^{17} cm^{-3}
Polysilicon gate doping (N_{Poly})	$1\times10^{19}cm^{-3}$
Gate voltage for G1 and G2(TGC)	1.5V
Drain bias (V_{ds})	1.5V
High- k dielectric (Si_3N_4)	k=7.5
Low-k dielectric (SiO_2)	k=3.9

AND, OR and NOT functionality can be implemented in VeSFET by controlling the depletion regions created by the two gates overlap. There could be two ways to manipulate this overlap: (1) by using different doing level in the channel and (2) by using different slit width. The concept of AND, OR and NOT function implementation using slit width variation is illustrated schematically in Fig. 2. It is analogous to the sliding doors designed with overlap. In AND type transistors the depletion regions from gate-1, owing to smaller slit width, approaches gate-2 dielectric (spread over full channel) and vice versa. Schematic illustration of switching functionality between AND, OR and NOT by varying the slit width, controlling the overlap of the depletion regions is shown in Fig.2a,2b,2c respectively.

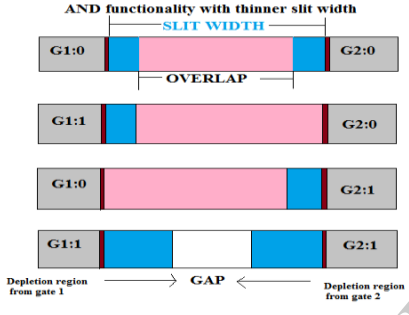


Fig. 2a: AND functionality with large overlap in depletion region such that high potential on one of the gates is unable to open the channel

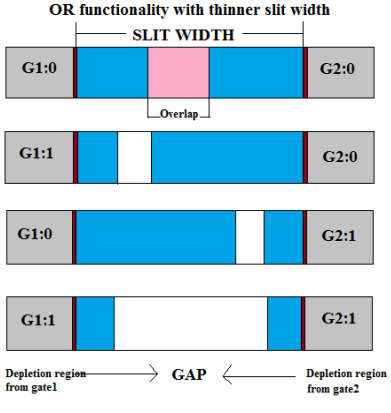
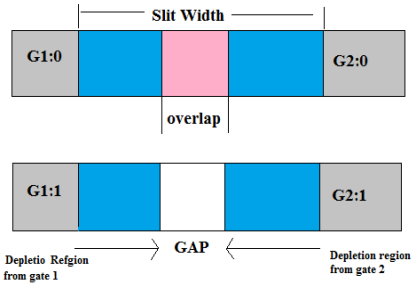


Fig. 2b: OR functionality with small overlap of depletion where high potential on any of the gates can open the channel. The concept is analogues to sliding doors with overlap

The inverter circuit can be easily implemented using single VeSFET device by providing low and high input at two gates of the device either TGC or IGC, thus the transistor count can be reduced from two to one as compare to CMOS technology.



INVERTER TGC

Fig. 2c: Inverter functionality of the VeSFET device with moderate substrate doping concentration.

Low input at both the gates resulting in merging of overlap region thus no current flows and output is also low. High input at both the gates withdraws the overlapped depletion region and provides a conducting path for current between source and drain results in high output.

3. Results and Discussions

The n channel VeSFET device at radius = 50nm is simulated using Sentaurus TCAD device simulator. The height of the device is 200nm, gate oxide thickness is 4.5nm, the substrate doping concentration is 5e+17cm^{-3} and boron concentration for twin gate structure is 1e+19cm^{-3} . The device is operated at 1.2V for TGC and IGC structure.

3.1 Electrical Characteristics of n channel VeSFET

The VeSFET structure of r=50nm which corresponds to CMOS technology at 90nm node is shown in Fig.3 generated by Sentaurus Structure Editor. The size of the single unit cell structure is 6r. Radius is considered as

minimum feature size for VeSFET structures [10].

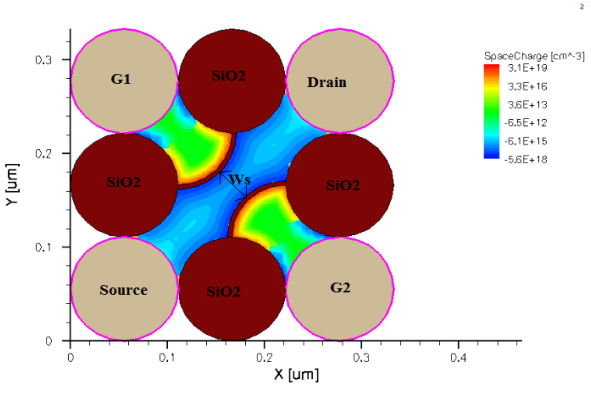


Fig. 3 n channel VeSFET structure using Sentaurus

The I_d-V_g characteristics of both devices VeSFET and MOSFET are shown in Fig.4a. at two different drain voltages V_{ds}=0.05V and 1.2V. Fig.4a describes the comparison of IGC, TGC VeSFET and nMOSFET for I_{off} current on logarithmic scale. When V_{ds} is very small i.e for 0.05V the off current for TGC is 2pA and for IGC mode it is 5pA. For TGC the off current is reduced by order of 2, whereas it is very much reduced when compared with conventional MOSFET as shown in Fig.4b.

When V_{ds} is increased from 0.05V to 1.2V the increment in off current is from 10^{-12} to 10^{-11} both for TGC and IGC configuration and for MOSFET it is increased by a value of 10 µA. The increase in off current with increase in drain voltage is due to drain induced barrier lowering (DIBL), DIBL is very common in very short channel devices. With the channel length scales down to 90nm or lower, the drain potential has very strong effect to the channel. This high drain to source voltage will roll off the threshold voltage. This is a 2-D effect.

For conventional MOSFET at 90nm node the increment in off current is upto 10µA where as it is 10pA for VeSFET as shown in fig.4a, it is evident from the figure that DIBL effect is affecting more the MOSFET devices as compare to the VeSFET (TGC and IGC both) as the rise in current is 10^5 times smaller in VeSFET device

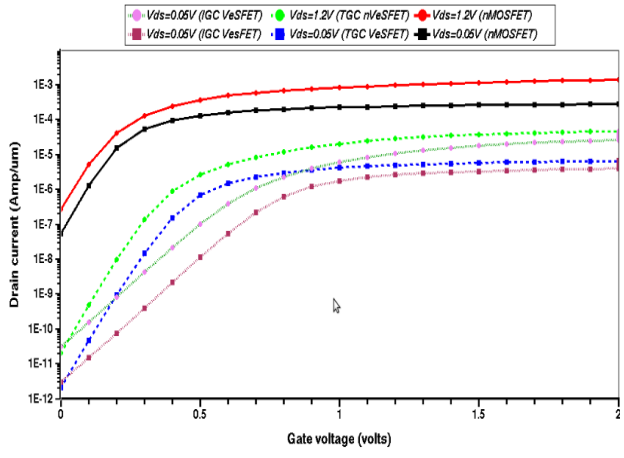


Fig. 4a Comparison of I_{off} current for IGC, TGC VeSFET and conventional MOSFET at 90nm node

The I_d-V_d characteristics of TGC and IGC modes of VeSFET are shown in Fig.4b and Fig.4c at different gate voltages ranging from V_{gs} at 0.0V to 1.5V.

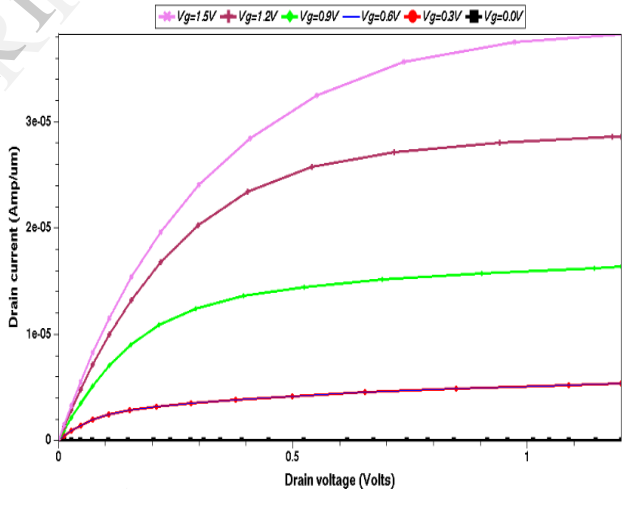


Fig. 4b I_d-V_d characteristics of n channel VeSFET (TGC)

Fig. 4a and 4b describes the output characteristics of n channel TGC and IGC VeSFET, characteristics are obtained at different gate voltages varying from 0V to 1.5V and keeping drain voltage fixed at supply voltage.

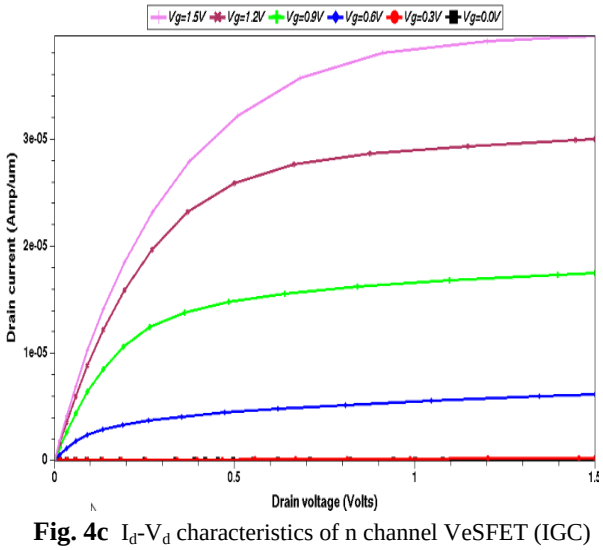


Fig. 4c I_d-V_d characteristics of n channel VeSFET (IGC)

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3.2 Variation in substrate and poly gate doping concentration

The opening of conducting channel for drift current flow between the depletion layers occurs at the gate voltage defined as threshold voltage V_{th}. In the case of tied gates it corresponds to the depletion regions induced by the gates meeting in the middle of the slit[13] .

The threshold voltage for VeSFET at zero drain bias voltage is given as [13]

$$V_{tho} = \varphi_{fb} - \eta . s_0 - (\frac{s_0}{\chi})^2 \quad (2)$$

$$\eta = \frac{qN_{sub}}{C_{ox}}, \quad (3)$$

$$\chi = \frac{2\varepsilon_{si}}{qN_{sub}} \quad (4)$$

Wher,C_{ox}=oxide acitance, N_{sub}= substrate doping and S_0= technological width. From equation (2) it is clear that with increase in the substrate doping of VeSFET device there is reduction in the threshold voltage. Threshold voltage of the device is also modified with technological width S_0 which is calculated as:

$$L = 2S_0 = \xi r ; \quad \xi = \frac{2-\frac{\pi}{2}}{\sqrt{2}-1} \cong 1.036 \quad (5)$$

ξ is resistance fitting coefficient (usually close to unity)[13]. The variation of substrate and gate doping concentrations its effect on threshold voltage and I_{off} current is shown in the Fig. 5a and Fig. 5b.

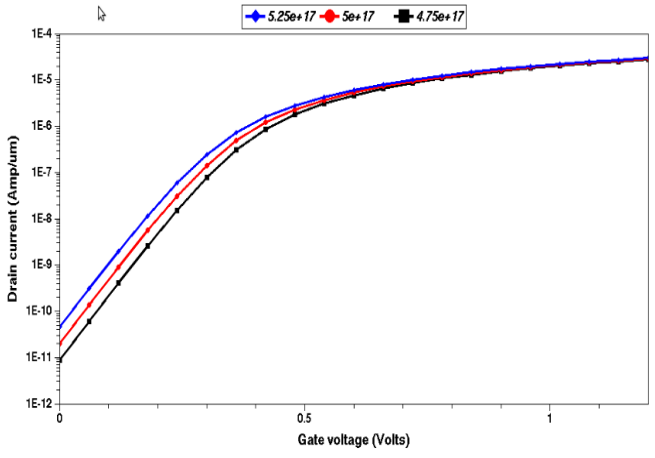

Fig.5a I_{off} variation at different substrate doping concentration

With increase in substrate doping the off current is increased by seven times in VeSFET (TGC) device. In order to increase the on current and to reduce the threshold voltage the substrate doping concentration should be increased with reduction in the gate doping concentration.

The variation in polysilicon gate doping concentration is shown in Fig.5b, with increase in poly gate doping concentration the threshold voltage is increased and the off current is reduced by an order of more than 100 in VeSFET (TGC) device, therefore an optimised value of poly gate doping should be considered for better performance.

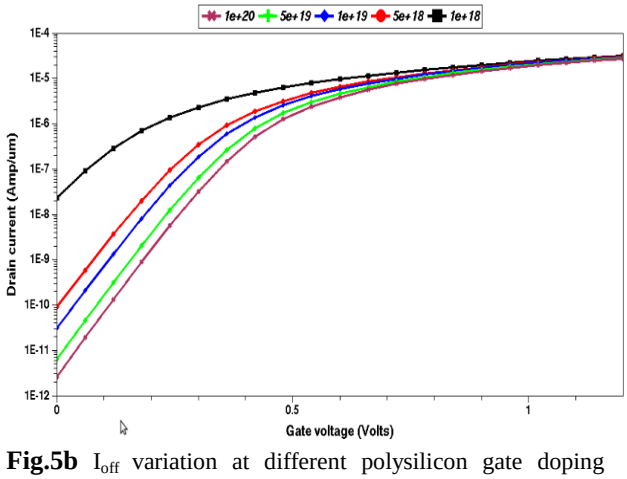

Fig.5b I_{off} variation at different polysilicon gate doping concentration

3.3 Si_3N_4 as Insulator

Taking Si_3N_4 as an insulator instead of taking SiO_2 shows reduction in off current as Si_3N_4 is having dielectric constant of 7.5 as compare to SiO_2 having dielectric constant of 3.9, so the capacitive control of gate is better in Si_3N_4 and it can be considered as a better insulator alternative for VeSFET structure

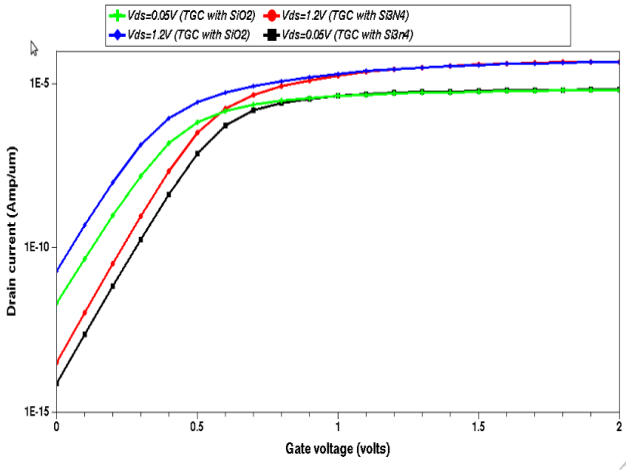

Fig. 6a Reduction in off current for TGC at two different drains voltage for VeSFET with Si_3N_4 and SiO_2 as insulator.

4. Conclusion

The comparison of electrical characteristics for reduction in I_{off} current in IGC and TGC configuration was done successfully. Based on the results it can be concluded that as compared to IGC VeSFET, TGC VeSFET shows more reduction in off current for two different drain voltages. Smaller I_{off} and steep subthreshold slope are very important characteristics which can reduce the power consumption as much as possible to prolong battery life. Simulations have shown reduction in I_{off} current with increase in gate doping concentration and reduction in substrate doping concentration. Reduction in off current with Si_3N_4 as an insulator is also reported through simulations.

5. References

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