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Performance Analysis of Various Universal Logic Redundant Adders

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***Abstract* - Redundant signed digit arithmetic is popular due to carry-free property. Adders form an almost obligatory component of every contemporary integrated circuit. The prerequisite of the adder is that it is primarily fast and secondarily efficient in terms of power consumption and chip area. This paper presents the pertinent choice for selecting the adder topology with the tradeoff between delay, power consumption and area. The adder topologies used in this work are redundant adders designed using universal gates. The module functionality and performance issues like area, power dissipation and propagation delay are analyzed at 0.12µm 6metal layer CMOS technology using Microwind & DSCH tool.**

Key Words: RBSD adder, verilogHDL, CMOS, high speed arithmetic, Layout Design.

1. INTRODUCTION

Digital computer arithmetic operations play a crucial role in many applications, where speed is essential, e.g., in digital signal processing, communications, cryptography, etc. Adders are also very significant component in digital systems because of their widespread use in other basic digital operations such as subtraction, multiplication and division. Hence, improving performance of the digital adder would extensively advance the execution of binary operations inside a circuit compromised of such blocks. Many different adder architectures for speeding up binary addition have been studied and proposed over the last decades.

Ripple Carry Adder (RCA) is the simplest, but slowest adders with O(n) area and O(n) delay, where n is the operand size in bits. Carry Look-Ahead (CLA) adder have O(n· log(n)) area and O(log(n)) delay, but typically suffer from irregular layout [6], [7]. Therefore RBSD adder cell based on redundant signed digit arithmetic is selected which can add two numbers of any bit length in constant time due to carry free property [1].

The design of physical layout is very tightly linked to overall circuit performance (area, speed, power dissipation) since the physical structure directly determines the trans-conductances of the transistor, the parasitic capacitance and resistances, and obviously, the silicon area which is used for a certain function. Here CMOS technology is used as it is the dominant technology in the global IC industry and it yields products with low power dissipation and is nearly ideal as a switching device. So for producing regular layout different architectures of RBSD adder cells are discussed and their area, delay and power is compared.

The functionality and performance analysis are done using Microwind and DSCH tool. Since Microwind integrates traditionally separated front-end and back-end chip design into an integrated flow, accelerating the design cycle and reduced design complexities. It tightly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification. Performance issues like area, power dissipation and propagation delay for all the adder cells are analyzed at 0.12µm 6metal layer CMOS technology.

The remaining part of this paper is organized as under. Section 2 explains the topology detail of various redundant signed digit adder cells using universal logic. Section 3 and 4 presents the simulation and performance analysis of adder cells respectively. Conclusion is presented in last section.

2. UNIVERSAL LOGIC RBSD ADDER CELL

This section presents the brief about four different architectures of universal logic RBSD adder cell (RAC) of which performance analysis is studied.

- NAND-NAND
- NOR-NOR
- Proposed NAND-NAND
- Proposed NOR-NOR

Kal and Rajashekhar, 1990 [4] has given following Boolean expressions for the design of RBSD adder cell.

$$d_i = m_i \oplus \overline{xip}\,\overline{xin} \oplus \overline{yip}\,\overline{yin} \quad (1)$$

$$m_{i+1} = \overline{xip}\;\overline{yip} \quad (2)$$

$$b_{i+1} = \overline{m_i}\;\overline{xip}\,\overline{xin} + \overline{m_i}\;\overline{yip}\,\overline{yin} + xip\;yip + \overline{xip}\,\overline{xin}\;\;\overline{yip}\,\overline{yin} \quad (3)$$

$$sip = \overline{d_i} bi \quad (4)$$

$$sin = d_i \overline{b_i} \quad (5)$$

With the help of equations 1-5, Kal and Rajashekhar designed a RBSD adder cell which was made by using different type of logic gates i.e. AND, OR, NOR, XOR, NOT etc. [2].

2.1 RAC: NAND-NAND / RAC:NOR-NOR

In digital design techniques, much attention has to be paid to network design in the form of repeated pattern of identical circuits. Due to the similar type of gate (NAND or NOR), NMOS and CMOS designs are easy for the designer as there is repetition of similar design and hence uniformity in circuit. These circuits can be designed by using universal gates as these gates are in-expensive in manufacturing aspects also. Keeping above aspects in mind RBSD adder cell is designed using NOR-NOR logic and NAND-NAND logic by N. Sharma in 2006 shown in fig. 1 and fig. 2 respectively [4].

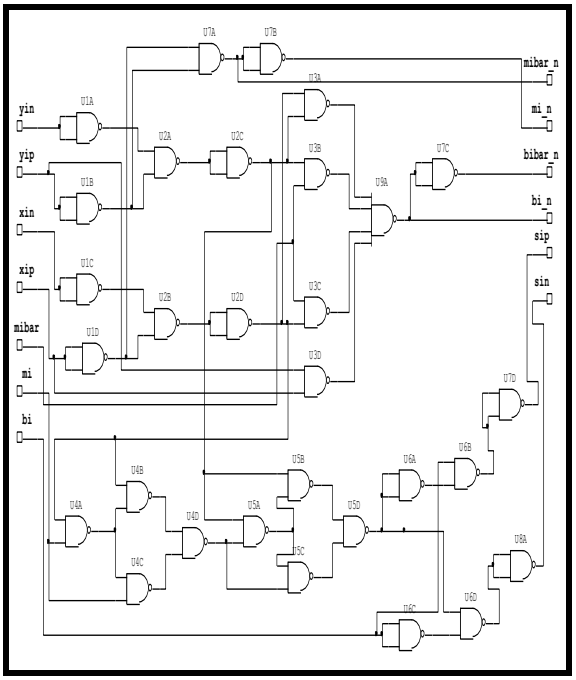

Figure -1: RAC:NAND-NAND

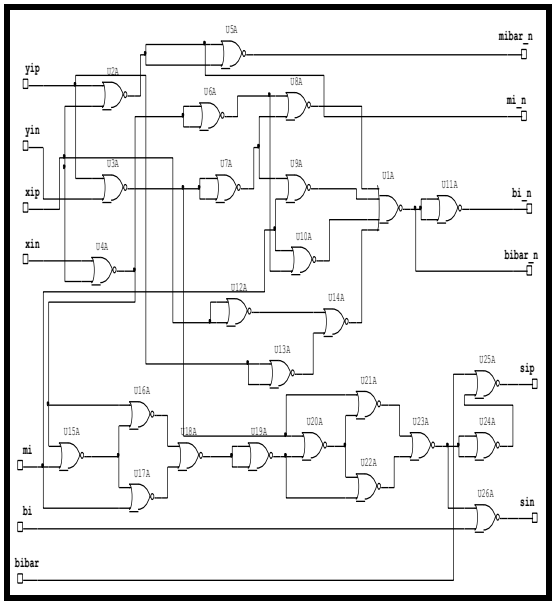

Figure -2: RAC:NOR-NOR

2.2 Proposed RAC:NAND-NAND and Proposed RAC:NOR-NOR

Further to reduce the hardware complexity and delay, proposed architectures of adder cells are suggested by the author. These circuits are designed with reduced number of (i) NOR gates and (ii) NAND gates as shown in fig. 3 and fig. 4 respectively [3].

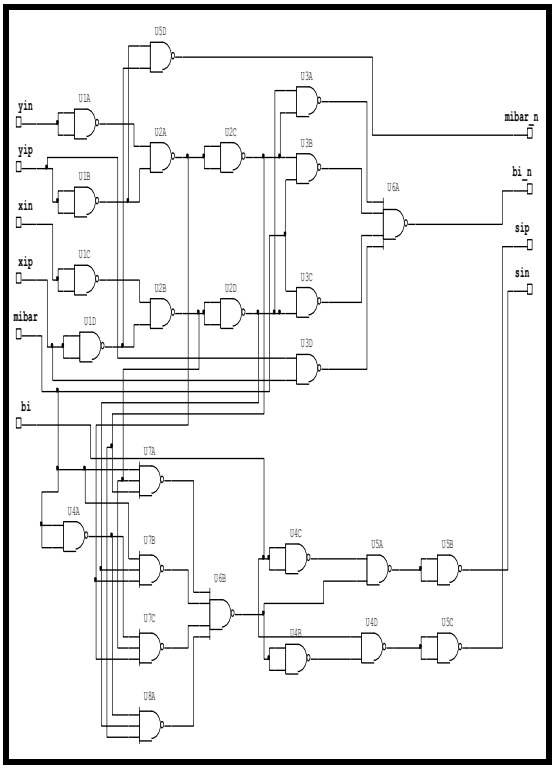

Figure -3: Proposed RAC:NAND-NAND

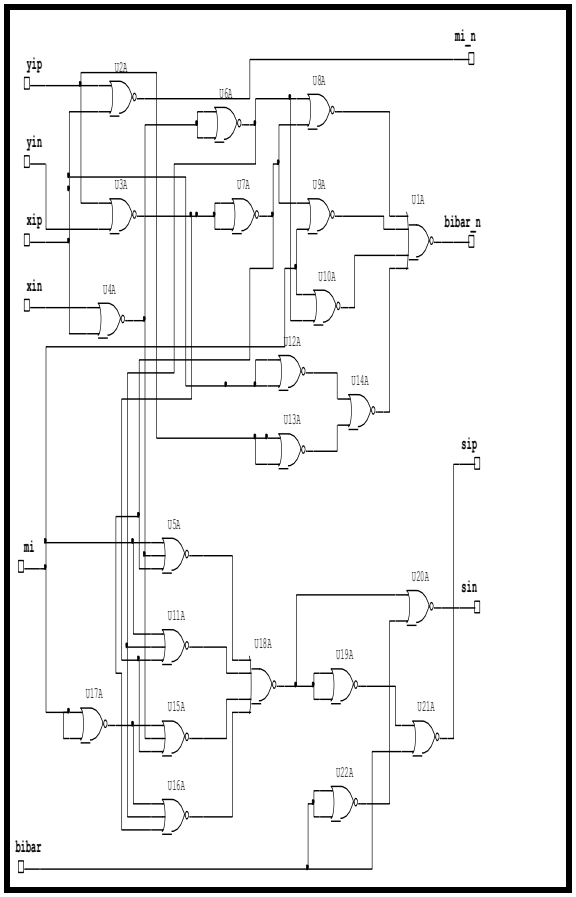

Figure -4: Proposed RAC:NOR-NOR

3. SIMULATION RESULTS

Above mentioned adder cells are designed using 0.12µm CMOS technology using Microwind (MW). This software is dedicated to the training in sub micron CMOS VLSI design, consisting in a layout editor, electrical circuit extractor and a fast online analog simulator. Lambda is 0.06µm (60nm). The Microwind simulation provides two environments like logic editor and simulator. They are DSCH and MW which are used to validate logic design simulation with delay analysis and physical circuit extraction. All the adders used in this work are simulated using DSCH. First the simulation is performed using schematic entry and its corresponding test patterns are generated and its functionality is verified. After verification the schematic file is converted to VERILOG file.

Thereafter using Microwind environment, the VERILOG file is used to generate physical layout of logic design. All simulations are carried out at nominal conditions: V_{DD}=1.2V, I/O supply voltage:2.5 V and room temperature = 27 oC. The device model used in this simulation is empirical level 3 at High Speed. Other parameters of nMOS and pMOS are set as follows.

Parameter	nMOS	pMOS
W, L	0.240µm, 0.120µm (4λx2λ)	
VTO	0.30	-0.30
LD	0.00	0.00
UO	0.060	0.030
TOX	3.500	3.500
PHI	0.20	0.20
GAMMA	0.40	0.40
KAPPA	0.06	0.06
THETA	0.50	0.30
VMAX	120.00	110.00
NSS	0.06	0.06

To establish an unbiased testing environment, the simulations have been carried out using a comprehensive input signal pattern. After simulation area of the layout, delay and power dissipation in different adder cell structures [figure 1-4] are noted which are presented in table 1.

Table -1: Area Delay & Power Dissipation

Type of RAC	Area (μm^2)	Delay (ns)	Power Dissipation (µW) at Vdd 1.2 V
NOR-NOR	572.9	2.230	44.401
Proposed NOR-NOR	606.1	1.460	40.161
NAND-NAND	674.6	2.460	50.590
Proposed NAND-NAND	690.4	2.075	98.156

Graphs drawn in figure 5, 6 and 7 show the comparison among different adder cells for layout area, delay and power dissipation respectively. It has been shown that Proposed NOR-NOR adder cell is the best in delay and power dissipation but the layout area is approximately equal as in NOR-NOR.

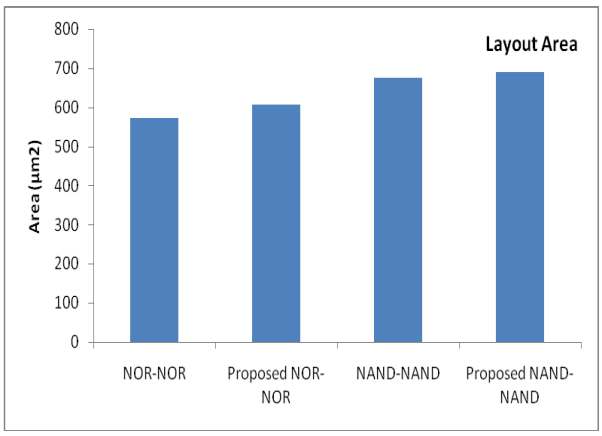

Figure -5: Comparison of Layout Area

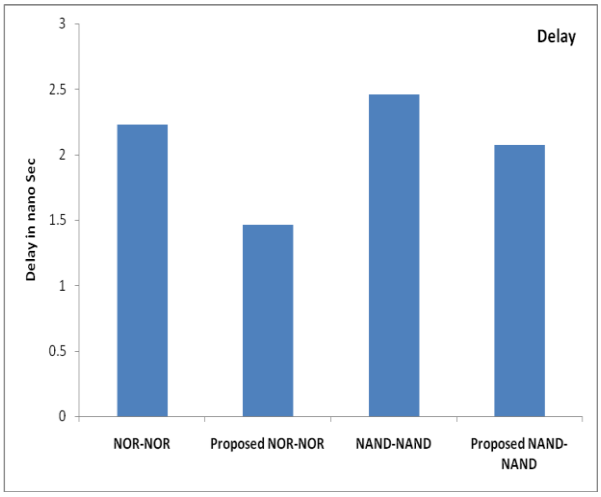

Figure -6: Comparison of Delay

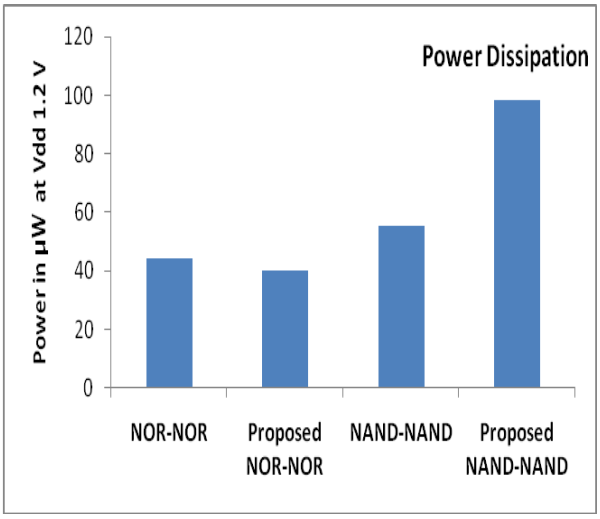

Figure -7: Comparison of Power Dissipation

4. PERFORMANCE ANALYSIS

For analyzing the performance of different adder cell architectures overall performance parameters AT, AT^2 and PD values for different adder cells are computed from the data in table 1.

Table -2: AT, AT^2 and PD values of Adder

Type of RAC	AT	AT^2	PD
NOR-NOR	1277.567	2848.974	99.01423
Proposed NOR-NOR	884.906	1291.963	58.63506
NAND-NAND	1659.516	4082.409	124.4514
Proposed NAND-NAND	1432.58	2972.604	203.6737

These values for different adder cells are plotted in figure 8. It is again proved that AT, AT^2 and PD values are less in for Proposed NOR- NOR and NAND-NAND adder cell.

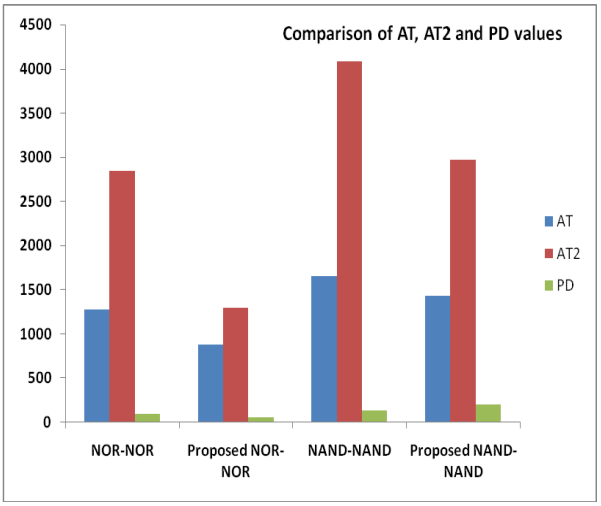

Figure -8: Comparison of adder cell in terms AT, AT^2 and PD

Power dissipation in various adder cells with respect to change in V_{DD} up to 2V is also computed which is given in table 4. By plotting these values it is clear from figure 9 that power dissipation at different V_{DD} is least in Proposed NOR-NOR adder cell.

Table -3: Power Dissipation at different V_{DD}

Type of RAC	Variation in V_{DD} upto 2 V									
	0.2	0.4	0.6	0.8	1	1.2	1.4	1.6	1.8	2
NOR-NOR	0	0.003	0.019	0.026	0.036	0.044	0.053	0.063	0.077	0.127
Proposed NOR-NOR	**0**	**0.003**	**0.019**	**0.026**	**0.033**	**0.04**	**0.047**	**0.055**	**0.065**	**0.1**
NAND-NAND	0.001	0.007	0.026	0.035	0.045	0.056	0.067	0.09	0.107	0.187
Proposed NAND-NAND	0.001	0.007	0.035	0.079	0.088	0.098	0.108	0.118	0.134	0.22

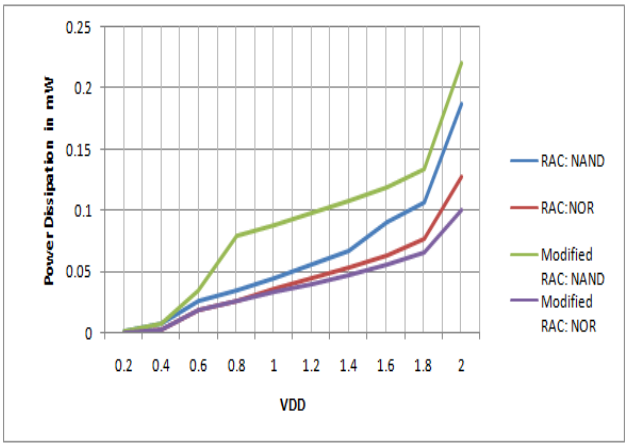

Figure -9: Power dissipation with change in V_{DD}

5. CONCLUSION

In this work, an exhaustive analysis of adder topologies in 0.12µm CMOS technologies has been carried out. The performances of various adder cells are tested for robustness against area, delay and power dissipation. Proposed Redundant Adder Cell NOR-NOR architecture is fastest with least power dissipation with slight increase in area as compared to NOR-NOR. Therefore this is suitable further to implement other arithmetic circuit so a compromise can be accepted in chip area. Pertinent choice of adder topologies is essential in the design of VLSI integrated circuits for high speed and high performance CMOS circuits. According to the presented results architecture of this adder cell has the best compromise among area, delay and power dissipation and is suitable for high performance and low-power circuits.

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BIOGRAPHIES

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